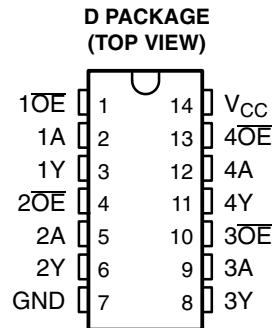


- Qualified for Automotive Applications
- Typical V_{OLP} (Output Ground Bounce) <1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs (-16-mA I_{OH} , 32-mA I_{OL})
- I_{off} and Power-Up 3-State Support Hot Insertion
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)



description/ordering information

The SN74ABT125Q-Q1 quadruple bus buffer gate features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (\overline{OE}) input is high.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION[†]

T_A	PACKAGE [‡]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC – D	Tape and reel	SN74ABT125QDRQ1	ABT125Q

[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

[‡] Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTION TABLE (each buffer)

INPUTS		OUTPUT Y
\overline{OE}	A	
L	H	H
L	L	L
H	X	Z

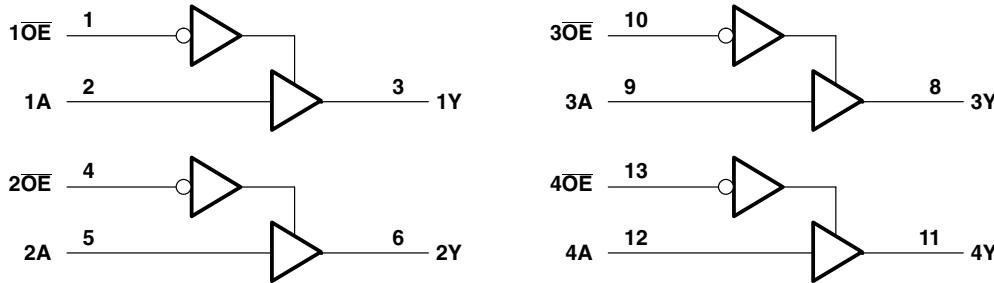


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SN74ABT125Q-Q1
QUADRUPLE BUS BUFFER GATE
WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	-0.5 V to 5.5 V
Current into any output in the low state, I_O	126 mA
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2)	86°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JEDEC 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
I_{OH}	High-level output current		-16	mA
I_{OL}	Low-level output current		32	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		$\mu s/V$
T_A	Operating free-air temperature	-40	125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT	
		MIN	TYP [†]	MAX				
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2	-1.2	-1.2	V	
V_{OH}	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$	2.5		2.5			V	
	$V_{CC} = 5\text{ V}$, $I_{OH} = -3\text{ mA}$	3		3				
	$V_{CC} = 4.5\text{ V}$ $I_{OH} = -16\text{ mA}$	2		2				
V_{OL}	$V_{CC} = 4.5\text{ V}$ $I_{OL} = 32\text{ mA}$		0.55		0.55	0.55	V	
V_{hys}		100					mV	
I_I	$V_{CC} = 0$ to 5.5 V , $V_I = V_{CC}$ or GND		± 1		± 1	± 1	μA	
I_{OZPU}	$V_{CC} = 0$ to 2.1 V , $V_O = 0.5\text{ V}$ to 2.7 V , $\overline{OE} = X$		± 50		± 50	± 50	μA	
I_{OZPD}	$V_{CC} = 2.1\text{ V}$ to 0 , $V_O = 0.5\text{ V}$ to 2.7 V , $\overline{OE} = X$		± 50		± 50	± 50	μA	
I_{OZH}	$V_{CC} = 2.1\text{ V}$ to 5.5 V , $V_O = 2.7\text{ V}$, $\overline{OE} \geq 2\text{ V}$		10		10	10	μA	
I_{OZL}	$V_{CC} = 2.1\text{ V}$ to 5.5 V , $V_O = 0.5\text{ V}$, $\overline{OE} \geq 2\text{ V}$		-10		-10	-10	μA	
I_{off}	$V_{CC} = 0$, V_I or $V_O \leq 4.5\text{ V}$		± 100				μA	
I_{CEX}	$V_{CC} = 5.5\text{ V}$, $V_O = 5.5\text{ V}$	Outputs high		50		50	μA	
I_O^{\ddagger}	$V_{CC} = 5.5\text{ V}$, $V_O = 2.5\text{ V}$		-50	-100	-200 [§]	-50	-200 [§]	mA
I_{CC}	$V_{CC} = 5.5\text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND	Outputs high		1	250	250	μA	
		Outputs low		24	30	30	mA	
		Outputs disabled		0.5	250	250	μA	
ΔI_{CC}^{\dagger}	Data inputs	$V_{CC} = 5.5\text{ V}$, One input at 3.4 V , Other inputs at V_{CC} or GND	Outputs enabled		1.5	1.5	mA	
			Outputs disabled		0.05	0.05		
Control inputs		$V_{CC} = 5.5\text{ V}$, One input at 3.4 V , Other inputs at V_{CC} or GND			1.5	1.5		
C_I	$V_I = 2.5\text{ V}$ or 0.5 V		3				pF	
C_O	$V_O = 2.5\text{ V}$ or 0.5 V		7				pF	

[†] All typical values are at $V_{CC} = 5\text{ V}$.

[‡] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[§] This limit may vary among suppliers.

[¶] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

SN74ABT125Q-Q1
QUADRUPLE BUS BUFFER GATE
WITH 3-STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

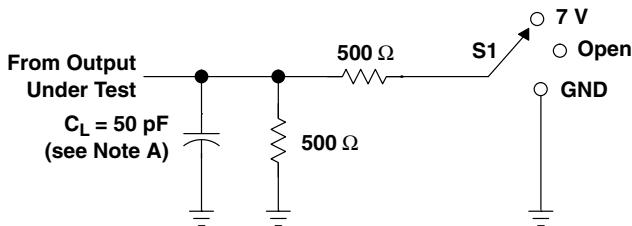
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t _{PLH} [†]	A	Y	1	3.2	4.6	1	6	ns
t _{PHL} [†]			1	2.5	4.6	1	6.2	
t _{PZH} [†]	OE	Y	1	3.6	5	1	6	ns
t _{PZL} [†]			1	2.5	6.2	1	7.5	
t _{PHZ}	OE	Y	1	3.8	5.4	1	6.3	ns
t _{PLZ} [†]			1	3.3	5.3	1	6.5	

[†] This limit may vary among suppliers.

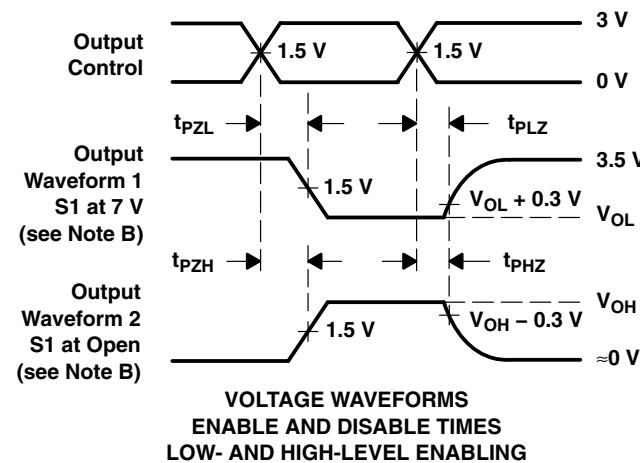
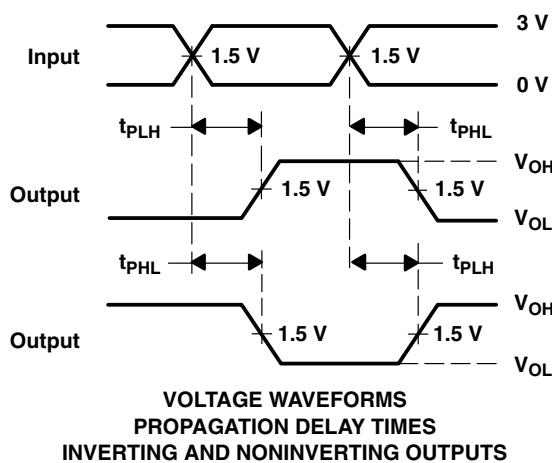
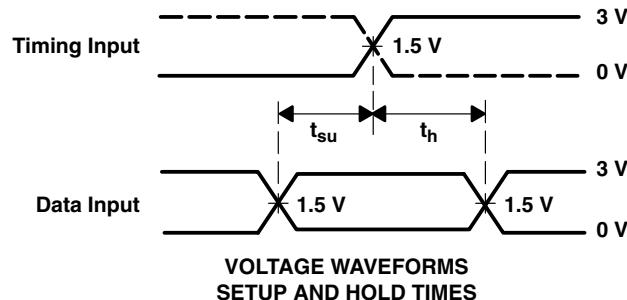
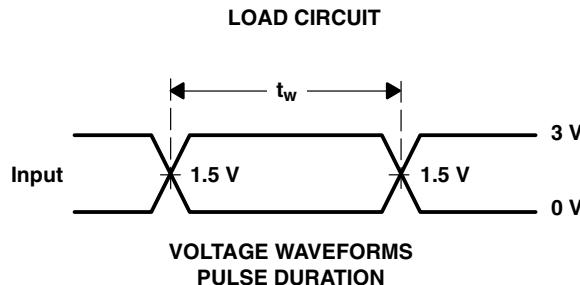


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PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



NOTES:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ABT125QDRG4Q1	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ABT125Q
SN74ABT125QDRG4Q1.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ABT125Q
SN74ABT125QDRQ1	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ABT125Q
SN74ABT125QDRQ1.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ABT125Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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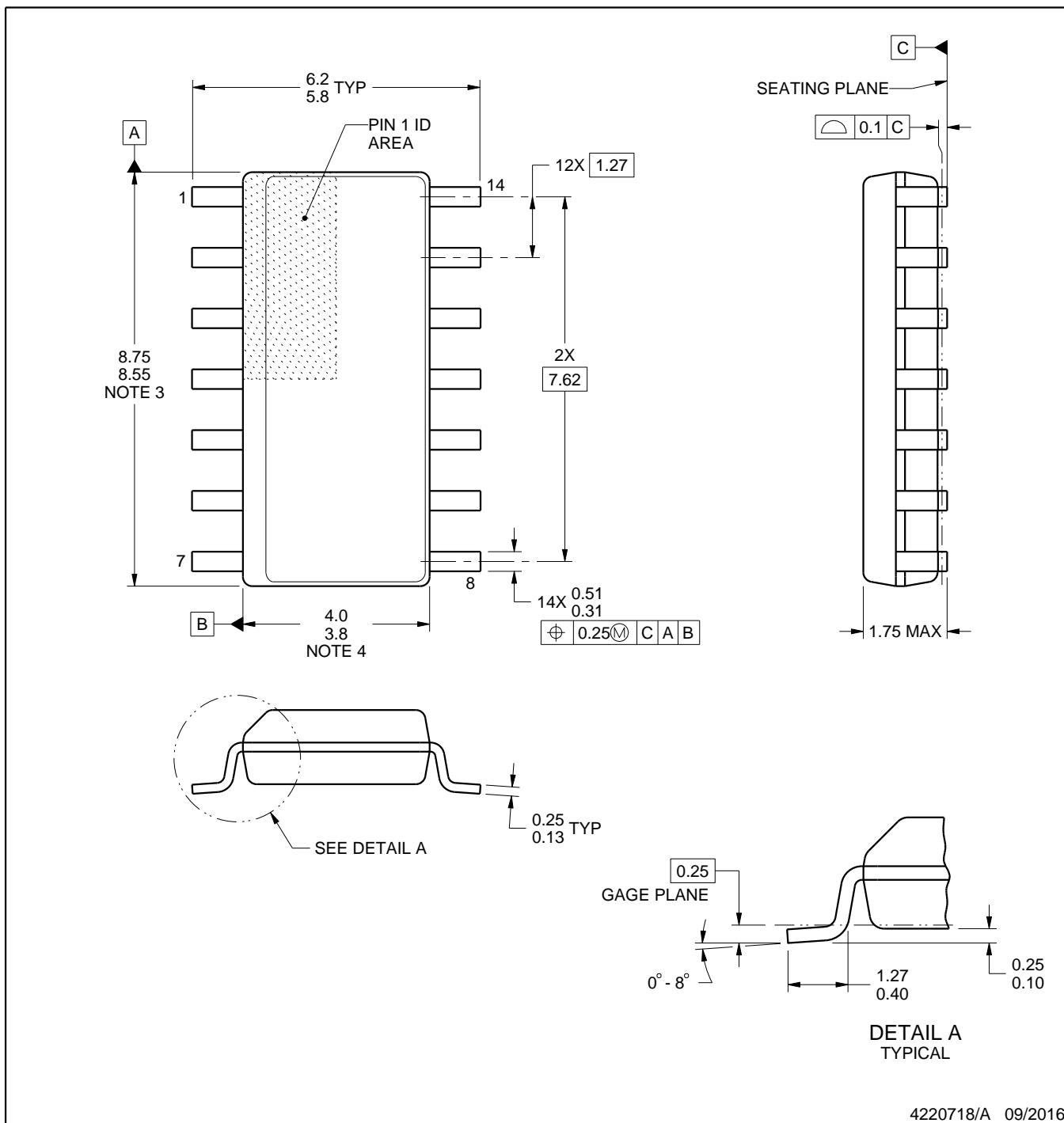
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PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

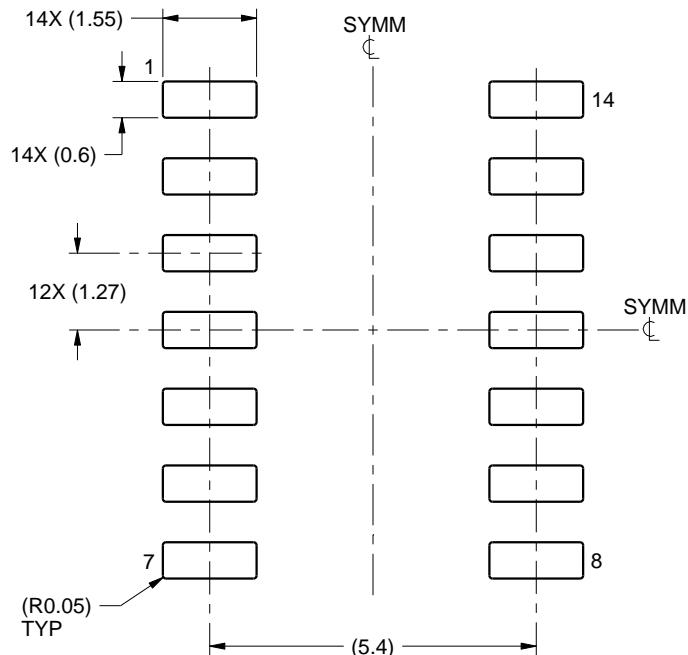
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

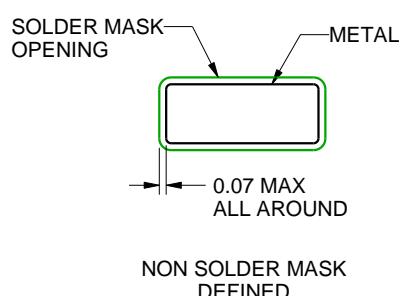
D0014A

SOIC - 1.75 mm max height

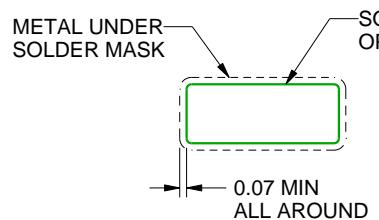
SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

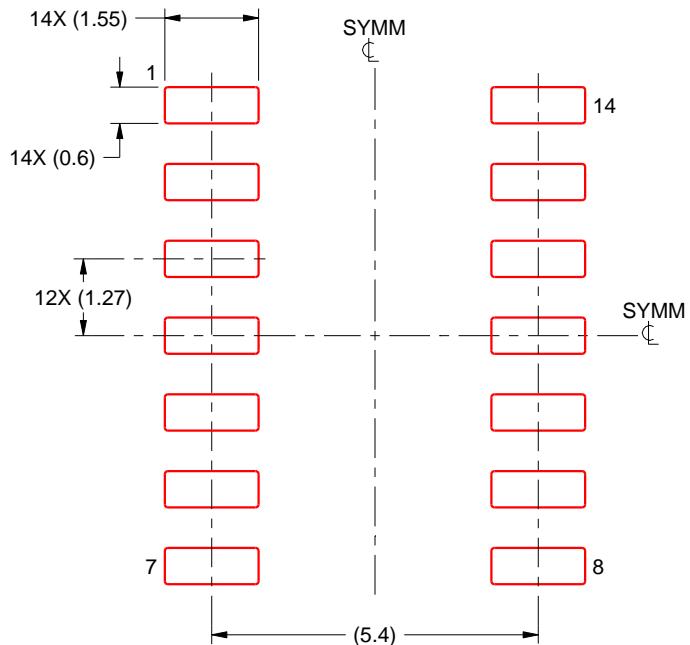
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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