



PSMN040-100MSE

N-channel 100 V 36.6 mΩ standard level MOSFET in LFPAK33
designed specifically for high power PoE applications

26 March 2013

Product data sheet

1. General description

New standards and proprietary approaches are enabling Power-over-Ethernet (PoE) systems capable of delivering up to 90W to each powered device (PD). Such solutions place increased demands on the power sourcing equipment (PSE) in terms of “soft-start”, thermal management and power density requirements.

2. Features and benefits

- Enhanced forward biased safe operating area for superior linear mode operation
- Low $R_{DS(on)}$ for low conduction losses
- Ultra reliable LFPAK33 package for superior thermal and ruggedness performance
- Very low I_{DSS}

3. Applications

- High power PoE applications (60W and higher)
- IEEE802.3at and proprietary solutions

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25^\circ\text{C}$; $T_j \leq 175^\circ\text{C}$	-	-	100	V
I_D	drain current	$T_j = 25^\circ\text{C}$; $V_{GS} = 10\text{ V}$; Fig. 1	-	-	30	A
P_{tot}	total power dissipation	$T_{mb} = 25^\circ\text{C}$; Fig. 2	-	-	91	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 10\text{ A}$; $T_j = 25^\circ\text{C}$; Fig. 13	-	29.4	36.6	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}$; $I_D = 10\text{ A}$; $V_{DS} = 50\text{ V}$	-	10.7	-	nC
$Q_{G(tot)}$	total gate charge	$T_j = 25^\circ\text{C}$; Fig. 14 ; Fig. 15	-	30	-	nC
Avalanche Ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(init)} = 25^\circ\text{C}$; $I_D = 30\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\Omega$; unclamped; Fig. 3	-	-	54	mJ

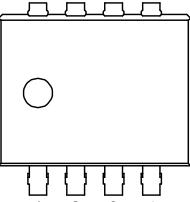
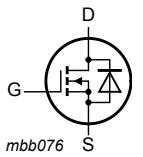


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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain	 LFPAK33 (SOT1210)	

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN040-100MSE	LFPAK33	Plastic single ended surface mounted package (LFPAK33); 4 leads	SOT1210

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN040-100MSE	M40E10

8. Limiting values

Table 5. Limiting values

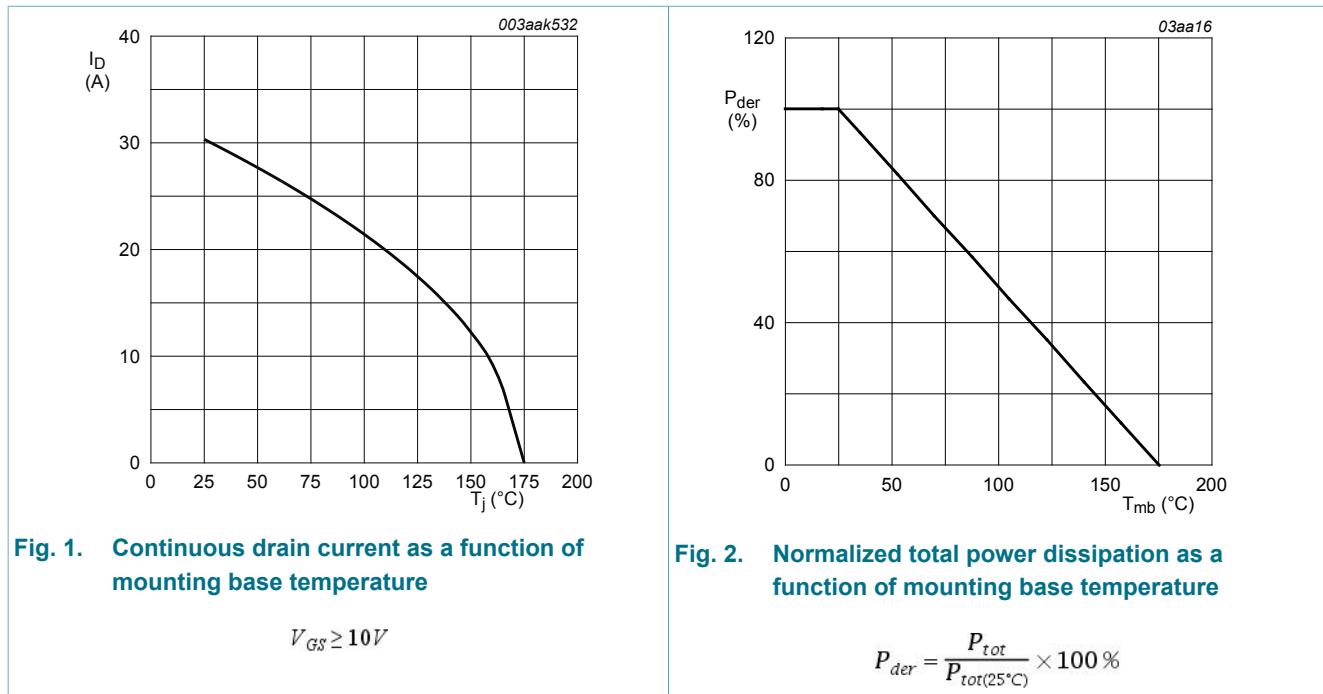
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25^\circ\text{C}$; $T_j \leq 175^\circ\text{C}$	-	100	V
V_{DGR}	drain-gate voltage	$T_j \geq 25^\circ\text{C}$; $T_j \leq 175^\circ\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_j = 25^\circ\text{C}$; Fig. 1	-	30	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100^\circ\text{C}$; Fig. 1	-	21	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25^\circ\text{C}$; Fig. 4	-	121	A
P_{tot}	total power dissipation	$T_{mb} = 25^\circ\text{C}$; Fig. 2	-	91	W
T_{stg}	storage temperature		-55	175	°C

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Symbol	Parameter	Conditions	Min	Max	Unit
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25$ °C	[1]	-	70 A
I_{SM}	peak source current	pulsed; $t_p \leq 10$ µs; $T_{mb} = 25$ °C	-	121	A
Avalanche Ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; $I_D = 30$ A; $V_{sup} \leq 100$ V; $R_{GS} = 50$ Ω; unclamped; Fig. 3	-	54	mJ

[1] Continuous current is limited by package.



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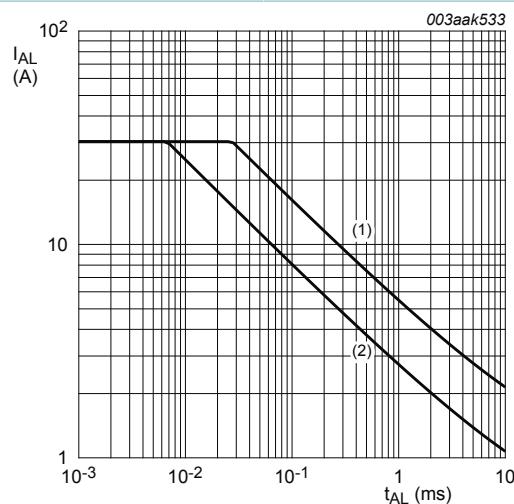


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1) $T_j \text{ (init)} = 25^\circ\text{C}$; (2) $T_j \text{ (init)} = 100^\circ\text{C}$

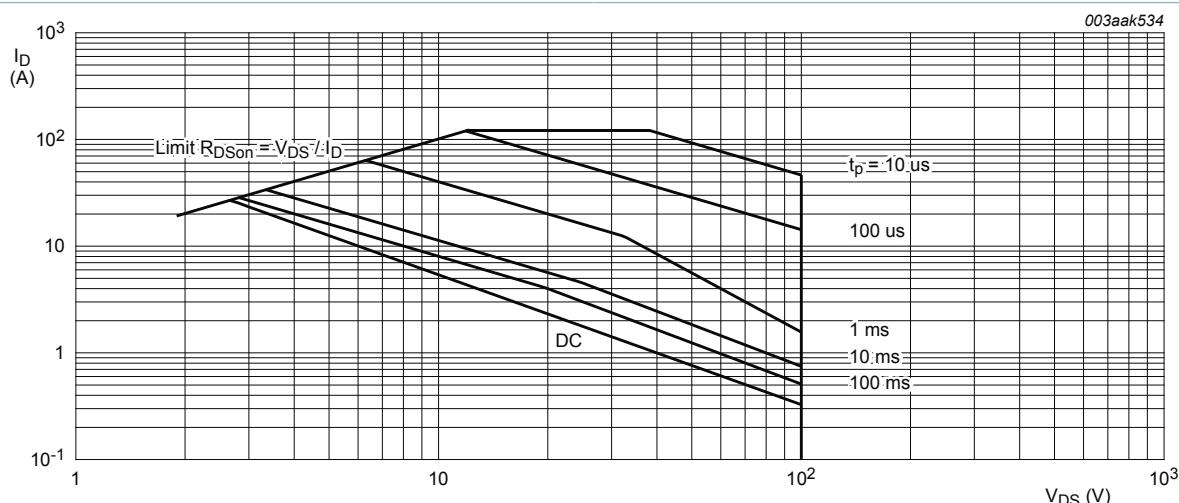


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^\circ\text{C}$; I_{DM} is a single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	1.44	1.65	K/W

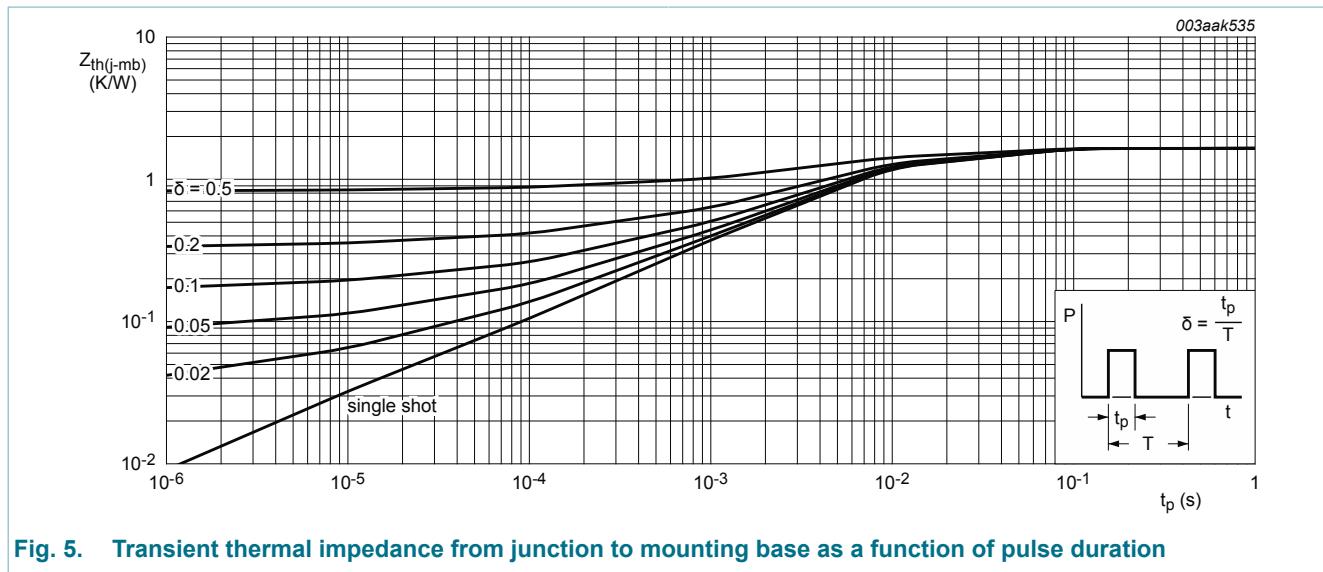


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25^\circ C$		100	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55^\circ C$		90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25^\circ C;$ Fig. 10 ; Fig. 11		2.3	3.3	4	V
		$I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55^\circ C;$ Fig. 10		-	-	4.6	V
		$I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175^\circ C;$ Fig. 10		1	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25^\circ C$		-	0.05	1	μA
		$V_{DS} = 100 V; V_{GS} = 0 V; T_j = 175^\circ C$		-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	10	100	nA
		$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	10	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 10 A; T_j = 100^\circ C;$ Fig. 12 ; Fig. 13		-	-	66	$m\Omega$
		$V_{GS} = 10 V; I_D = 10 A; T_j = 175^\circ C;$ Fig. 12 ; Fig. 13		-	-	99	$m\Omega$
		$V_{GS} = 10 V; I_D = 10 A; T_j = 25^\circ C;$ Fig. 13		-	29.4	36.6	$m\Omega$
R_G	gate resistance	$f = 10 MHz$		-	1.65	-	Ω

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
$Q_{G(\text{tot})}$	total gate charge	$I_D = 10 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C}$; Fig. 14 ; Fig. 15		-	30	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C}$		-	24	-	nC
Q_{GS}	gate-source charge	$I_D = 10 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C}$; Fig. 14 ; Fig. 15		-	7.6	-	nC
$Q_{GS(\text{th})}$	pre-threshold gate-source charge			-	4.5	-	nC
$Q_{GS(\text{th-pl})}$	post-threshold gate-source charge			-	3.1	-	nC
Q_{GD}	gate-drain charge			-	10.7	-	nC
$V_{GS(\text{pl})}$	gate-source plateau voltage	$I_D = 10 \text{ A}; V_{DS} = 50 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$; Fig. 14 ; Fig. 15		-	5.6	-	V
C_{iss}	input capacitance	$V_{DS} = 50 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C}$; Fig. 16		-	1470	-	pF
C_{oss}	output capacitance			-	110	-	pF
C_{rss}	reverse transfer capacitance			-	80	-	pF
$t_{d(\text{on})}$	turn-on delay time	$V_{DS} = 50 \text{ V}; R_L = 5 \Omega; V_{GS} = 10 \text{ V};$ $R_{G(\text{ext})} = 5 \Omega; T_j = 25 \text{ }^\circ\text{C}$		-	8.3	-	ns
t_r	rise time			-	14.1	-	ns
$t_{d(\text{off})}$	turn-off delay time			-	18.7	-	ns
t_f	fall time			-	13	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 20 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$; Fig. 17		-	0.82	1.2	V
t_{rr}	reverse recovery time	$I_S = 10 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$ $V_{DS} = 50 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$		-	41	-	ns
Q_r	recovered charge			-	75	-	nC

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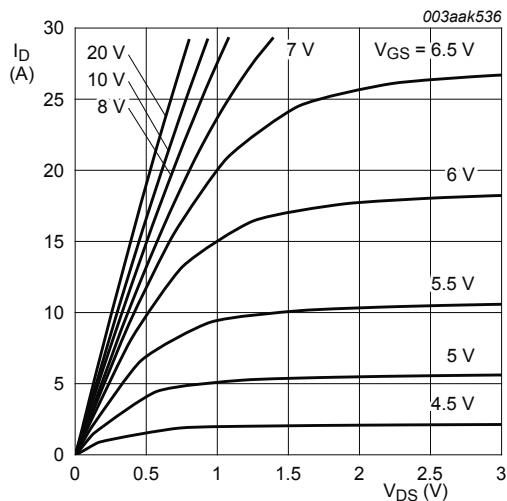


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

$T_j = 25^\circ C$

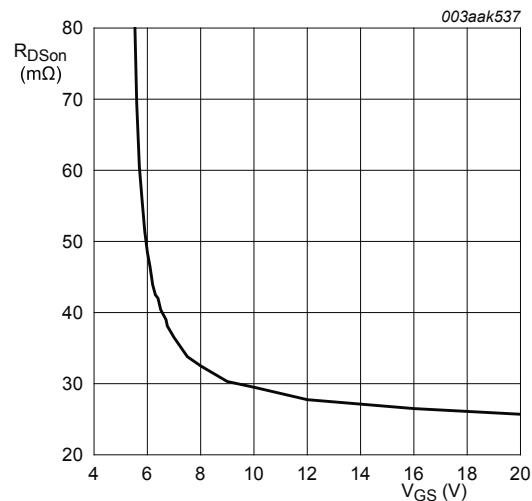


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25^\circ C; I_D = 10A$

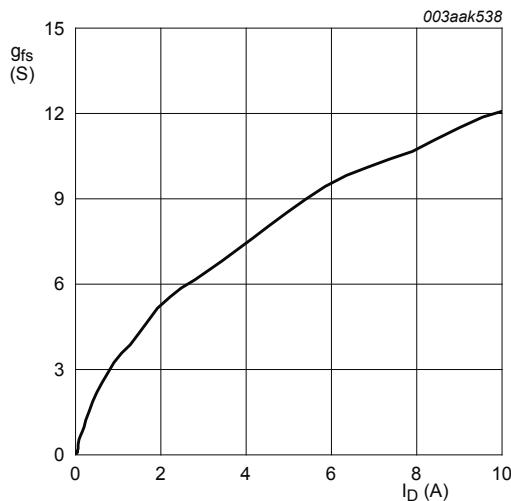


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25^\circ C; V_{DS} = 10V$

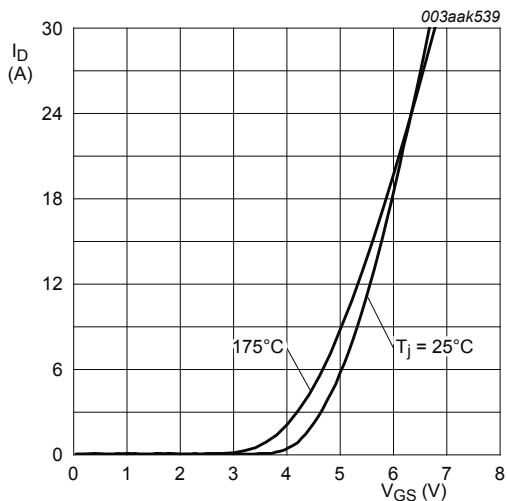


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10V$

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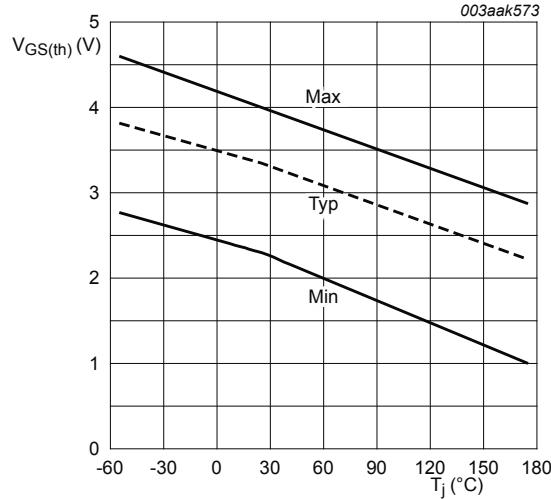


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

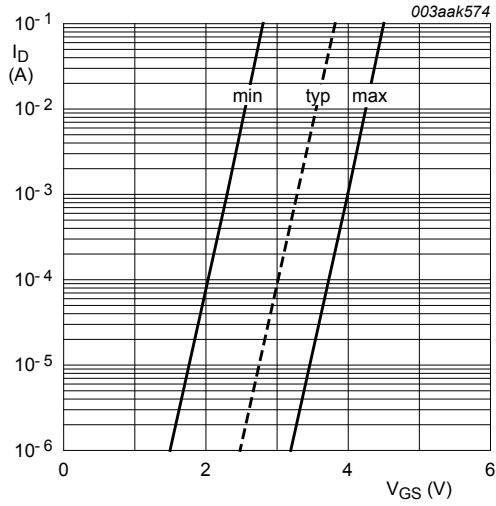


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

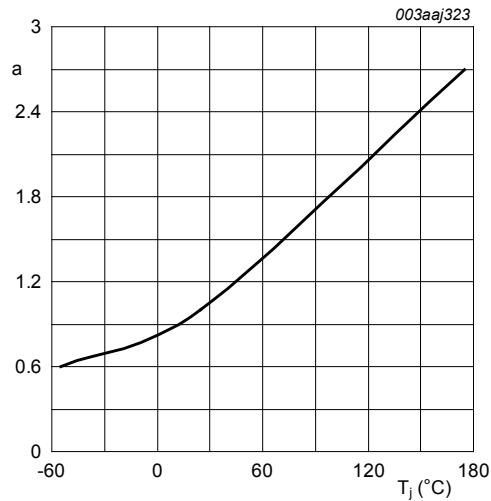


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

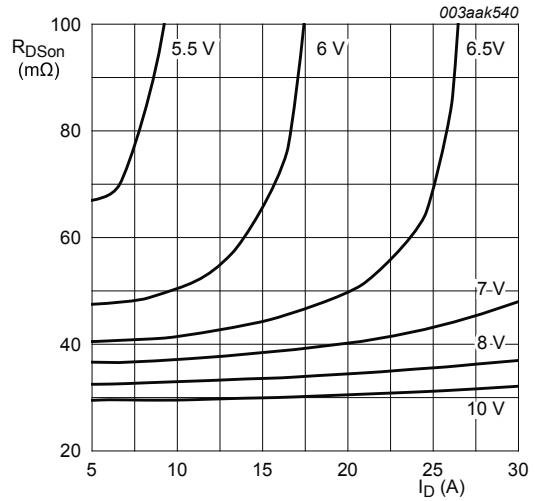


Fig. 13. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^\circ\text{C}$

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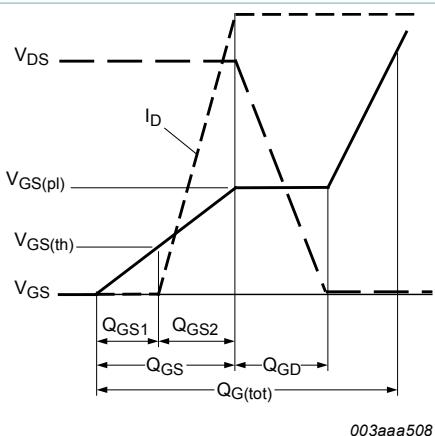


Fig. 14. Gate charge waveform definitions

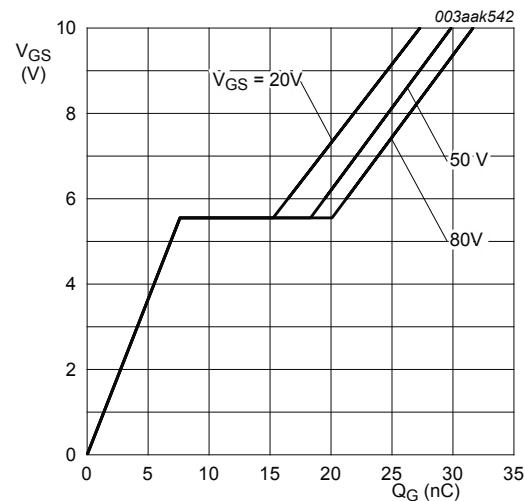


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^\circ\text{C}$; $I_D = 10\text{A}$

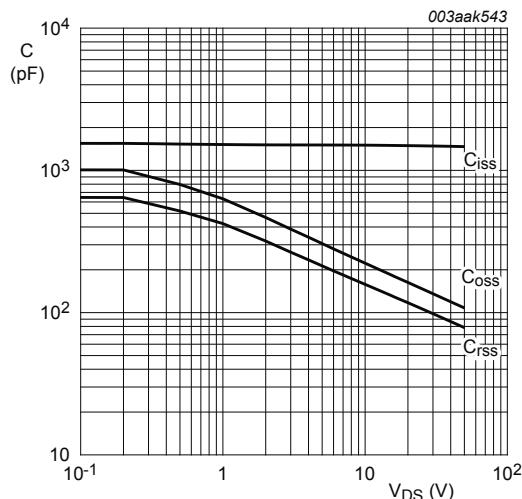


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0\text{V}$; $f = 1\text{MHz}$

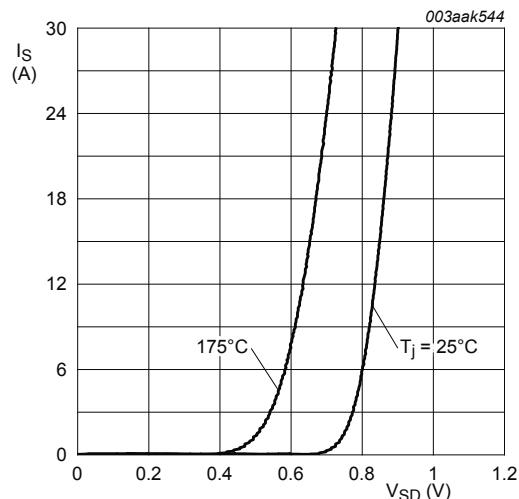


Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0\text{V}$

11. Package outline

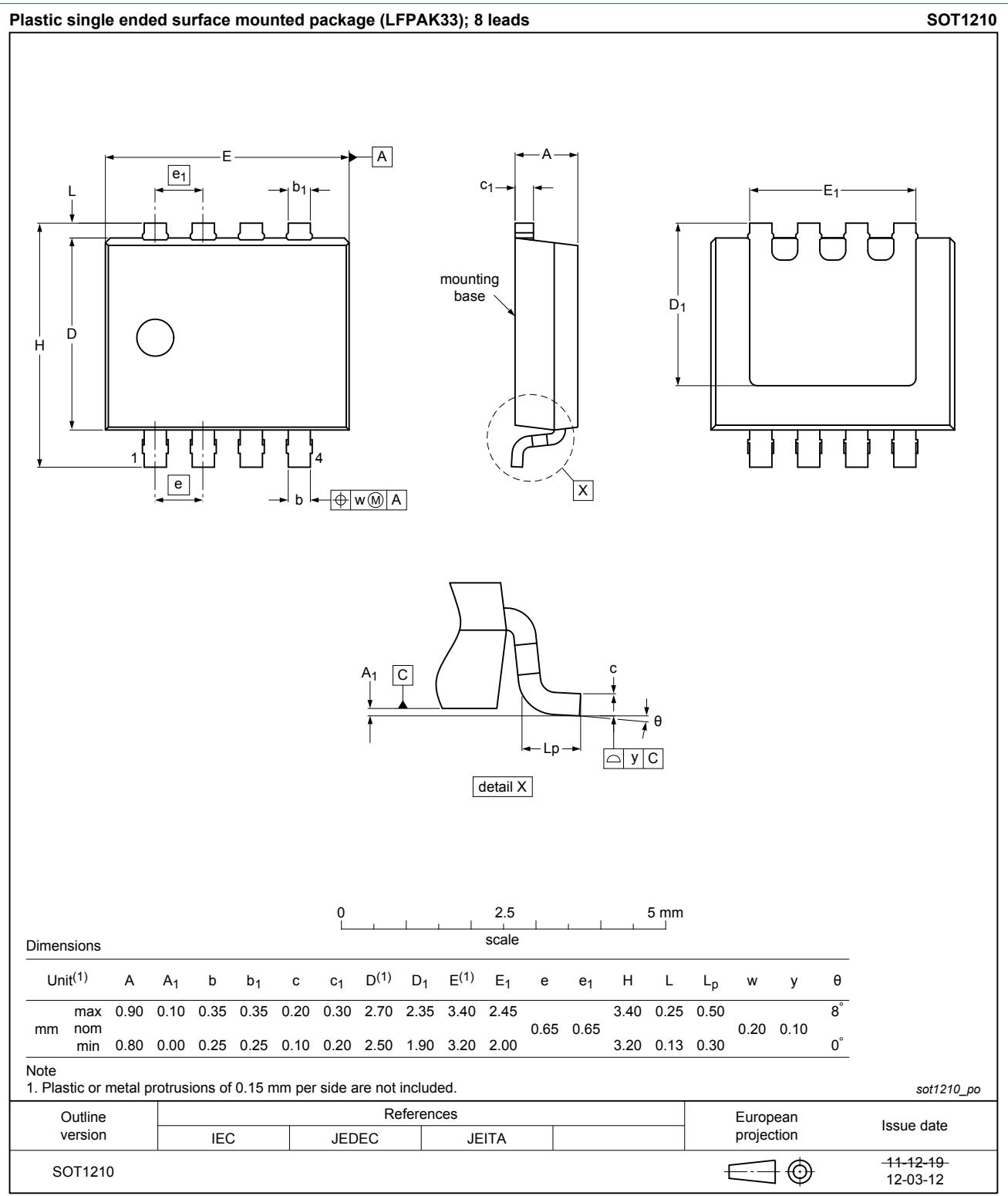


Fig. 18. Package outline LFPAK33 (SOT1210)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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13. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Quick reference data	1
5	Pinning information	2
6	Ordering information	2
7	Marking	2
8	Limiting values	2
9	Thermal characteristics	4
10	Characteristics	5
11	Package outline	10
12	Legal information	11
12.1	Data sheet status	11
12.2	Definitions	11
12.3	Disclaimers	11
12.4	Trademarks	12

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