

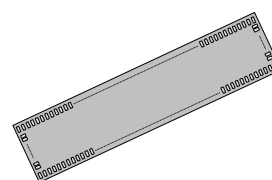
40COMMON x 128RGB LCD DRIVER FOR 4,096-COLOR STN DISPLAY

■ GENERAL DESCRIPTION

The **NJU6820** is a 40COMMON x 128RGB LCD driver for 4,096-color STN display. It contains common drivers, RGB drivers, a serial and a parallel MPU interface circuit, an internal LCD power supply, grayscale palettes and 61,440-bit display data RAM. The segment drivers for RGB (Red, Green, Blue) independently produce optimum 16 grayscales from a built-in 32-grayscale palette, and the LSI achieves 4,096 colors (16x16x16).

In addition, the **NJU6820** operates with a low voltage of 1.7V and a low operating current, therefore it is ideally suited for battery-powered handheld applications.

■ PACKAGE



BUMP CHIP

■ FEATURES

- 4,096-color STN LCD driver
- Built-in LCD Drivers : 40 common Drivers x 128RGB Drivers (384-segment Drivers in B&W)
- Built-in Display Data RAM (DDRAM) : 61,440 bits for Graphic Display
- Programmable Display Mode
 - Variable 16-grayscale Mode : 4,096 Colors
 - Variable 8-grayscale Mode : 256 Colors
 - Fixed 8-grayscale Mode : 256 Colors
 - B&W Mode : Black & White
- 8-/16-bit Parallel Interface Selectable
- 8-/16-bit Bus Length for Display Data Selectable
- 3-/4-line Serial Interface Selectable
- Programmable Duty Ratio and Bias Ratio
- Programmable Internal Voltage Booster : Maximum 5 times
- Programmable Contrast Control : 128-step Electrical Variable Resistor (EVR)
- Various Useful Instructions
- Low Operating Current : 450uA Typical at $V_{DD}=3V$, 4-time Boost, Checker Flag Display
- Low Logic Voltage : 1.7V to 3.3V
- Wide LCD Voltage Range : 5.0V to 18.0V
- C-MOS Technology
- Slim Chip for COG
- Package : Bump Chip / TCP

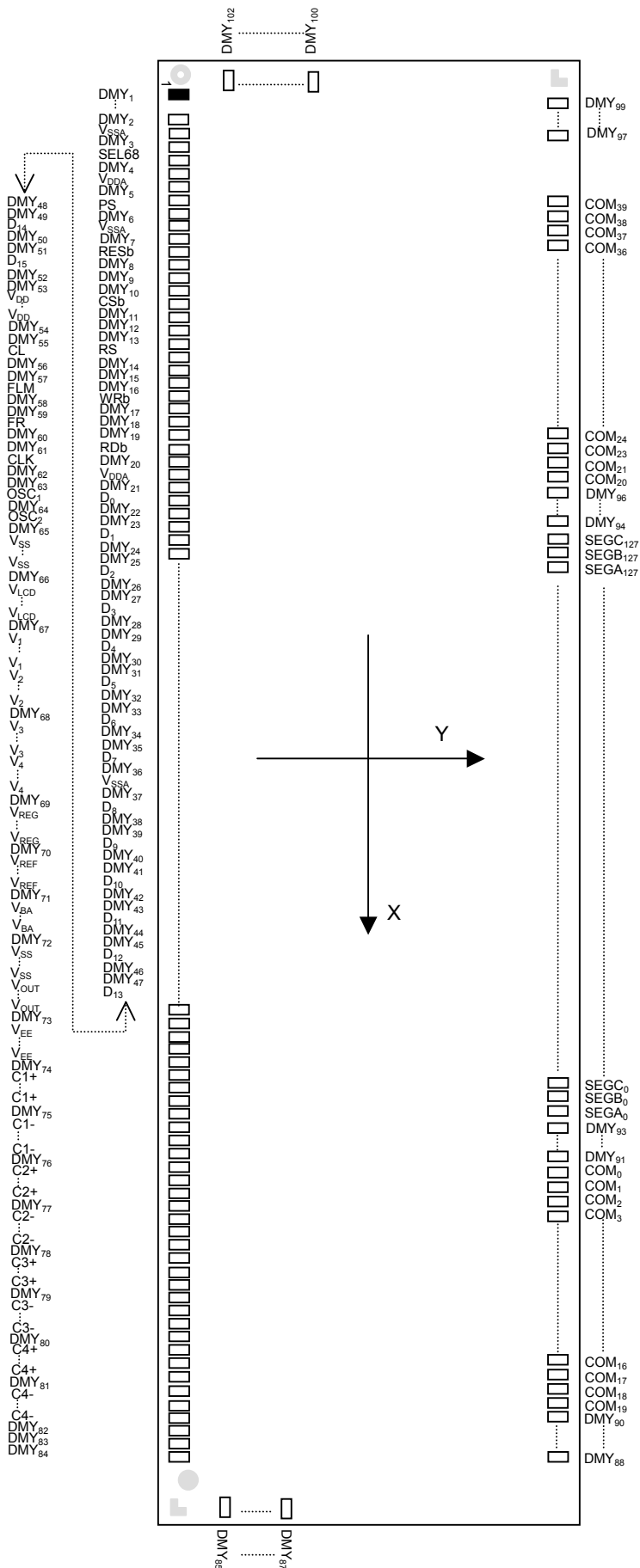
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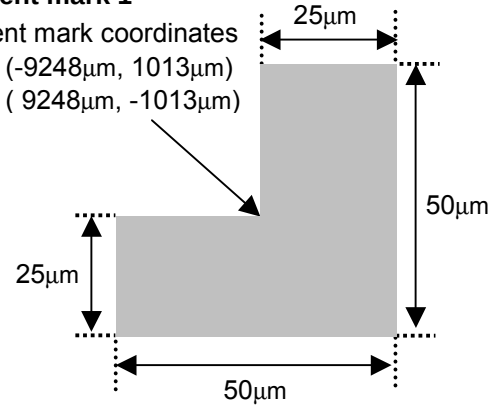
PAD LOCATION



Alignment mark 1

Alignment mark coordinates

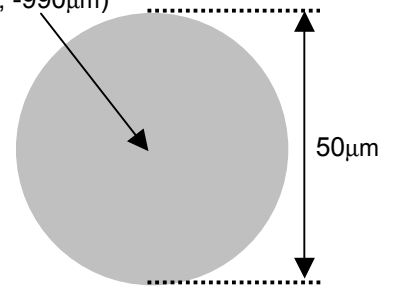
(-9248 μ m, 1013 μ m)
(9248 μ m, -1013 μ m)



Alignment mark 2

Alignment mark coordinates

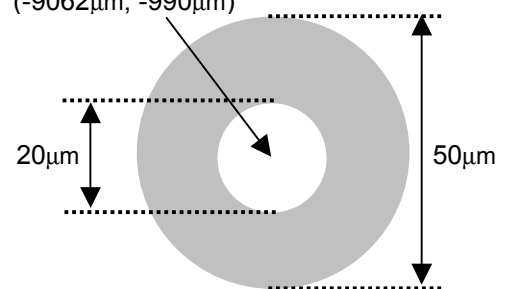
(9062 μ m, -990 μ m)



Alignment mark 3

Alignment mark coordinates

(-9062 μ m, -990 μ m)



Chip Center	:X=0 μ m, Y=0 μ m
Chip Size	:X=18.86mm, Y= 2.39mm
Chip Thickness	:625 μ m $\pm$ 25 μ m
Bump Pitch	:42 μ m(Min)
Bump Space	:18 μ m
Bump Size	:24 μ m x 140 μ m
Bump hight	:17.5 μ m(Typ)
Bump Material	:Au

■ PAD COORDINATES 1

Chip Size 18860μm x 2390μm (Chip Center 0μm x 0μm)

No.	PAD Name	X(μm)	Y(μm)	No.	PAD Name	X(μm)	Y(μm)	No.	PAD Name	X(μm)	Y(μm)
1	DMY ₀	-8967	-990	51	DMY ₂₄	-6699	-990	101	DMY ₄₈	-3507	-990
2	DMY ₁	-8925	-990	52	DMY ₂₅	-6573	-990	102	DMY ₄₉	-3381	-990
3	DMY ₂	-8883	-990	53	D ₂	-6531	-990	103	D ₁₄	-3339	-990
4	V _{SSA}	-8841	-990	54	D ₂	-6489	-990	104	D ₁₄	-3297	-990
5	V _{SSA}	-8799	-990	55	DMY ₂₆	-6447	-990	105	DMY ₅₀	-3255	-990
6	DMY ₃	-8757	-990	56	DMY ₂₇	-6321	-990	106	DMY ₅₁	-3129	-990
7	SEL68	-8715	-990	57	D ₃	-6279	-990	107	D ₁₅	-3087	-990
8	SEL68	-8673	-990	58	D ₃	-6237	-990	108	D ₁₅	-3045	-990
9	DMY ₄	-8631	-990	59	DMY ₂₈	-6195	-990	109	DMY ₅₂	-3003	-990
10	V _{DDA}	-8589	-990	60	DMY ₂₉	-6069	-990	110	DMY ₅₃	-2877	-990
11	V _{DDA}	-8547	-990	61	D ₄	-6027	-990	111	V _{DD}	-2835	-990
12	DMY ₅	-8505	-990	62	D ₄	-5985	-990	112	V _{DD}	-2793	-990
13	PS	-8463	-990	63	DMY ₃₀	-5943	-990	113	V _{DD}	-2751	-990
14	PS	-8421	-990	64	DMY ₃₁	-5817	-990	114	V _{DD}	-2709	-990
15	DMY ₆	-8379	-990	65	D ₅	-5775	-990	115	V _{DD}	-2667	-990
16	V _{SSA}	-8337	-990	66	D ₅	-5733	-990	116	V _{DD}	-2625	-990
17	V _{SSA}	-8295	-990	67	DMY ₃₂	-5691	-990	117	V _{DD}	-2583	-990
18	DMY ₇	-8253	-990	68	DMY ₃₃	-5565	-990	118	V _{DD}	-2541	-990
19	RESb	-8211	-990	69	D ₆	-5523	-990	119	V _{DD}	-2499	-990
20	RESb	-8169	-990	70	D ₆	-5481	-990	120	V _{DD}	-2457	-990
21	DMY ₈	-8127	-990	71	DMY ₃₄	-5439	-990	121	V _{DD}	-2415	-990
22	DMY ₉	-8085	-990	72	DMY ₃₅	-5313	-990	122	DMY ₅₄	-2289	-990
23	DMY ₁₀	-8043	-990	73	D ₇	-5271	-990	123	DMY ₅₅	-2163	-990
24	CSb	-8001	-990	74	D ₇	-5229	-990	124	CL	-2121	-990
25	CSb	-7959	-990	75	DMY ₃₆	-5187	-990	125	CL	-2079	-990
26	DMY ₁₁	-7917	-990	76	V _{SSA}	-5061	-990	126	DMY ₅₆	-2037	-990
27	DMY ₁₂	-7875	-990	77	V _{SSA}	-5019	-990	127	DMY ₅₇	-1911	-990
28	DMY ₁₃	-7833	-990	78	DMY ₃₇	-4893	-990	128	FLM	-1869	-990
29	RS	-7791	-990	79	D ₈	-4851	-990	129	FLM	-1827	-990
30	RS	-7749	-990	80	D ₈	-4809	-990	130	DMY ₅₈	-1785	-990
31	DMY ₁₄	-7707	-990	81	DMY ₃₈	-4767	-990	131	DMY ₅₉	-1659	-990
32	DMY ₁₅	-7665	-990	82	DMY ₃₉	-4641	-990	132	FR	-1617	-990
33	DMY ₁₆	-7623	-990	83	D ₉	-4599	-990	133	FR	-1575	-990
34	WRb	-7581	-990	84	D ₉	-4557	-990	134	DMY ₆₀	-1533	-990
35	WRb	-7539	-990	85	DMY ₄₀	-4515	-990	135	DMY ₆₁	-1407	-990
36	DMY ₁₇	-7497	-990	86	DMY ₄₁	-4389	-990	136	CLK	-1365	-990
37	DMY ₁₈	-7455	-990	87	D ₁₀	-4347	-990	137	CLK	-1323	-990
38	DMY ₁₉	-7413	-990	88	D ₁₀	-4305	-990	138	DMY ₆₂	-1281	-990
39	RDb	-7371	-990	89	DMY ₄₂	-4263	-990	139	DMY ₆₃	-1155	-990
40	RDb	-7329	-990	90	DMY ₄₃	-4137	-990	140	OSC ₁	-1113	-990
41	DMY ₂₀	-7287	-990	91	D ₁₁	-4095	-990	141	OSC ₁	-1071	-990
42	V _{DDA}	-7245	-990	92	D ₁₁	-4053	-990	142	DMY ₆₄	-1029	-990
43	V _{DDA}	-7203	-990	93	DMY ₄₄	-4011	-990	143	OSC ₂	-903	-990
44	DMY ₂₁	-7077	-990	94	DMY ₄₅	-3885	-990	144	OSC ₂	-861	-990
45	D ₀	-7035	-990	95	D ₁₂	-3843	-990	145	DMY ₆₅	-735	-990
46	D ₀	-6993	-990	96	D ₁₂	-3801	-990	146	V _{SS}	-693	-990
47	DMY ₂₂	-6951	-990	97	DMY ₄₆	-3759	-990	147	V _{SS}	-651	-990
48	DMY ₂₃	-6825	-990	98	DMY ₄₇	-3633	-990	148	V _{SS}	-609	-990
49	D ₁	-6783	-990	99	D ₁₃	-3591	-990	149	V _{SS}	-567	-990
50	D ₁	-6741	-990	100	D ₁₃	-3549	-990	150	V _{SS}	-525	-990

■ PAD COORDINATES 2

Chip Size 18860μm x 2390μm (Chip Center 0μm x 0μm)

No.	PAD Name	X(μm)	Y(μm)	No.	PAD Name	X(μm)	Y(μm)	No.	PAD Name	X(μm)	Y(μm)
151	V _{SS}	-483	-990	201	V ₄	1953	-990	251	V _{OUT}	4179	-990
152	V _{SS}	-441	-990	202	V ₄	1995	-990	252	V _{OUT}	4221	-990
153	V _{SS}	-399	-990	203	V ₄	2037	-990	253	V _{OUT}	4263	-990
154	V _{SS}	-357	-990	204	V ₄	2079	-990	254	V _{OUT}	4305	-990
155	V _{SS}	-315	-990	205	DMY ₆₉	2121	-990	255	V _{OUT}	4347	-990
156	V _{SS}	-273	-990	206	V _{REG}	2163	-990	256	V _{OUT}	4389	-990
157	DMY ₆₆	-147	-990	207	V _{REG}	2205	-990	257	V _{OUT}	4431	-990
158	V _{LCD}	-21	-990	208	V _{REG}	2247	-990	258	V _{OUT}	4473	-990
159	V _{LCD}	21	-990	209	V _{REG}	2289	-990	259	DMY ₇₃	4641	-990
160	V _{LCD}	63	-990	210	V _{REG}	2331	-990	260	V _{EE}	4683	-990
161	V _{LCD}	105	-990	211	V _{REG}	2373	-990	261	V _{EE}	4725	-990
162	V _{LCD}	147	-990	212	V _{REG}	2415	-990	262	V _{EE}	4767	-990
163	V _{LCD}	189	-990	213	V _{REG}	2457	-990	263	V _{EE}	4809	-990
164	V _{LCD}	231	-990	214	V _{REG}	2499	-990	264	V _{EE}	4851	-990
165	V _{LCD}	273	-990	215	V _{REG}	2541	-990	265	V _{EE}	4893	-990
166	V _{LCD}	315	-990	216	DMY ₇₀	2583	-990	266	V _{EE}	4935	-990
167	DMY ₆₇	357	-990	217	V _{REF}	2625	-990	267	V _{EE}	4977	-990
168	V ₁	399	-990	218	V _{REF}	2667	-990	268	V _{EE}	5019	-990
169	V ₁	441	-990	219	V _{REF}	2709	-990	269	V _{EE}	5061	-990
170	V ₁	483	-990	220	V _{REF}	2751	-990	270	DMY ₇₄	5187	-990
171	V ₁	525	-990	221	V _{REF}	2793	-990	271	C1+	5229	-990
172	V ₁	567	-990	222	V _{REF}	2835	-990	272	C1+	5271	-990
173	V ₁	609	-990	223	V _{REF}	2877	-990	273	C1+	5313	-990
174	V ₁	651	-990	224	V _{REF}	2919	-990	274	C1+	5355	-990
175	V ₁	693	-990	225	V _{REF}	2961	-990	275	C1+	5397	-990
176	V ₁	735	-990	226	V _{REF}	3003	-990	276	C1+	5439	-990
177	V ₂	861	-990	227	DMY ₇₁	3045	-990	277	C1+	5481	-990
178	V ₂	903	-990	228	V _{BA}	3087	-990	278	C1+	5523	-990
179	V ₂	945	-990	229	V _{BA}	3129	-990	279	C1+	5565	-990
180	V ₂	987	-990	230	V _{BA}	3171	-990	280	C1+	5607	-990
181	V ₂	1029	-990	231	V _{BA}	3213	-990	281	DMY ₇₅	5649	-990
182	V ₂	1071	-990	232	V _{BA}	3255	-990	282	C1-	5691	-990
183	V ₂	1113	-990	233	V _{BA}	3297	-990	283	C1-	5733	-990
184	V ₂	1155	-990	234	V _{BA}	3339	-990	284	C1-	5775	-990
185	V ₂	1197	-990	235	V _{BA}	3381	-990	285	C1-	5817	-990
186	DMY ₆₈	1239	-990	236	V _{BA}	3423	-990	286	C1-	5859	-990
187	V ₃	1281	-990	237	V _{BA}	3465	-990	287	C1-	5901	-990
188	V ₃	1323	-990	238	DMY ₇₂	3507	-990	288	C1-	5943	-990
189	V ₃	1365	-990	239	V _{SS}	3549	-990	289	C1-	5985	-990
190	V ₃	1407	-990	240	V _{SS}	3591	-990	290	C1-	6027	-990
191	V ₃	1449	-990	241	V _{SS}	3633	-990	291	C1-	6069	-990
192	V ₃	1491	-990	242	V _{SS}	3675	-990	292	DMY ₇₆	6111	-990
193	V ₃	1533	-990	243	V _{SS}	3717	-990	293	C2+	6153	-990
194	V ₃	1575	-990	244	V _{SS}	3759	-990	294	C2+	6195	-990
195	V ₃	1617	-990	245	V _{SS}	3801	-990	295	C2+	6237	-990
196	V ₄	1743	-990	246	V _{SS}	3843	-990	296	C2+	6279	-990
197	V ₄	1785	-990	247	V _{SS}	3885	-990	297	C2+	6321	-990
198	V ₄	1827	-990	248	V _{SS}	3927	-990	298	C2+	6363	-990
199	V ₄	1869	-990	249	V _{OUT}	4095	-990	299	C2+	6405	-990
200	V ₄	1911	-990	250	V _{OUT}	4137	-990	300	C2+	6447	-990

■ PAD COORDINATES 3

Chip Size 18860μm x 2390μm (Chip Center 0μm x 0μm)

No.	PAD Name	X(μm)	Y(μm)	No.	PAD Name	X(μm)	Y(μm)	No.	PAD Name	X(μm)	Y(μm)
301	C2+	6489	-990	351	C4-	8589	-990	401	SEGA ₃	7665	990
302	C2+	6531	-990	352	C4-	8631	-990	402	SEGB ₃	7623	990
303	DMY ₇₇	6573	-990	353	C4-	8673	-990	403	SEGC ₃	7581	990
304	C2-	6615	-990	354	C4-	8715	-990	404	SEGA ₄	7539	990
305	C2-	6657	-990	355	C4-	8757	-990	405	SEGB ₄	7497	990
306	C2-	6699	-990	356	C4-	8799	-990	406	SEGC ₄	7455	990
307	C2-	6741	-990	357	C4-	8841	-990	407	SEGA ₅	7413	990
308	C2-	6783	-990	358	DMY ₈₂	8883	-990	408	SEGB ₅	7371	990
309	C2-	6825	-990	359	DMY ₈₃	8925	-990	409	SEGC ₅	7329	990
310	C2-	6867	-990	360	DMY ₈₄	8967	-990	410	SEGA ₆	7287	990
311	C2-	6909	-990	361	DMY ₈₅	9225	-910	411	SEGB ₆	7245	990
312	C2-	6951	-990	362	DMY ₈₆	9225	-868	412	SEGC ₆	7203	990
313	C2-	6993	-990	363	DMY ₈₆	9225	-826	413	SEGA ₇	7161	990
314	DMY ₇₈	7035	-990	364	DMY ₈₆	9225	-784	414	SEGB ₇	7119	990
315	C3+	7077	-990	365	DMY ₈₇	9225	-742	415	SEGC ₇	7077	990
316	C3+	7119	-990	366	DMY ₈₈	9135	990	416	SEGA ₈	7035	990
317	C3+	7161	-990	367	DMY ₈₉	9093	990	417	SEGB ₈	6993	990
318	C3+	7203	-990	368	DMY ₉₀	9051	990	418	SEGC ₈	6951	990
319	C3+	7245	-990	369	COM ₁₉	9009	990	419	SEGA ₉	6909	990
320	C3+	7287	-990	370	COM ₁₈	8967	990	420	SEGB ₉	6867	990
321	C3+	7329	-990	371	COM ₁₇	8925	990	421	SEGC ₉	6825	990
322	C3+	7371	-990	372	COM ₁₆	8883	990	422	SEGA ₁₀	6783	990
323	C3+	7413	-990	373	COM ₁₅	8841	990	423	SEGB ₁₀	6741	990
324	C3+	7455	-990	374	COM ₁₄	8799	990	424	SEGC ₁₀	6699	990
325	DMY ₇₉	7497	-990	375	COM ₁₃	8757	990	425	SEGA ₁₁	6657	990
326	C3-	7539	-990	376	COM ₁₂	8715	990	426	SEGB ₁₁	6615	990
327	C3-	7581	-990	377	COM ₁₁	8673	990	427	SEGC ₁₁	6573	990
328	C3-	7623	-990	378	COM ₁₀	8631	990	428	SEGA ₁₂	6531	990
329	C3-	7665	-990	379	COM ₉	8589	990	429	SEGB ₁₂	6489	990
330	C3-	7707	-990	380	COM ₈	8547	990	430	SEGC ₁₂	6447	990
331	C3-	7749	-990	381	COM ₇	8505	990	431	SEGA ₁₃	6405	990
332	C3-	7791	-990	382	COM ₆	8463	990	432	SEGB ₁₃	6363	990
333	C3-	7833	-990	383	COM ₅	8421	990	433	SEGC ₁₃	6321	990
334	C3-	7875	-990	384	COM ₄	8379	990	434	SEGA ₁₄	6279	990
335	C3-	7917	-990	385	COM ₃	8337	990	435	SEGB ₁₄	6237	990
336	DMY ₈₀	7959	-990	386	COM ₂	8295	990	436	SEGC ₁₄	6195	990
337	C4+	8001	-990	387	COM ₁	8253	990	437	SEGA ₁₅	6153	990
338	C4+	8043	-990	388	COM ₀	8211	990	438	SEGB ₁₅	6111	990
339	C4+	8085	-990	389	DMY ₉₁	8169	990	439	SEGC ₁₅	6069	990
340	C4+	8127	-990	390	DMY ₉₂	8127	990	440	SEGA ₁₆	6027	990
341	C4+	8169	-990	391	DMY ₉₃	8085	990	441	SEGB ₁₆	5985	990
342	C4+	8211	-990	392	SEGA ₀	8043	990	442	SEGC ₁₆	5943	990
343	C4+	8253	-990	393	SEGB ₀	8001	990	443	SEGA ₁₇	5901	990
344	C4+	8295	-990	394	SEGC ₀	7959	990	444	SEGB ₁₇	5859	990
345	C4+	8337	-990	395	SEGA ₁	7917	990	445	SEGC ₁₇	5817	990
346	C4+	8379	-990	396	SEGB ₁	7875	990	446	SEGA ₁₈	5775	990
347	DMY ₈₁	8421	-990	397	SEGC ₁	7833	990	447	SEGB ₁₈	5733	990
348	C4-	8463	-990	398	SEGA ₂	7791	990	448	SEGC ₁₈	5691	990
349	C4-	8505	-990	399	SEGB ₂	7749	990	449	SEGA ₁₉	5649	990
350	C4-	8547	-990	400	SEGC ₂	7707	990	450	SEGB ₁₉	5607	990

■ PAD COORDINATES 4

Chip Size 18860μm x 2390μm (Chip Center 0μm x 0μm)

No.	PAD Name	X(μm)	Y(μm)	No.	PAD Name	X(μm)	Y(μm)	No.	PAD Name	X(μm)	Y(μm)
451	SEGC ₁₉	5565	990	501	SEGB ₃₆	3465	990	551	SEGA ₅₃	1365	990
452	SEGA ₂₀	5523	990	502	SEGC ₃₆	3423	990	552	SEGB ₅₃	1323	990
453	SEGB ₂₀	5481	990	503	SEGA ₃₇	3381	990	553	SEGC ₅₃	1281	990
454	SEGC ₂₀	5439	990	504	SEGB ₃₇	3339	990	554	SEGA ₅₄	1239	990
455	SEGA ₂₁	5397	990	505	SEGC ₃₇	3297	990	555	SEGB ₅₄	1197	990
456	SEGB ₂₁	5355	990	506	SEGA ₃₈	3255	990	556	SEGC ₅₄	1155	990
457	SEGC ₂₁	5313	990	507	SEGB ₃₈	3213	990	557	SEGA ₅₅	1113	990
458	SEGA ₂₂	5271	990	508	SEGC ₃₈	3171	990	558	SEGB ₅₅	1071	990
459	SEGB ₂₂	5229	990	509	SEGA ₃₉	3129	990	559	SEGC ₅₅	1029	990
460	SEGC ₂₂	5187	990	510	SEGB ₃₉	3087	990	560	SEGA ₅₆	987	990
461	SEGA ₂₃	5145	990	511	SEGC ₃₉	3045	990	561	SEGB ₅₆	945	990
462	SEGB ₂₃	5103	990	512	SEGA ₄₀	3003	990	562	SEGC ₅₆	903	990
463	SEGC ₂₃	5061	990	513	SEGB ₄₀	2961	990	563	SEGA ₅₇	861	990
464	SEGA ₂₄	5019	990	514	SEGC ₄₀	2919	990	564	SEGB ₅₇	819	990
465	SEGB ₂₄	4977	990	515	SEGA ₄₁	2877	990	565	SEGC ₅₇	777	990
466	SEGC ₂₄	4935	990	516	SEGB ₄₁	2835	990	566	SEGA ₅₈	735	990
467	SEGA ₂₅	4893	990	517	SEGC ₄₁	2793	990	567	SEGB ₅₈	693	990
468	SEGB ₂₅	4851	990	518	SEGA ₄₂	2751	990	568	SEGC ₅₈	651	990
469	SEGC ₂₅	4809	990	519	SEGB ₄₂	2709	990	569	SEGA ₅₉	609	990
470	SEGA ₂₆	4767	990	520	SEGC ₄₂	2667	990	570	SEGB ₅₉	567	990
471	SEGB ₂₆	4725	990	521	SEGA ₄₃	2625	990	571	SEGC ₅₉	525	990
472	SEGC ₂₆	4683	990	522	SEGB ₄₃	2583	990	572	SEGA ₆₀	483	990
473	SEGA ₂₇	4641	990	523	SEGC ₄₃	2541	990	573	SEGB ₆₀	441	990
474	SEGB ₂₇	4599	990	524	SEGA ₄₄	2499	990	574	SEGC ₆₀	399	990
475	SEGC ₂₇	4557	990	525	SEGB ₄₄	2457	990	575	SEGA ₆₁	357	990
476	SEGA ₂₈	4515	990	526	SEGC ₄₄	2415	990	576	SEGB ₆₁	315	990
477	SEGB ₂₈	4473	990	527	SEGA ₄₅	2373	990	577	SEGC ₆₁	273	990
478	SEGC ₂₈	4431	990	528	SEGB ₄₅	2331	990	578	SEGA ₆₂	231	990
479	SEGA ₂₉	4389	990	529	SEGC ₄₅	2289	990	579	SEGB ₆₂	189	990
480	SEGB ₂₉	4347	990	530	SEGA ₄₆	2247	990	580	SEGC ₆₂	147	990
481	SEGC ₂₉	4305	990	531	SEGB ₄₆	2205	990	581	SEGA ₆₃	105	990
482	SEGA ₃₀	4263	990	532	SEGC ₄₆	2163	990	582	SEGB ₆₃	63	990
483	SEGB ₃₀	4221	990	533	SEGA ₄₇	2121	990	583	SEGC ₆₃	21	990
484	SEGC ₃₀	4179	990	534	SEGB ₄₇	2079	990	584	SEGA ₆₄	-21	990
485	SEGA ₃₁	4137	990	535	SEGC ₄₇	2037	990	585	SEGB ₆₄	-63	990
486	SEGB ₃₁	4095	990	536	SEGA ₄₈	1995	990	586	SEGC ₆₄	-105	990
487	SEGC ₃₁	4053	990	537	SEGB ₄₈	1953	990	587	SEGA ₆₅	-147	990
488	SEGA ₃₂	4011	990	538	SEGC ₄₈	1911	990	588	SEGB ₆₅	-189	990
489	SEGB ₃₂	3969	990	539	SEGA ₄₉	1869	990	589	SEGC ₆₅	-231	990
490	SEGC ₃₂	3927	990	540	SEGB ₄₉	1827	990	590	SEGA ₆₆	-273	990
491	SEGA ₃₃	3885	990	541	SEGC ₄₉	1785	990	591	SEGB ₆₆	-315	990
492	SEGB ₃₃	3843	990	542	SEGA ₅₀	1743	990	592	SEGC ₆₆	-357	990
493	SEGC ₃₃	3801	990	543	SEGB ₅₀	1701	990	593	SEGA ₆₇	-399	990
494	SEGA ₃₄	3759	990	544	SEGC ₅₀	1659	990	594	SEGB ₆₇	-441	990
495	SEGB ₃₄	3717	990	545	SEGA ₅₁	1617	990	595	SEGC ₆₇	-483	990
496	SEGC ₃₄	3675	990	546	SEGB ₅₁	1575	990	596	SEGA ₆₈	-525	990
497	SEGA ₃₅	3633	990	547	SEGC ₅₁	1533	990	597	SEGB ₆₈	-567	990
498	SEGB ₃₅	3591	990	548	SEGA ₅₂	1491	990	598	SEGC ₆₈	-609	990
499	SEGC ₃₅	3549	990	549	SEGB ₅₂	1449	990	599	SEGA ₆₉	-651	990
500	SEGA ₃₆	3507	990	550	SEGC ₅₂	1407	990	600	SEGB ₆₉	-693	990

■ PAD COORDINATES 5

Chip Size 18860μm x 2390μm (Chip Center 0μm x 0μm)

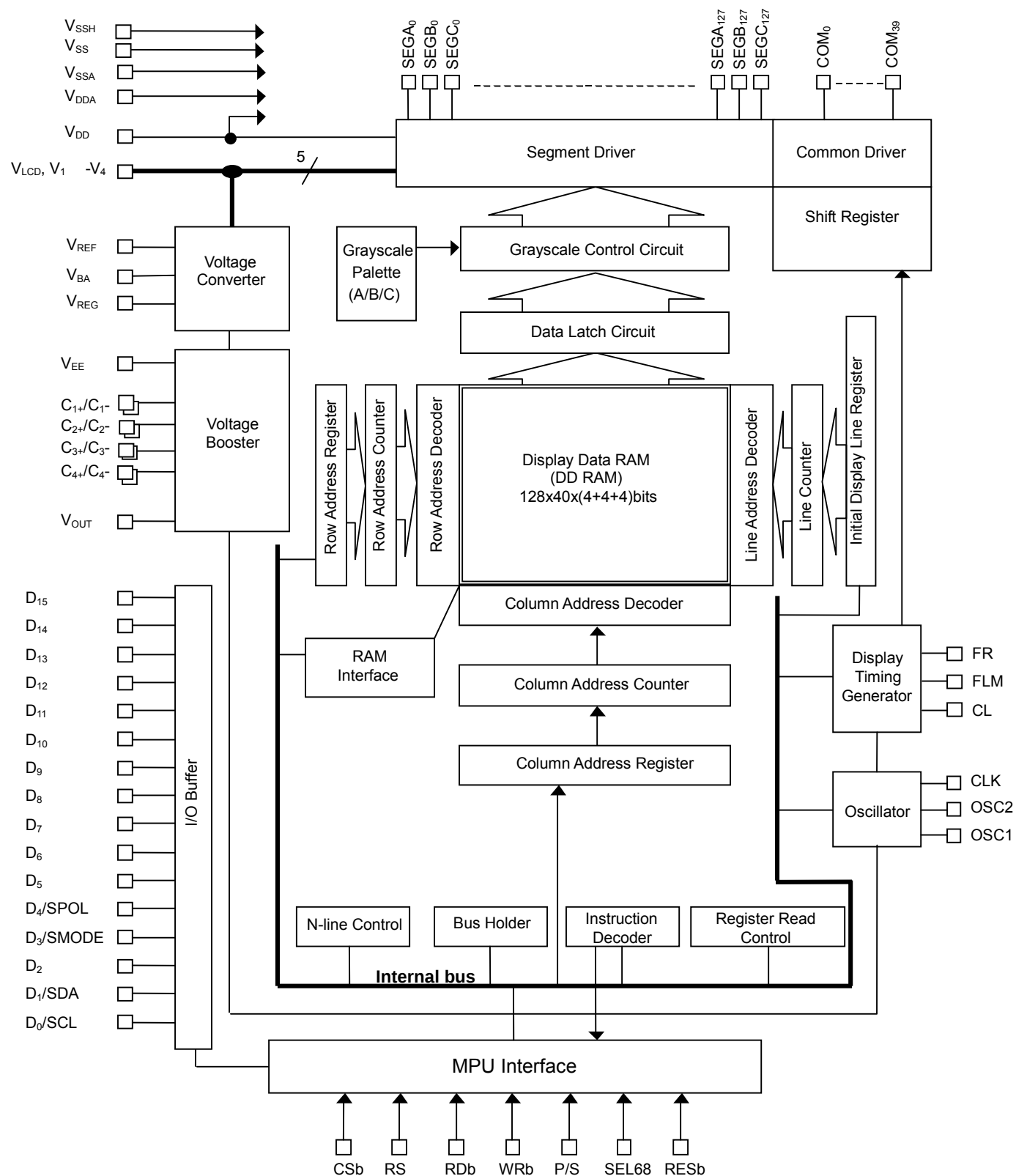
No.	PAD Name	X(μm)	Y(μm)	No.	PAD Name	X(μm)	Y(μm)	No.	PAD Name	X(μm)	Y(μm)
601	SEGC ₆₉	-735	990	651	SEGB ₈₆	-2835	990	701	SEGA ₁₀₃	-4935	990
602	SEGA ₇₀	-777	990	652	SEGC ₈₆	-2877	990	702	SEGB ₁₀₃	-4977	990
603	SEGB ₇₀	-819	990	653	SEGA ₈₇	-2919	990	703	SEGC ₁₀₃	-5019	990
604	SEGC ₇₀	-861	990	654	SEGB ₈₇	-2961	990	704	SEGA ₁₀₄	-5061	990
605	SEGA ₇₁	-903	990	655	SEGC ₈₇	-3003	990	705	SEGB ₁₀₄	-5103	990
606	SEGB ₇₁	-945	990	656	SEGA ₈₈	-3045	990	706	SEGC ₁₀₄	-5145	990
607	SEGC ₇₁	-987	990	657	SEGB ₈₈	-3087	990	707	SEGA ₁₀₅	-5187	990
608	SEGA ₇₂	-1029	990	658	SEGC ₈₈	-3129	990	708	SEGB ₁₀₅	-5229	990
609	SEGB ₇₂	-1071	990	659	SEGA ₈₉	-3171	990	709	SEGC ₁₀₅	-5271	990
610	SEGC ₇₂	-1113	990	660	SEGB ₈₉	-3213	990	710	SEGA ₁₀₆	-5313	990
611	SEGA ₇₃	-1155	990	661	SEGC ₈₉	-3255	990	711	SEGB ₁₀₆	-5355	990
612	SEGB ₇₃	-1197	990	662	SEGA ₉₀	-3297	990	712	SEGC ₁₀₆	-5397	990
613	SEGC ₇₃	-1239	990	663	SEGB ₉₀	-3339	990	713	SEGA ₁₀₇	-5439	990
614	SEGA ₇₄	-1281	990	664	SEGC ₉₀	-3381	990	714	SEGB ₁₀₇	-5481	990
615	SEGB ₇₄	-1323	990	665	SEGA ₉₁	-3423	990	715	SEGC ₁₀₇	-5523	990
616	SEGC ₇₄	-1365	990	666	SEGB ₉₁	-3465	990	716	SEGA ₁₀₈	-5565	990
617	SEGA ₇₅	-1407	990	667	SEGC ₉₁	-3507	990	717	SEGB ₁₀₈	-5607	990
618	SEGB ₇₅	-1449	990	668	SEGA ₉₂	-3549	990	718	SEGC ₁₀₈	-5649	990
619	SEGC ₇₅	-1491	990	669	SEGB ₉₂	-3591	990	719	SEGA ₁₀₉	-5691	990
620	SEGA ₇₆	-1533	990	670	SEGC ₉₂	-3633	990	720	SEGB ₁₀₉	-5733	990
621	SEGB ₇₆	-1575	990	671	SEGA ₉₃	-3675	990	721	SEGC ₁₀₉	-5775	990
622	SEGC ₇₆	-1617	990	672	SEGB ₉₃	-3717	990	722	SEGA ₁₁₀	-5817	990
623	SEGA ₇₇	-1659	990	673	SEGC ₉₃	-3759	990	723	SEGB ₁₁₀	-5859	990
624	SEGB ₇₇	-1701	990	674	SEGA ₉₄	-3801	990	724	SEGC ₁₁₀	-5901	990
625	SEGC ₇₇	-1743	990	675	SEGB ₉₄	-3843	990	725	SEGA ₁₁₁	-5943	990
626	SEGA ₇₈	-1785	990	676	SEGC ₉₄	-3885	990	726	SEGB ₁₁₁	-5985	990
627	SEGB ₇₈	-1827	990	677	SEGA ₉₅	-3927	990	727	SEGC ₁₁₁	-6027	990
628	SEGC ₇₈	-1869	990	678	SEGB ₉₅	-3969	990	728	SEGA ₁₁₂	-6069	990
629	SEGA ₇₉	-1911	990	679	SEGC ₉₅	-4011	990	729	SEGB ₁₁₂	-6111	990
630	SEGB ₇₉	-1953	990	680	SEGA ₉₆	-4053	990	730	SEGC ₁₁₂	-6153	990
631	SEGC ₇₉	-1995	990	681	SEGB ₉₆	-4095	990	731	SEGA ₁₁₃	-6195	990
632	SEGA ₈₀	-2037	990	682	SEGC ₉₆	-4137	990	732	SEGB ₁₁₃	-6237	990
633	SEGB ₈₀	-2079	990	683	SEGA ₉₇	-4179	990	733	SEGC ₁₁₃	-6279	990
634	SEGC ₈₀	-2121	990	684	SEGB ₉₇	-4221	990	734	SEGA ₁₁₄	-6321	990
635	SEGA ₈₁	-2163	990	685	SEGC ₉₇	-4263	990	735	SEGB ₁₁₄	-6363	990
636	SEGB ₈₁	-2205	990	686	SEGA ₉₈	-4305	990	736	SEGC ₁₁₄	-6405	990
637	SEGC ₈₁	-2247	990	687	SEGB ₉₈	-4347	990	737	SEGA ₁₁₅	-6447	990
638	SEGA ₈₂	-2289	990	688	SEGC ₉₈	-4389	990	738	SEGB ₁₁₅	-6489	990
639	SEGB ₈₂	-2331	990	689	SEGA ₉₉	-4431	990	739	SEGC ₁₁₅	-6531	990
640	SEGC ₈₂	-2373	990	690	SEGB ₉₉	-4473	990	740	SEGA ₁₁₆	-6573	990
641	SEGA ₈₃	-2415	990	691	SEGC ₉₉	-4515	990	741	SEGB ₁₁₆	-6615	990
642	SEGB ₈₃	-2457	990	692	SEGA ₁₀₀	-4557	990	742	SEGC ₁₁₆	-6657	990
643	SEGC ₈₃	-2499	990	693	SEGB ₁₀₀	-4599	990	743	SEGA ₁₁₇	-6699	990
644	SEGA ₈₄	-2541	990	694	SEGC ₁₀₀	-4641	990	744	SEGB ₁₁₇	-6741	990
645	SEGB ₈₄	-2583	990	695	SEGA ₁₀₁	-4683	990	745	SEGC ₁₁₇	-6783	990
646	SEGC ₈₄	-2625	990	696	SEGB ₁₀₁	-4725	990	746	SEGA ₁₁₈	-6825	990
647	SEGA ₈₅	-2667	990	697	SEGC ₁₀₁	-4767	990	747	SEGB ₁₁₈	-6867	990
648	SEGB ₈₅	-2709	990	698	SEGA ₁₀₂	-4809	990	748	SEGC ₁₁₈	-6909	990
649	SEGC ₈₅	-2751	990	699	SEGB ₁₀₂	-4851	990	749	SEGA ₁₁₉	-6951	990
650	SEGA ₈₆	-2793	990	700	SEGC ₁₀₂	-4893	990	750	SEGB ₁₁₉	-6993	990

■ PAD COORDINATES 6

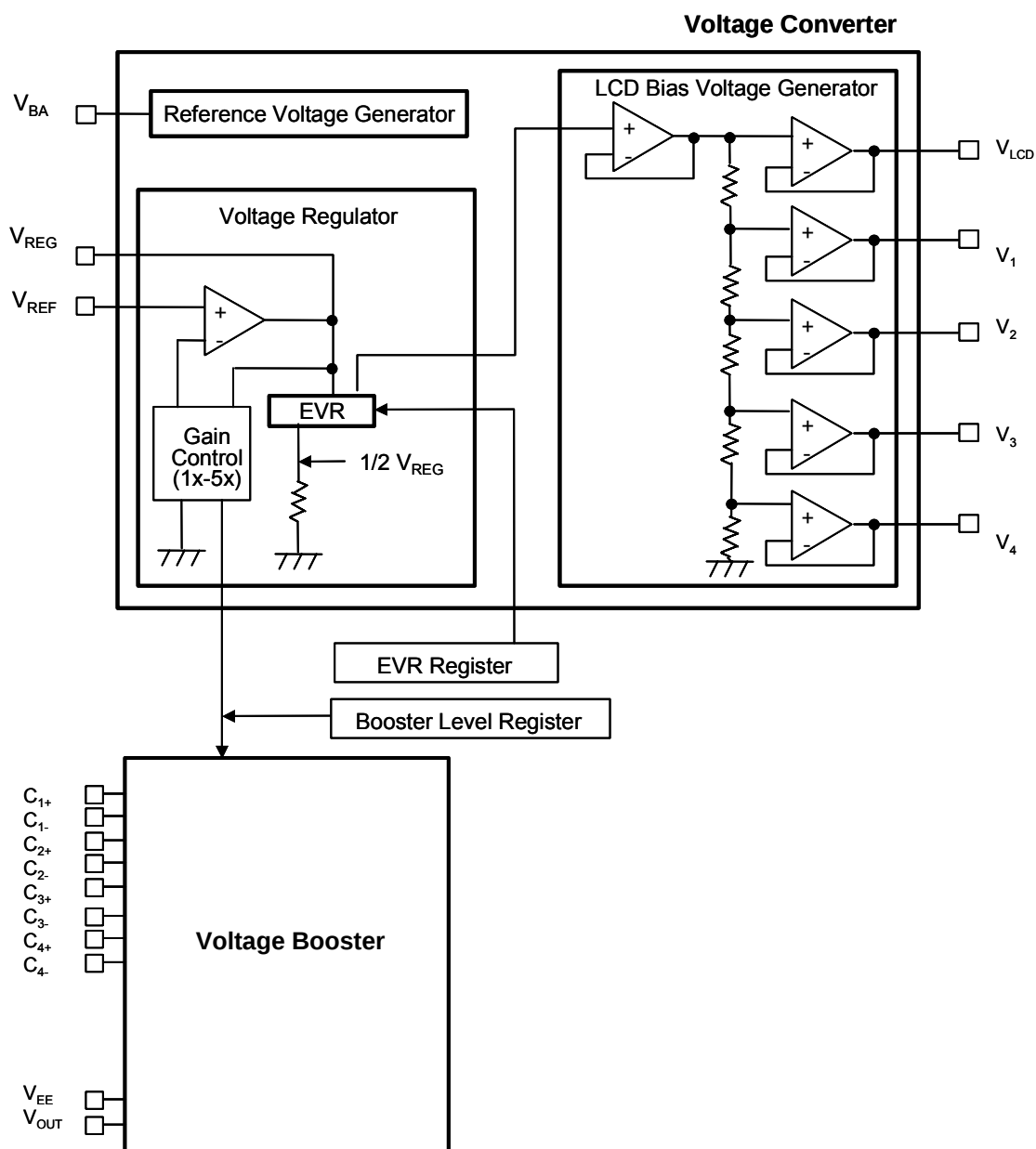
Chip Size 18860μm x 2390μm (Chip Center 0μm x 0μm)

No.	PAD Name	X(μm)	Y(μm)	No.	PAD Name	X(μm)	Y(μm)	No.	PAD Name	X(μm)	Y(μm)
751	SEGC ₁₁₉	-7035	990	801	DMY ₉₉	-9135	990				
752	SEGA ₁₂₀	-7077	990	802	DMY ₁₀₀	-9225	-742				
753	SEGB ₁₂₀	-7119	990	803	DMY ₁₀₁	-9225	-784				
754	SEGC ₁₂₀	-7161	990	804	DMY ₁₀₁	-9225	-826				
755	SEGA ₁₂₁	-7203	990	805	DMY ₁₀₁	-9225	-868				
756	SEGB ₁₂₁	-7245	990	806	DMY ₁₀₂	-9225	-910				
757	SEGC ₁₂₁	-7287	990								
758	SEGA ₁₂₂	-7329	990								
759	SEGB ₁₂₂	-7371	990								
760	SEGC ₁₂₂	-7413	990								
761	SEGA ₁₂₃	-7455	990								
762	SEGB ₁₂₃	-7497	990								
763	SEGC ₁₂₃	-7539	990								
764	SEGA ₁₂₄	-7581	990								
765	SEGB ₁₂₄	-7623	990								
766	SEGC ₁₂₄	-7665	990								
767	SEGA ₁₂₅	-7707	990								
768	SEGB ₁₂₅	-7749	990								
769	SEGC ₁₂₅	-7791	990								
770	SEGA ₁₂₆	-7833	990								
771	SEGB ₁₂₆	-7875	990								
772	SEGC ₁₂₆	-7917	990								
773	SEGA ₁₂₇	-7959	990								
774	SEGB ₁₂₇	-8001	990								
775	SEGC ₁₂₇	-8043	990								
776	DMY ₉₄	-8085	990								
777	DMY ₉₅	-8127	990								
778	DMY ₉₆	-8169	990								
779	COM ₂₀	-8211	990								
780	COM ₂₁	-8253	990								
781	COM ₂₂	-8295	990								
782	COM ₂₃	-8337	990								
783	COM ₂₄	-8379	990								
784	COM ₂₅	-8421	990								
785	COM ₂₆	-8463	990								
786	COM ₂₇	-8505	990								
787	COM ₂₈	-8547	990								
788	COM ₂₉	-8589	990								
789	COM ₃₀	-8631	990								
790	COM ₃₁	-8673	990								
791	COM ₃₂	-8715	990								
792	COM ₃₃	-8757	990								
793	COM ₃₄	-8799	990								
794	COM ₃₅	-8841	990								
795	COM ₃₆	-8883	990								
796	COM ₃₇	-8925	990								
797	COM ₃₈	-8967	990								
798	COM ₃₉	-9009	990								
799	DMY ₉₇	-9051	990								
800	DMY ₉₈	-9093	990								

■ BLOCK DIAGRAM



■ LCD POWER SUPPLY BLOCK DIAGRAM



■ TERMINAL DESCRIPTION 1

No.	Terminal	I/O	Function						
111-121	V _{DD}	Power	Power Supply for Logic Circuits						
146-156	V _{SS}	Power	GND for Logic Circuits						
239-248	V _{SSH}	Power	GND for High Voltage Circuits						
10,11, 42,43,	V _{DDA}	Power	V _{DDA} is internally connected to V _{DD} to fix SEL68 or P/S to “H” if necessary, and cannot be used as main power supply. • V _{DDA} should be open if not used.						
4,5, 16,17, 76,77,	V _{SSA}	Power	V _{SSA} is internally connected to V _{SS} to fix SEL68 or P/S to “L” if necessary, and cannot be used as main GND. • V _{SSA} should be open if not used.						
158-166 168-176 177-185 187-195 196-204	V _{LCD} V ₁ V ₂ V ₃ V ₄	Power	LCD Bias Voltages • When the internal LCD power supply is used, internal LCD bias voltages (V _{LCD} and V ₁ -V ₄) are activated by the “Power Control” instruction. Stabilizing capacitors are required between each bias voltage and V _{SS} . • When the external LCD power supply is used, LCD bias voltages are externally supplied on V _{LCD} , V ₁ , V ₂ , V ₃ and V ₄ individually, with the following relation maintained: V _{SSH} <V ₄ <V ₃ <V ₂ <V ₁ <V _{LCD}						
271-280 282-291	C ₁₊ C ₁₋	Power	Capacitor Connection for Voltage Booster						
293-302 304-313	C ₂₊ C ₂₋	Power	Capacitor Connection for Voltage Booster						
315-324 326-335	C ₃₊ C ₃₋	Power	Capacitor Connection for Voltage Booster						
337-346 348-357	C ₄₊ C ₄₋	Power	Capacitor Connection for Voltage Booster						
228-237	V _{BA}	Power	Reference-Voltage Generator Output						
217-226	V _{REF}	Power	Voltage Regulator Input						
260-269	V _{EE}	Power	Voltage Booster Input • V _{EE} is normally connected to V _{DD} .						
249-258	V _{OUT}	Power	Voltage Booster Output • Input if an external LCD power supply is used.						
19,20	RESb	I	Reset • Active “L”						
206-215	V _{REG}	Power	Voltage Regulator Output						
7,8	SEL68	I	MPU Mode Select <table><tr><td>SEL86</td><td>H</td><td>L</td></tr><tr><td>MPU</td><td>68-series</td><td>80-series</td></tr></table>	SEL86	H	L	MPU	68-series	80-series
SEL86	H	L							
MPU	68-series	80-series							

■ TERMINAL DESCRIPTION 2

No.	Terminal	I/O	Function						
45,46	D ₀ /SCL	I/O	<u>Parallel Interface</u> D ₇ to D ₀ : 8-bit Bi-directional Bus • In the parallel interface mode (P/S="H"), D ₇ -D ₀ are connected to 8-bit bi-directional MPU bus. <u>Serial Interface</u> SDA : Serial Data SCL : Serial Clock SMODE : 3-/4-line Serial Mode Select SPOL : RS Polarity Select (3-line Serial Interface Mode) • In the 3 or 4-line serial interface mode (P/S="L"), D ₀ is assigned to SCL, and D ₁ to SDA. • In the 3-line serial interface mode, D ₄ is assigned to SPOL. • Serial data on SDA is latched at the rising edge of SCL signal in order of D ₇ , D ₆ ,... and D ₀ , and then converted into 8-bit parallel data at the timing of the internal signal produced from the 8 th SCL. • SCL should be set to "L" right after data transmission or during non-access.						
49,50	D ₁ /SDA	I/O							
57,58	D ₃ /SMODE	I/O							
61,62	D ₄ /SPOL	I/O							
53,54 65,66 69,70 73,74	D ₂ D ₅ D ₆ D ₇	I/O							
79,80 83,84 87,88 91,92 95,96 99,100 103,104 107,108	D ₈ D ₉ D ₁₀ D ₁₁ D ₁₂ D ₁₃ D ₁₄ D ₁₅	I/O	8-bit Bi-directional Bus • In the 16-bit bus length mode, D ₁₅ -D ₈ are assigned to upper 8-bit data bus. • In the serial interface mode or the 8-bit parallel interface mode, D ₁₅ -D ₈ should be fixed to "H" or "L".						
24,25	CSb	I	Chip Select • Active "L"						
29,30	RS	I	Register Select • This signal interprets transferred data as display data or instruction. <table><tr><td>RS</td><td>H</td><td>L</td></tr><tr><td>Data</td><td>Instruction</td><td>Display Data</td></tr></table>	RS	H	L	Data	Instruction	Display Data
RS	H	L							
Data	Instruction	Display Data							
39,40	RDb (E)	I	<u>80-series MPU Interface (P/S="H", SEL68="L")</u> Data Read (RDb) Signal • Active "L" <u>68-series MPU Interface (P/S="H", SEL68="H")</u> Enable Signal • Active "H"						
34,35	WRb (R/W)	I	<u>80-series MPU Interface (P/S="H", SEL68="L")</u> Data Write (WRb) Signal • Active "L" <u>68-series MPU Interface (P/S="H", SEL68="H")</u> Data Read or Write (R/W) Signal <table><tr><td>R/W</td><td>H</td><td>L</td></tr><tr><td>Status</td><td>Read</td><td>Write</td></tr></table>	R/W	H	L	Status	Read	Write
R/W	H	L							
Status	Read	Write							

■ TERMINAL DESCRIPTION 3

No.	Terminal	I/O	Function																		
13,14	P/S	I	Parallel/Serial Interface Mode Select																		
			<table><tr><th>P/S</th><th>Chip Select</th><th>Display / Instruction</th><th>Data</th><th>Read /Write</th><th>Serial Clock</th></tr><tr><td>H</td><td>CSb</td><td>RS</td><td>D₀ ~ D₇</td><td>RDb, WRb</td><td>-</td></tr><tr><td>L</td><td>CSb</td><td>RS</td><td>SDA (D₁)</td><td>Write Only</td><td>SCL (D₀)</td></tr></table>	P/S	Chip Select	Display / Instruction	Data	Read /Write	Serial Clock	H	CSb	RS	D ₀ ~ D ₇	RDb, WRb	-	L	CSb	RS	SDA (D ₁)	Write Only	SCL (D ₀)
			P/S	Chip Select	Display / Instruction	Data	Read /Write	Serial Clock													
			H	CSb	RS	D ₀ ~ D ₇	RDb, WRb	-													
L	CSb	RS	SDA (D ₁)	Write Only	SCL (D ₀)																
• In the serial interface mode (P/S="L"), RDb, WRb, D ₂ and D ₅ -D ₁₅ should be fixed to "H" or "L".																					
124,125	CL	O	Line Clock																		
128,129	FLM	O	First Line Maker																		
			• FLM is normally open.																		
132,133	FR	O	Frame Rate																		
			• FR is normally open.																		
136,137	CLK	O	Clock Output																		
			• CLK is normally open.																		
140,141 143,144	OSC1 OSC2	I	OSC																		
		O	• When the internal oscillator is used, fix OSC1 to "H" or "L" and leave OSC2 open. To attain more accurate frequency, connect OSC1 and OSC2 with an external resistor. • When the internal oscillator is not used, input external clock to OSC1 and leave OSC2 open.																		
392-775	SEGA ₀ ~SEGA ₁₂₇ SEGB ₀ ~SEGB ₁₂₇ SEGC ₀ ~SEGC ₁₂₇	O	Segment Drivers																		
			<table><tr><th>REV Register</th><th>OFF</th><th>ON</th></tr><tr><td>Normal</td><td>0</td><td>1</td></tr><tr><td>Reverse</td><td>1</td><td>0</td></tr></table>	REV Register	OFF	ON	Normal	0	1	Reverse	1	0									
			REV Register	OFF	ON																
			Normal	0	1																
Reverse	1	0																			
• Segment drivers output the following voltage levels.																					
B/W Mode (Example)																					
			FR Signal Display Data Reverse Display OFF (Normal) Reverse Display ON V₂, V_{LCD}, V₃, V_{SSH}																		
369-388, 779-798,	COM ₀ ~ COM ₄₀	O	Common Drivers																		
			• Common drivers output the following voltage levels.																		
			<table><tr><th>Data</th><th>FR</th><th>Output Levels</th></tr><tr><td>H</td><td>H</td><td>V_{SSH}</td></tr><tr><td>L</td><td>H</td><td>V₁</td></tr><tr><td>H</td><td>L</td><td>V_{LCD}</td></tr><tr><td>L</td><td>L</td><td>V₄</td></tr></table>	Data	FR	Output Levels	H	H	V _{SSH}	L	H	V ₁	H	L	V _{LCD}	L	L	V ₄			
			Data	FR	Output Levels																
H	H	V _{SSH}																			
L	H	V ₁																			
H	L	V _{LCD}																			
L	L	V ₄																			

(NOTE) DUMMY PADs: No. 1-3, 12, 18, 21-23, 26-28, 31-33, 36-38, 41, 47, 48, 51, 52, 55, 56, 59, 60, 63, 64, 67, 68, 71, 72, 75, 81, 82, 85, 86, 89, 90, 93, 94, 97, 98, 101, 102, 105, 106, 109, 110, 122, 123, 126, 127, 130, 131, 134, 135, 138, 139, 142, 145, 157, 167, 186, 205, 216, 227, 238, 259, 270, 281, 292, 314, 325, 336, 347, 358-368, 389-391, 776-778, 799-806.

■ FUNCTIONAL DESCRIPTION

(1) MPU INTERFACE

(1-1) Selection of Parallel/Serial Interface Mode

The P/S selects a parallel or a serial interface mode, as shown in Table 1. In the serial interface mode, neither display data in the DDRAM nor instruction data in the registers can be read out.

Table 1 Selection of Parallel/Serial Interface Mode

P/S	I/F Mode	CSb	RS	RDb	WRb	SEL68	SDA	SCL	Data
H	Parallel I/F	CSb	RS	RDb	WRb	SEL68			D ₇ -D ₀ (D ₁₅ -D ₀)
L	Serial I/F	CSb	RS	-	-	-	SDA	SCL	-

NOTE) “-” : Fix to “H” or “L”.

(1-2) Selection of MPU Mode

In the parallel interface mode, the SEL68 selects 68 or 80-series MPU mode, as shown in Table 2.

Table 2 Selection of MPU Mode

SEL68	MPU Mode	CSb	RS	RDb	WRb	Data
H	68-series MPU	CSb	RS	E	R/W	D ₇ -D ₀ (D ₁₅ -D ₀)
L	80-series MPU	CSb	RS	RDb	WRb	D ₇ -D ₀ (D ₁₅ -D ₀)

(1-3) Data Recognition

In the parallel interface mode, the data from MPU is interpreted as display data or instruction according to the combination of the RS, RDb and WRb (R/W) signals, as shown in Table 3.

Table 3 Data Recognition (Parallel Interface Mode)

RS	68-series	80-series		Function
	R/W	RDb	WRb	
H	H	L	H	Read Instruction
H	L	H	L	Write Instruction
L	H	L	H	Read Display Data
L	L	H	L	Write Display Data

(1-4) Selection of 3-/4-line Serial Interface Mode

In the serial interface mode, the SMODE selects 3- or 4-line serial interface mode, as shown in Table 4.

Table 4 Selection of 3-/4-line Serial Interface Mode

SMODE	Serial Interface Mode
H	3-line
L	4-line

(1-5) 4-line Serial Interface Mode

While the chip select is active (CSb=“L”), the SDA and SCL are enabled. While the chip select is inactive (CSb=“H”), the SDA and SCL are disabled, and the internal shift register and the internal counter are being initialized. 8-bit serial data on the SDA is latched at the rising edge of the SCL signal in order of D₇, D₆,..., and D₀, and converted into 8-bit parallel data at the timing of the internal signal produced from the 8th SCL signal. The data on the SDA is interpreted as display data or instruction according to the RS.

Table 5 Data Recognition (4-line Serial Interface)

RS	Data Recognition
H	Instruction
L	Display Data

Note that the SCL should be set to “L” right after data transmission or during non-access because the serial interface is susceptible to external noises which may cause malfunctions. For added safety, inactivate the chip-select (CSb=“H”) temporary whenever 8-bit data transmission is completed. Fig 1 illustrates the interface timing of the 4-line serial interface mode.

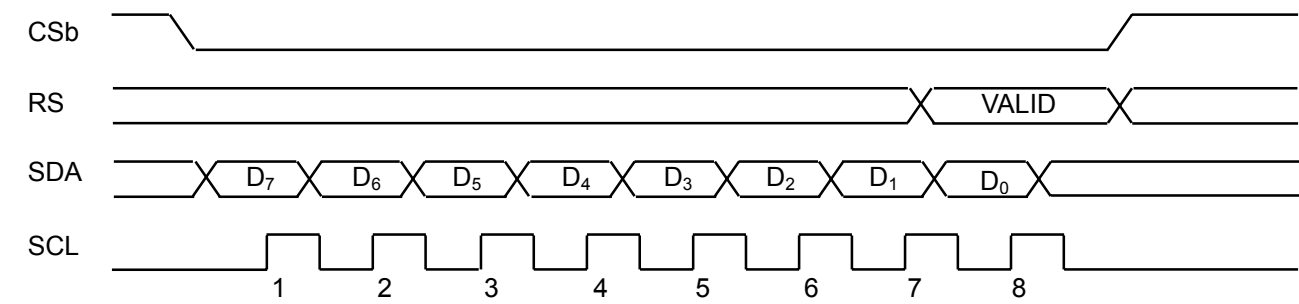


Fig 1 4-line Serial Interface Timing

(1-6) 3-line Serial Interface Mode

While the chip select is active (CSb=“L”), the SDA and SCL are enabled. While the chip select is not active (CSb=“H”), the SDA and SCL are disabled, and the internal shift register and the internal counter are being initialized. 9-bit serial data on the SDA is latched at the rising edge of the SCL signal in order of RS, D7, D6,..., and D0, and then converted into 9-bit parallel data at the timing of the internal signal produced from the 9th SCL signal. The data on the SDA is interpreted as display data or instruction according to the combination of the RS bit and the SPOL status, as follows.

Table 6 Data Recognition (3-line Serial Interface)

SPOL=L		SPOL=H	
RS	Data Recognition	RS	Data Recognition
0	Display Data	0	Instruction
1	Instruction	1	Display Data

Note that the SCL should be set to “L” right after data transmission or during non-access because the serial interface is susceptible to external noises which may cause malfunctions. For added safety, inactivate the chip-select (CSb=“H”) temporary whenever 9-bit data transmission is completed. Fig 2 illustrates the interface timing of the 3-line serial interface mode.

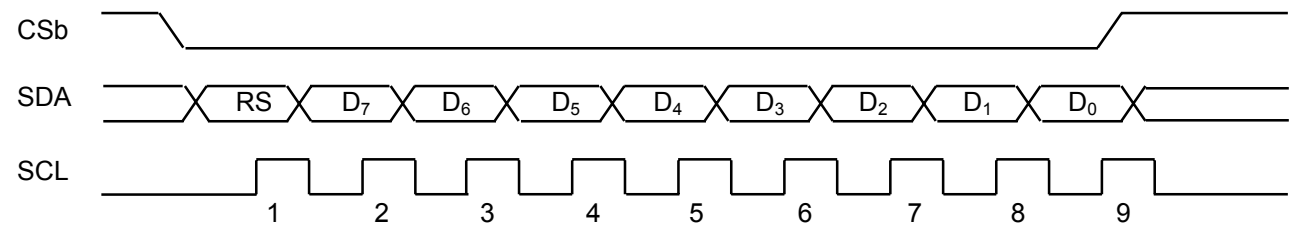


Fig 2 3-line Serial Interface Timing

(1-7) Accessing DDRAM

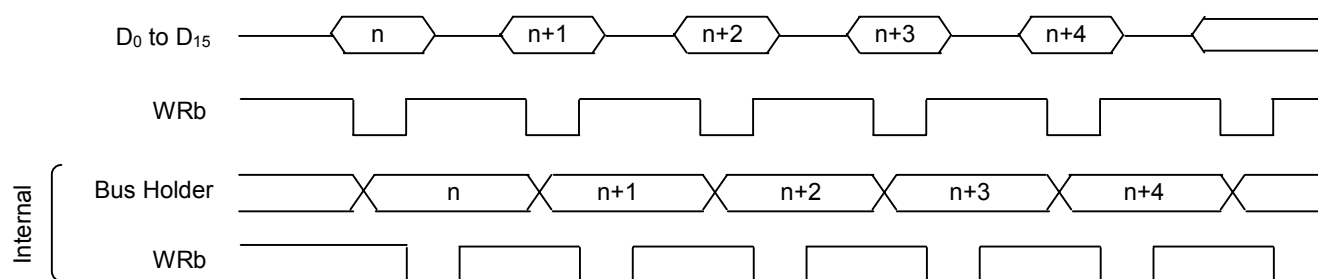
While the chip select is active (CSb="L"), the data from MPU can be written into the DDRAM or the instruction register. When the RS is "L", the data is interpreted as display data which is stored in the DDRAM. The display data is latched at the rising edge of the WRb signal in the 80-series MPU mode, or at the falling edge of the E signal in the 68-series MPU mode.

Table 7 Data Recognition

RS	Data Recognition
L	Display Data
H	Instruction

In the DDRAM read sequence, be sure to execute a dummy read right after setting an address or right after writing display data or instruction. The data from MPU is temporarily held in the internal bus-holder, then released on the internal data-bus, therefore a dummy data is read out by the 1st "Display Data Read" instruction. After that, the display data is read out from a specified address by the 2nd instruction. Note that the "Display Data Read" instruction cannot be used in the serial interface mode.

Display Data Write Operation



Display Data Read Operation

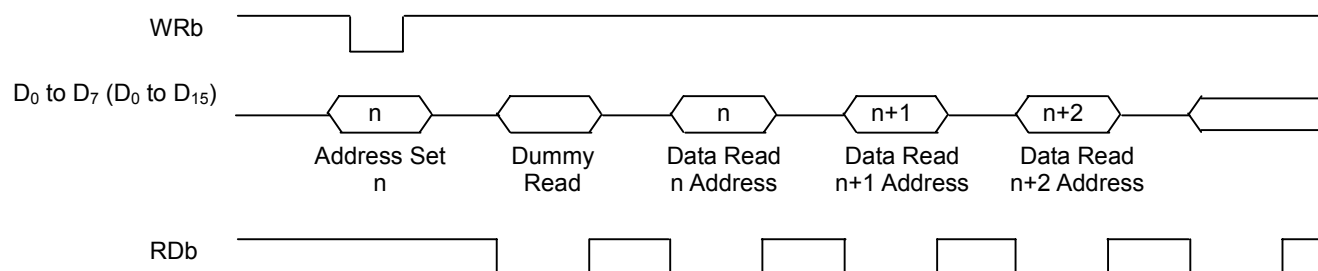


Fig 3 Internal-signal Timing of Display Data Read/Write Operations

NOTE) In 16-bit bus length mode, instruction is transmitted to/from instruction register in 16 bits, as well as display data.

(1-8) Accessing Instruction Register

Each instruction register has a specific address in between (0H) and (FH), and instruction data is read out from the register by the “Register Address” and “Register Read” instructions. For more information, refer to “(14-23) Register Address” and “(14-24) Register Read”.

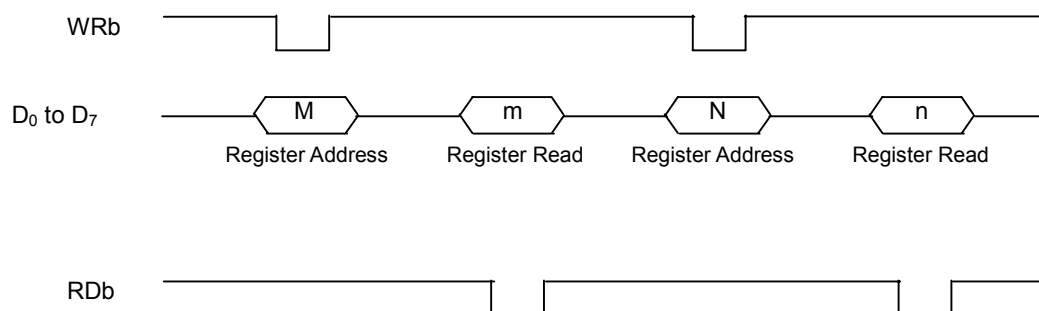


Fig 4 Access Timing of Instruction Register

(1-9) Selection of 8-/16-bit Bus Length (Parallel Interface Mode)

Either 8- or 16-bit bus length is selected by the D₀ (WLS) bit of the “Bus Length” instruction. In the 16-bit bus length mode, instruction as well as display data is transmitted to/from the instruction registers in 16 bits (D₁₅ to D₀). However, only lower 8 bits (D₇ to D₀) are valid for instruction register access. And only 12 bits are actually stored in the DDRAM, even though entire 16 bits (D₁₅ to D₀) are transmitted for DDRAM access. For more information, refer to “(4-4) Bit Assignment of Display Data”.

Table 8 Selection of 8-/16-bit Bus Length Mode

WLS	Bus Length Mode
L	8-bit Bus Length
H	16-bit Bus Length

(2) INITIAL DISPLAY LINE REGISTER

The address data in the initial display line register specifies the row address, which corresponds to an initial COM and is normally positioned on top of a screen in full display. The initial COM is the start position of common scanning, which is specified by the “Initial COM” instruction.

The row address, which is established in the initial display line register, is preset into the line counter whenever the FLM becomes “H”. At the rising edge of the CL signal, the line counter is counted-up, then 384-bit display data is latched into the data latch circuit. At the falling edge of the CL signal, the latch data is released to the grayscale control circuit to decide a grayscale level, then the segment drivers A_i, B_i and C_i (i=0 to 127) generate LCD waveforms.

(3) COLUMN AND ROW ADDRESS COUNTERS

The column and row address counters designate a column address and a row address respectively for DDRAM access, but they are completely independent from the line counter. The line counter provides a line address which is synchronized with display control timings such as the FLM and the CL.

(4) DDRAM

(4-1) DDRAM Address Range

The DDRAM is capable of 40 bits for row address and 1,536 bits (12-bit x 128-segment) for column address. The range of the column address is varied depending on the settings as follows, and the row address is from (00H) to (27H). Setting outside these ranges is not allowed, otherwise it may cause malfunctions. For DDRAM access, two data transmissions are needed for 1 RGB-pixel in the 8-bit bus length mode, and one transmission in the 16-bit bus length mode.

8-bit Bus Length

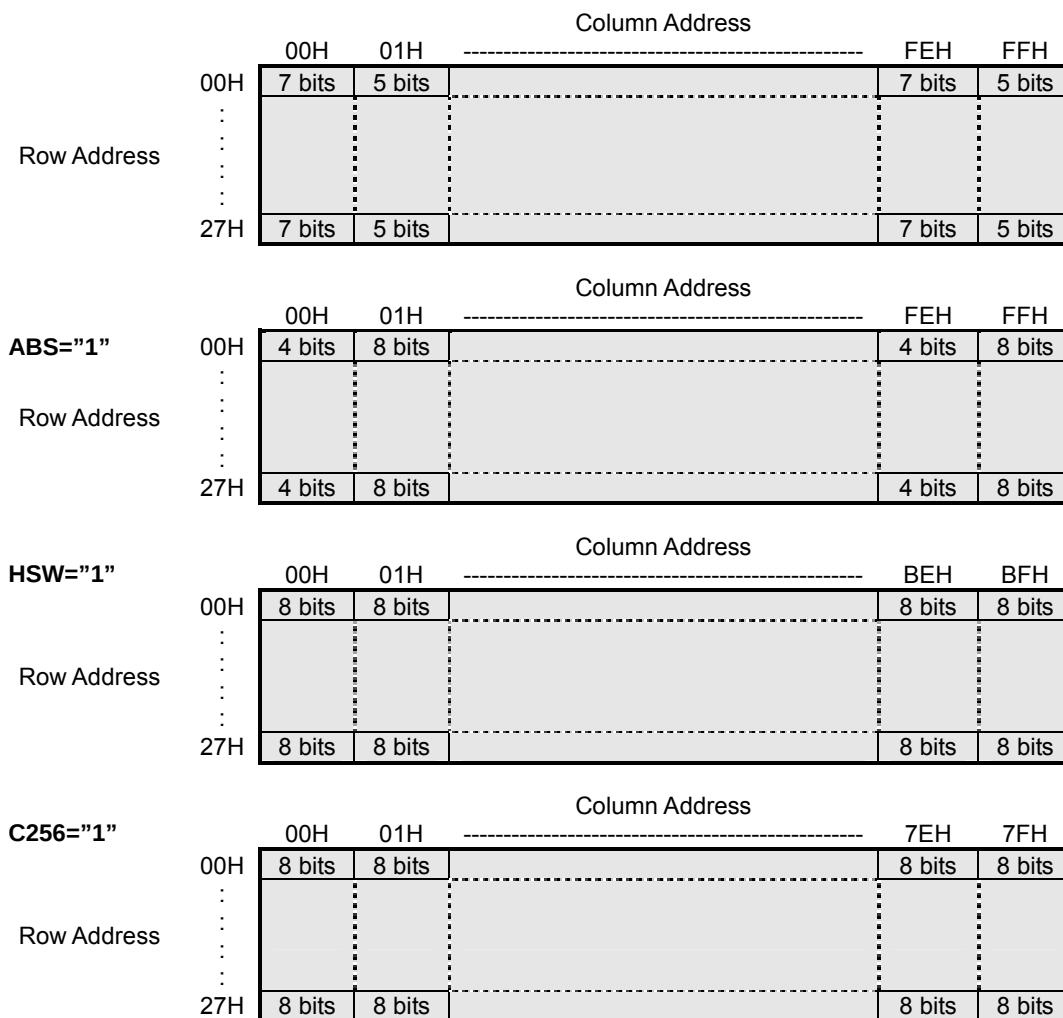


Fig 5 Range of Column Address in 8-bit Bus Length

16-bit Bus Length

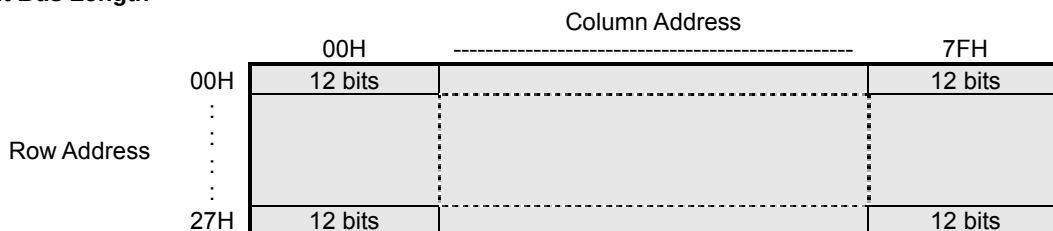


Fig 6 Range of Column Address in 16-bit Bus Length

(4-2) Window Area for DDRAM Access

In addition to the normal DDRAM access discussed previously, the window area access can be used. This area is set by the “Increment Control” instruction and the designation of the start point and the end point.

By the “Increment Control”, auto-increment is set for column address and row address individually. Once this mode is set up, the column address, row address or both are automatically counted up, whenever the DDRAM is accessed. And, the start point is specified by the “Column Address” and “Row Address” instructions, and the end point by the “Window End Column Address” and “Window End Row Address” instructions. For more information, refer to “(14-9) Increment Control”, “(14-25) Window End Column Address” and “(14-26) Window End Row Address”. The typical sequence of the window area setting is listed below.

1. Set “1” at D₃ (WIN), D₁ (AYI) and D₀ (AXI) of “Increment Control” instruction.
2. Set start point by “Column Address” and “Row Address” instructions.
3. Set end point by “Window End Column Address” and “Window End Row Address” instructions.
4. Window area is set up, and DDRAM can be accessed.

NOTE) The order of address setting is column address first, then row address.

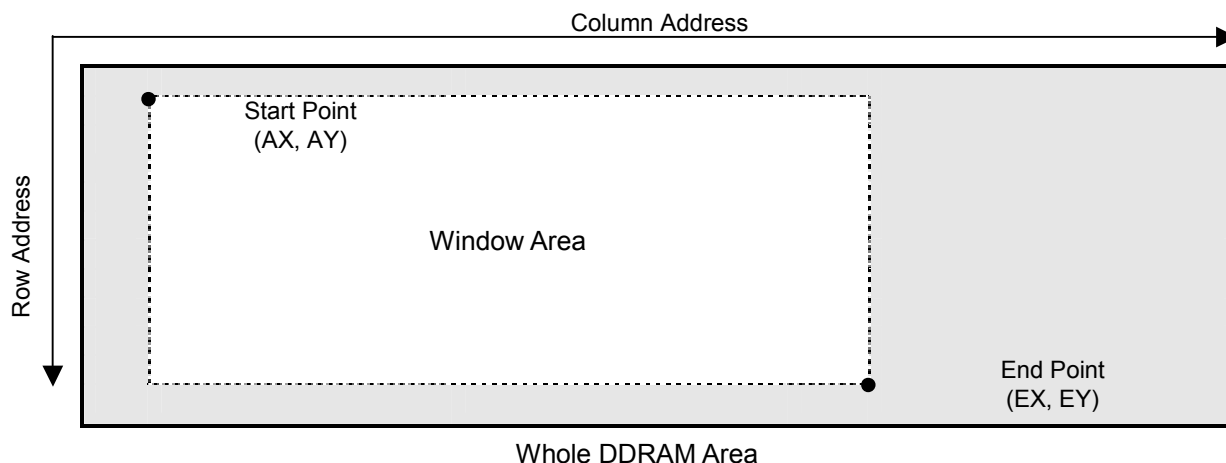
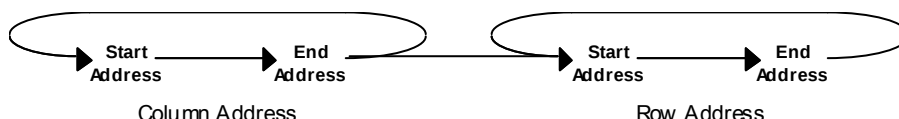


Fig 7 Window Area

NOTE1) The following relation should be maintained to avoid malfunctions.

- AX (Window Start Column Address) < EX (Window End Column Address) < Maximum Column Address
- AY (Window Start Row Address) < EY (Window End Row Address) < Maximum Row Address

NOTE3) Auto-increment in the window area



NOTE2) A read-modify-write operation is enabled by setting “1” at the D₂ (AIM) of the “Increment Control” instruction. Refer to the description about “AIM” bit in “(14-9) Increment Control”.

(4-3) Segment Direction

The DDRAM access direction is controlled by the D₀ (REF) bit of the “Display Control (2)” instruction. This function is used to reverse the segment direction for reducing the restrictions on the IC position of an LCD module.

(4-4-2) Bit Assignment in Variable 16-grayscale Mode

16-bit Bus Length (MON=0, PWM=0, C256=0, WLS=1)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																									
*	0	0	0	X=00H												↔		X=7FH											
*	0	1	1	X=7FH												↔		X=00H											
Display Data in DDRAM				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↔		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
Grayscale Palette				Palette A				Palette B				Palette C				↔		Palette A				Palette B				Palette C			
Segment Driver				SEGA ₀				SEGB ₀				SEGC ₀				↔		SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																									
*	0	0	1	X=00H												↔		X=7FH											
*	0	1	0	X=7FH												↔		X=00H											
Display Data in DDRAM				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↔		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
Grayscale Palette				Palette A				Palette B				Palette C				↔		Palette A				Palette B				Palette C			
Segment Driver				SEGC ₀				SEGB ₀				SEGA ₀				↔		SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																									
*	1	0	0	X=00H												↔		X=7FH											
*	1	1	1	X=7FH												↔		X=00H											
Display Data in DDRAM				D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔		D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Grayscale Palette				Palette A				Palette B				Palette C				↔		Palette A				Palette B				Palette C			
Segment Driver				SEGA ₀				SEGB ₀				SEGC ₀				↔		SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																									
*	1	0	1	X=00H												↔		X=7FH											
*	1	1	0	X=7FH												↔		X=00H											
Display Data in DDRAM				D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔		D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Grayscale Palette				Palette A				Palette B				Palette C				↔		Palette A				Palette B				Palette C			
Segment Driver				SEGC ₀				SEGB ₀				SEGA ₀				↔		SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

8-bit Bus Length (MON=0, PWM=0, C256=0, WLS=0)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver															
0	0	0	0	X=00H				X=01H				←→				X=FEH			
0	0	1	1	X=FEH				X=FFH				←→				X=00H			
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				←→				←→				←→				←→			
				←→				←→				←→				←→			
Grayscale Palette				Palette A				Palette B				Palette C				←→			
Segment Driver				SEGA ₀				SEGB ₀				SEGC ₀				←→			
																SEGA ₁₂₇			
																SEGB ₁₂₇			
																SEGC ₁₂₇			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver															
0	0	0	1	X=00H				X=01H				←→				X=FEH			
0	0	1	0	X=FEH				X=FFH				←→				X=00H			
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				←→				←→				←→				←→			
				←→				←→				←→				←→			
Grayscale Palette				Palette A				Palette B				Palette C				←→			
Segment Driver				SEGC ₀				SEGB ₀				SEGA ₀				←→			
																SEGC ₁₂₇			
																SEGB ₁₂₇			
																SEGA ₁₂₇			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver															
0	1	0	0	X=00H				X=01H				←→				X=FEH			
0	1	1	1	X=FEH				X=FFH				←→				X=00H			
Display Data in DDRAM				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄
				←→				←→				←→				←→			
				←→				←→				←→				←→			
Grayscale Palette				Palette A				Palette B				Palette C				←→			
Segment Driver				SEGA ₀				SEGB ₀				SEGC ₀				←→			
																SEGA ₁₂₇			
																SEGB ₁₂₇			
																SEGC ₁₂₇			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver															
0	1	0	1	X=00H				X=01H				←→				X=FEH			
0	1	1	0	X=FEH				X=FFH				←→				X=00H			
Display Data in DDRAM				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄
				←→				←→				←→				←→			
				←→				←→				←→				←→			
Grayscale Palette				Palette A				Palette B				Palette C				←→			
Segment Driver				SEGC ₀				SEGB ₀				SEGA ₀				←→			
																SEGC ₁₂₇			
																SEGB ₁₂₇			
																SEGA ₁₂₇			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
1	*	0	0	X=00H								X=01H								X=02H								..			
Display Data in DDRAM Grayscale Palette Segment Driver				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	..			
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				...			
				SEGA ₀				SEGB ₀				SEGC ₀				SEGA ₁				SEGB ₁				SEGC ₁				...			

Column Address / Display Data / Segment Driver																												
...	X=BDH								X=BEH								X=BFH											
..	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀				
...	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C							
...	SEGA ₁₂₆				SEGB ₁₂₆				SEGC ₁₂₆				SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇							

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
1	*	0	1	X=00H								X=01H								X=02H								..			
Display Data in DDRAM Grayscale Palette Segment Driver				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	..			
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				...			
				SEGC ₀				SEGB ₀				SEGA ₀				SEGC ₁				SEGB ₁				SEGA ₁				...			

Column Address / Display Data / Segment Driver																												
...	X=BDH								X=BEH								X=BFH											
..	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀				
...	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C							
...	SEGC ₁₂₆				SEGB ₁₂₆				SEGA ₁₂₆				SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇							

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
1	*	1	0	X=BEH				X=BFH								X=BDH								X=BEH				..			
Display Data in DDRAM Grayscale Palette Segment Driver				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	...			
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				...			
				SEGC ₀				SEGB ₀				SEGA ₀				SEGC ₁				SEGB ₁				SEGA ₁				...			

Column Address / Display Data / Segment Driver																												
...	X=01H				X=02H								X=00H								X=01H							
..	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄				
...	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C							
...	SEGC ₁₂₆				SEGB ₁₂₆				SEGA ₁₂₆				SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇							

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
1	*	1	1	X=BEH				X=BFH								X=BDH								X=BEH				..			
Display Data in DDRAM Grayscale Palette Segment Driver				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	...			
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				...			
				SEGA ₀				SEGB ₀				SEGC ₀				SEGA ₁				SEGB ₁				SEGC ₁				...			

Column Address / Display Data / Segment Driver																												
...	X=01H				X=02H								X=00H								X=01H							
..	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄				
...	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C							
...	SEGA ₁₂₆				SEGB ₁₂₆				SEGC ₁₂₆				SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇							

(4-4-3) Bit Assignment in Variable 8-level Gradation Mode

8-bit Bus Length (MON=0, PWM=0, C256=1, WLS=0)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																
*	*	0	0	X=00H								↔	X=7FH							
*	*	1	1	X=7FH								↔	X=00H							
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↕	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				Palette A			Palette B			Palette C		↔	Palette A			Palette B			Palette C	
				SEGA ₀			SEGB ₀			SEGC ₀		↔	SEGA ₁₂₇			SEGB ₁₂₇			SEGC ₁₂₇	

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																	
*	*	0	1	X=00H								↔	X=7FH								
*	*	1	0	X=7FH								↔	X=00H								
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
				Palette A			Palette B			Palette C		↔	Palette A			Palette B			Palette C		
				SEGC ₀			SEGB ₀			SEGA ₀		↔	SEGC ₁₂₇			SEGB ₁₂₇			SEGA ₁₂₇		

(4-4-4) Bit Assignment in Fixed 8-level Gradation Mode

16-bit Bus Length (MON=0, PWM=1, C256=0, WLS=1)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
*	0	0	0	X=00H														↔		X=7FH											
*	0	1	1	X=7FH														↔		X=00H											
Display Data in DDRAM				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↕		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁		
				Palette A				Palette B				Palette C				↔		Palette A				Palette B				Palette C					
				SEGA ₀				SEGB ₀				SEGC ₀				↔		SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇					

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
*	0	0	1	X=00H																↔		X=7FH									
*	0	1	0	X=7FH																↔		X=00H									
Display Data in DDRAM				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↕	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁			
				Palette A				Palette B				Palette C				↔		Palette A				Palette B				Palette C					
				SEGC ₀				SEGB ₀				SEGA ₀				↔		SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇					

NOTE) The data indicated with a slash mark (/) is invalid.

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																												
*	1	0	0	X=00H														↔	X=7FH													
*	1	1	1	X=7FH														↔	X=00H													
Display Data in DDRAM				D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀				
				Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C							
				SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇							

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																								
*	1	0	1	X=00H												↔	X=7FH											
*	1	1	0	X=7FH												↔	X=00H											
Display Data in DDRAM				D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
				SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

NOTE) The data indicated with a slash mark (/) is invalid.

8-bit Bus Length (MON=0, PWM=1, C256=0, WLS=0)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver											
0	0	0	0	X=00H			X=01H			↔			X=FEH		
0	0	1	1	X=FEH			X=FFH			↔			X=00H		
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄
				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				↔			↔			↔			↔		
Grayscale Palette				Palette A			Palette B			↔			Palette A		
Segment Driver				SEGA ₀			SEGB ₀			↔			SEGA ₁₂₇		

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver											
0	0	0	1	X=00H			X=01H			↔			X=FEH		
0	0	1	0	X=FEH			X=FFH			↔			X=00H		
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄
				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				↔			↔			↔			↔		
Grayscale Palette				Palette A			Palette B			↔			Palette A		
Segment Driver				SEGC ₀			SEGB ₀			↔			SEGC ₁₂₇		

NOTE) The data indicated with a slash mark (/) is invalid.

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver											
0	1	0	0	X=00H			X=01H			↔			X=FEH		
0	1	1	1	X=FEH			X=FFH			↔			X=00H		
Display Data in DDRAM				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				↔			↔			↔			↔		
Grayscale Palette				Palette A			Palette B			↔			Palette A		
Segment Driver				SEGA ₀			SEGB ₀			↔			SEGA ₁₂₇		

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver											
0	1	0	1	X=00H			X=01H			↔			X=FEH		
0	1	1	0	X=FEH			X=FFH			↔			X=00H		
Display Data in DDRAM				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				↔			↔			↔			↔		
Grayscale Palette				Palette A			Palette B			↔			Palette A		
Segment Driver				SEGC ₀			SEGB ₀			↔			SEGC ₁₂₇		

NOTE) The data indicated with a slash mark (/) is invalid.

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
1	*	0	0	X=00H								X=01H								X=02H								..			
Display Data in DDRAM Grayscale Palette Segment Driver				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	..			
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				...			
				SEGA ₀				SEGB ₀				SEGC ₀				SEGA ₁				SEGB ₁				SEGC ₁				...			

Column Address / Display Data / Segment Driver																								
...	X=BDH								X=BEH								X=BFH							
...	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
...	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
...	SEGA ₁₂₆				SEGB ₁₂₆				SEGC ₁₂₆				SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
1	*	0	1	X=00H								X=01H								X=02H								..			
Display Data in DDRAM Grayscale Palette Segment Driver				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	..			
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				...			
				SEGC ₀				SEGB ₀				SEGA ₀				SEGC ₁				SEGB ₁				SEGA ₁				...			

Column Address / Display Data / Segment Driver																								
...	X=BDH								X=BEH								X=BFH							
...	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
...	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
...	SEGC ₁₂₆				SEGB ₁₂₆				SEGA ₁₂₆				SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
1	*	1	0	X=BEH				X=BFH								X=BDH								X=BEH				..			
Display Data in DDRAM Grayscale Palette Segment Driver				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	...			
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				...			
				SEGC ₀				SEGB ₀				SEGA ₀				SEGC ₁				SEGB ₁				SEGA ₁				...			

Column Address / Display Data / Segment Driver																									
...	X=01H				X=02H								X=00H								X=01H				
...	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	
...	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				
...	SEGC ₁₂₆				SEGB ₁₂₆				SEGA ₁₂₆				SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇				

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
1	*	1	1	X=BEH				X=BFH								X=BDH								X=BEH				..			
Display Data in DDRAM Grayscale Palette Segment Driver				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	...			
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				...			
				SEGA ₀				SEGB ₀				SEGC ₀				SEGA ₁				SEGB ₁				SEGC ₁				...			

Column Address / Display Data / Segment Driver																									
...	X=01H				X=02H								X=00H								X=01H				
...	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	
...	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				
...	SEGA ₁₂₆				SEGB ₁₂₆				SEGC ₁₂₆				SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇				

8-bit Bus Length (MON=0, PWM=1, C256=1, WLS=0)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																
*	*	0	0	X=00H								↔	X=7FH							
*	*	1	1	X=7FH								↔	X=00H							
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				Palette A			Palette B			Palette C		↔	Palette A			Palette B			Palette C	
				SEGA ₀			SEGB ₀			SEGC ₀		↔	SEGA ₁₂₇			SEGB ₁₂₇			SEGC ₁₂₇	

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																	
*	*	0	1	X=00H								↔	X=7FH								
*	*	1	0	X=7FH								↔	X=00H								
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
				Palette A			Palette B			Palette C		↔	Palette A			Palette B			Palette C		
				SEGC ₀			SEGB ₀			SEGA ₀		↔	SEGC ₁₂₇			SEGB ₁₂₇			SEGA ₁₂₇		

(4-4-5) Bit Assignment in B&W Mode

16-bit Bus Length (MON=1, PWM=*, C256=0, WLS=1)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																								
*	0	0	0	X=00H										↔	X=7FH													
*	0	1	1	X=7FH										↔	X=00H													
Display Data in DDRAM				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↕	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
				Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
				SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																								
*	0	0	1	X=00H												↔	X=7FH											
*	0	1	0	X=7FH												↔	X=00H											
Display Data in DDRAM				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↕	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
				Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
				SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																								
*	1	0	0	X=00H										↔	X=7FH													
*	1	1	1	X=7FH										↔	X=00H													
Display Data in DDRAM				D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
				SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																								
*	1	0	1	X=00H										↔	X=7FH													
*	1	1	0	X=7FH										↔	X=00H													
Display Data in DDRAM				D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
				SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

NOTE) The data indicated with a slash mark (/) is invalid, and only MSB bits are effective.

8-bit Bus Length (MON=1, PWM=*, C256=0, WLS=0)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																								
0	0	0	0	X=00H				X=01H		↔	X=FEH				X=FFH													
0	0	1	1	X=FEH				X=FFH		↔	X=00H				X=01H													
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	↔	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁
				Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
				SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver															
0	0	0	1	X=00H				X=01H		↔	X=FEH				X=FFH				
0	0	1	0	X=FEH				X=FFH		↔	X=00H				X=01H				
Display Data in DDRAM										↔									
				Palette A				Palette B				↔		Palette A				Palette B	
				SEGC ₀				SEGB ₀				↔		SEGC ₁₂₇				SEGB ₁₂₇	
Segment Driver				SEGA ₀				↔		SEGA ₁₂₇									

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																	
0	1	0	0	X=00H	X=01H			↔	X=FEH	X=FFH											
0	1	1	1	X=FEH	X=FFH			↔	X=00H	X=01H											
Display Data in DDRAM				D ³	D ²	D ¹	D ⁰		↔	D ³	D ²	D ¹	D ⁰	D ⁷	D ⁶	D ⁵	D ⁴	D ³	D ²	D ¹	D ⁰
				Palette A		Palette B		Palette C	↔	Palette A		Palette B		Palette C							
				SEGA ₀		SEGB ₀		SEGC ₀	↔	SEGA ₁₂₇		SEGB ₁₂₇		SEGC ₁₂₇							

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																	
0	1	0	1	X=00H		X=01H		↔	X=FEH		X=FFH										
0	1	1	0	X=FEH		X=FFH		↔	X=00H		X=01H										
Display Data in DDRAM												↔									
				Palette A		Palette B		Palette C		↔		Palette A		Palette B		Palette C					
				SEGC ₀		SEGB ₀		SEGA ₀		↔		SEGC ₁₂₇		SEGB ₁₂₇		SEGA ₁₂₇					

NOTE) The data indicated with a slash mark (/) is invalid, and only MSB bits are effective.

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver											
1	*	0	0	X=00H				X=01H				X=02H			
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₇	D ₆	D ₅	D ₄	D ₇	D ₆	D ₅	D ₄
Grayscale Palette Segment Driver				Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	...	...	...
				SEGA ₀	SEGB ₀	SEGC ₀	SEGA ₁	SEGB ₁	SEGC ₁	...	...	...	...	...	...

Column Address / Display Data / Segment Driver																
...	X=BDH				X=BEH				X=BFH							
...	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
...	Palette A		Palette B		Palette C		Palette A		Palette B		Palette C					
...	SEGA ₁₂₆		SEGB ₁₂₆		SEGC ₁₂₆		SEGA ₁₂₇		SEGB ₁₂₇		SEGC ₁₂₇					

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver											
1	*	0	1	X=00H				X=01H				X=02H			
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₇	D ₆	D ₅	D ₄	D ₇	D ₆	D ₅	D ₄
Grayscale Palette Segment Driver				Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	...	...	...	...	...	...
				SEGC ₀	SEGB ₀	SEGA ₀	SEGC ₁	SEGB ₁	SEGA ₁	...	...	...	...	...	...

Column Address / Display Data / Segment Driver																								
...	X=BDH				X=BEH				X=BFH															
...	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀								
...	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
...	SEGC ₁₂₆				SEGB ₁₂₆				SEGA ₁₂₆				SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver											
1	*	1	0	X=BEH			X=BFH			X=BDH			X=BEH		
Display Data in DDRAM				D ₃	D ₂	D ₁	D ₃	D ₂	D ₁	D ₃	D ₂	D ₁	D ₃	D ₂	D ₁
Grayscale Palette Segment Driver				Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	...	...	...	...	...	...
				SEGC ₀	SEGB ₀	SEGA ₀	SEGC ₁	SEGB ₁	SEGA ₁	...	...	...	...	...	...

Column Address / Display Data / Segment Driver												
..	X=01H			X=02H			X=00H			X=01H		
..	D ₃	D ₂	D ₁	D ₃	D ₂	D ₁	D ₃	D ₂	D ₁	D ₃	D ₂	D ₁
...	Palette A			Palette B			Palette C			Palette A		
...	SEGC ₁₂₆			SEGB ₁₂₆			SEGA ₁₂₆			SEGC ₁₂₇		
...	SEGC ₁₂₇			SEGB ₁₂₇			SEGA ₁₂₇			SEGC ₁₂₈		

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver											
1	*	1	1	X=BEH			X=BFH			X=BDH			X=BEH		
Display Data in DDRAM				D ₃	D ₂	D ₁	D ₃	D ₂	D ₁	D ₃	D ₂	D ₁	D ₃	D ₂	D ₁
Grayscale Palette Segment Driver				Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	...	...	...	...	...	...
				SEGA ₀	SEGB ₀	SEGC ₀	SEGA ₁	SEGB ₁	SEGC ₁	...	...	...	...	...	...

Column Address / Display Data / Segment Driver												
...	X=01H			X=02H			X=00H			X=01H		
...	D ₃	D ₂	D ₁	D ₃	D ₂	D ₁	D ₃	D ₂	D ₁	D ₃	D ₂	D ₁
...	Palette A			Palette B			Palette C			Palette A		
...	SEGA ₁₂₆			SEGB ₁₂₆			SEGC ₁₂₆			SEGA ₁₂₇		

NOTE) The data indicated with a slash mark (/) is invalid, and only MSB bits are effective.

8-bit Bus Length (MON=1, PWM=*, C256=1, WLS=0)

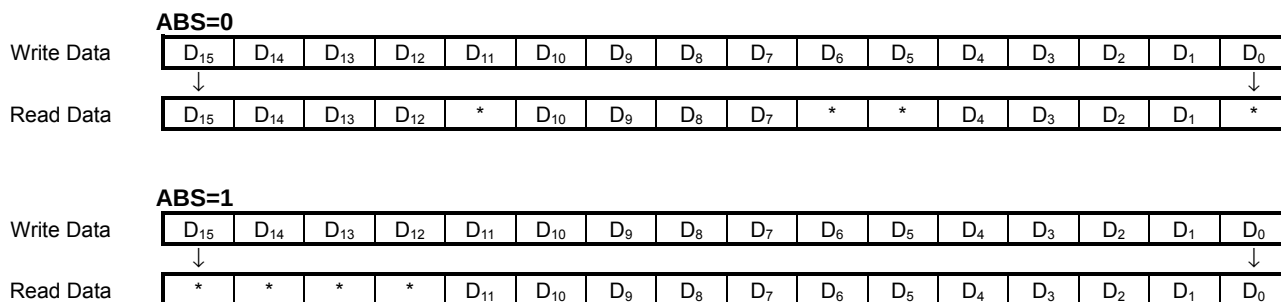
HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																																												
*	*	0	0	X=00H								↔	X=7FH																																			
*	*	1	1	X=7FH								↔	X=00H																																			
Display Data in DDRAM				D ₇			D ₆			D ₅			D ₄			D ₃			D ₂			D ₁			D ₀	↔	D ₇			D ₆			D ₅			D ₄			D ₃			D ₂			D ₁			D ₀
				Palette A			Palette B			Palette C			↔	Palette A			Palette B			Palette C																												
				SEGA ₀			SEGB ₀			SEGC ₀			↔	SEGA ₁₂₇			SEGB ₁₂₇			SEGC ₁₂₇																												

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																
*	*	0	1	X=00H								↔	X=7FH							
*	*	1	0	X=7FH								↔	X=00H							
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				Palette A			Palette B			Palette C		↔	Palette A			Palette B			Palette C	
				SEGC ₀			SEGB ₀			SEGA ₀		↔	SEGC ₁₂₇			SEGB ₁₂₇			SEGA ₁₂₇	

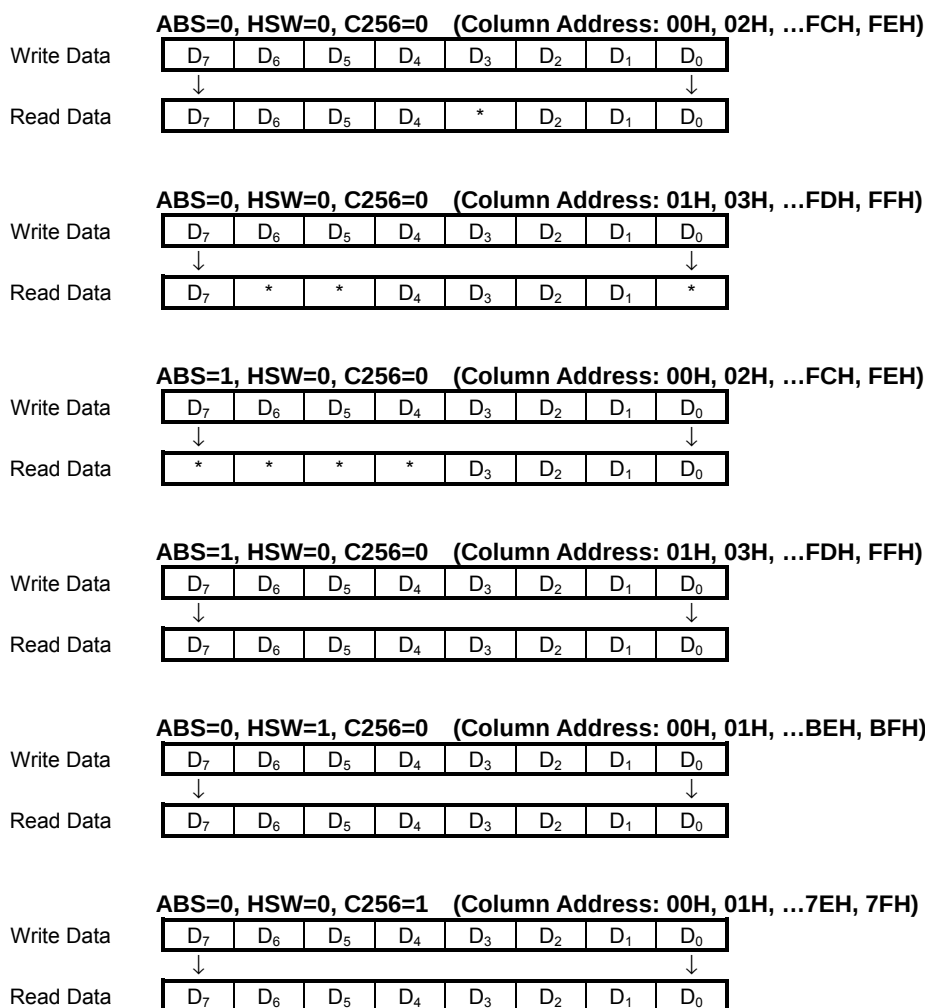
NOTE) The data indicated with a slash mark (/) is invalid, and only MSB bits are effective.

(4-5) Write Data and Read Data

16-bit Bus Length



8-bit Bus Length



NOTE) * : Invalid Data

(5) GRAYSCALE CONTROL CIRCUIT

(5-1) Display Mode Selection

A display mode is selected by the combination of the D₂ (MON) bit of the “Display Control (1)” instruction and the D₃ (PWM) and D₂ (C256) bits of the “Display Mode Control” instruction, as shown below.

Table 11 Display Mode Selection

MON	PWM	C256 (NOTE1)	Display Mode		Bus Length		Oscillation (NOTE2)
0	0	0	Variable 16-grayscale Mode	4096 Colors	8-/16-bit	(WLS=0/1)	f _{osc1}
		1	Variable 8-grayscale Mode	256 Colors	8-bit	(WLS=0)	
	1	0	Fixed 8-grayscale Mode	256 Colors	8-/16-bit	(WLS=0/1)	f _{osc2}
		1			8-bit	(WLS=0)	
1	*	0	B&W Mode	Black & White	8-/16-bit	(WLS=0/1)	f _{osc3}
		1			8-bit	(WLS=0)	

NOTE1) In the variable grayscale mode, “C256” bit selects either 16-grayscale (4K colors) or 8-grayscale (256 colors). When C256=“0” (16-grayscale), all 12 bits are assigned to 1 RGB-pixel. When C256=“1” (8-grayscale), only 8 bits are assigned and the 8-bit bus length should be used. In the fixed 8-grayscale mode or the B&W mode, the “C256” bit is usually “1”. For more information how the display data is assigned, refer to “(4-4) Bit Assignment of Display Data”.

NOTE2) Oscillation frequency is decided according to the display mode, and is fine-tuned by the “Frequency Control” Instruction. Refer to “(10) OSCILLATOR” and “OSCILLATION FREQUENCY AND FRAME FREQUENCY”.

(5-1-1) Variable 16-grayscale Mode

In this mode, each of the palettes A_j, B_j and C_j (j=0-15) is capable of selecting 16 from 32 grayscales (0/31-31/31) by setting palette data in the grayscale palette. Then, each of the segment drivers SEG_{Ai}, SEG_{Bi} and SEG_{Ci} (i=0 to 127) generates 16 grayscales to achieve 4,096 colors. Refer to Table 12-1 and Table 12-2.

(5-1-2) Variable 8-grayscale Mode

Each of the palettes A_j, B_j and C_j (j=0-15) is capable of selecting 8 from 32 grayscales (0/31-31/31). 2 segment drivers of 1 RGB-group (SEG_{Ai}, SEG_{Bi} and SEG_{Ci} (i=0 to 127)) generate 8 grayscales, and the other driver does 4 grayscales to achieve 256 colors. Refer to Table 13-1 through Table 13-4. The 8-bit bus length is usually used in this mode.

(5-1-3) Fixed 8-grayscale Mode

The palette setting is not necessary, because the palettes A_j, B_j and C_j (j=0-15) are always fixed at 4 or 8 grayscales between 0/7 and 7/7. 2 segment drivers of 1 RGB-group (SEG_{Ai}, SEG_{Bi} and SEG_{Ci} (i=0 to 127)) are fixed at 8 grayscales, and the other driver is 4 grayscales, then results in 256 colors. Refer to Table 14-1 and Table 14-2.

(5-1-4) B&W Mode

The palette setting is not necessary, where the only MSB bits of display data are valid. Refer to Table 15.

(6) GRAYSCALE PALETTE

(6-1) Grayscale Selection in Variable 16-grayscale Mode

Table 12-1 Grayscale selection

(Palette Aj, Bj, and Cj)

Display Data MSB----LSB	Palette Name
0 0 0 0	Palette A0/B0/C0
0 0 0 1	Palette A1/B1/C1
0 0 1 0	Palette A2/B2/C2
0 0 1 1	Palette A3/B3/C3
0 1 0 0	Palette A4/B4/C4
0 1 0 1	Palette A5/B5/C5
0 1 1 0	Palette A6/B6/C6
0 1 1 1	Palette A7/B7/C7
1 0 0 0	Palette A8/B8/C8
1 0 0 1	Palette A9/B9/C9
1 0 1 0	Palette A10/B10/C10
1 0 1 1	Palette A11/B11/C11
1 1 0 0	Palette A12/B12/C12
1 1 0 1	Palette A13/B13/C13
1 1 1 0	Palette A14/B14/C14
1 1 1 1	Palette A15/B15/C15

Table 12-2 Grayscale Palette

(Palette Aj, Bj, and Cj)

Palette Data MSB---LSB	Grayscale	Default Setting	Palette Data MSB---LSB	Grayscale	Default Setting
0 0 0 0 0	0	Palette A0/B0/C0	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	Palette A8/B8/C8
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31	Palette A1/B1/C1	1 0 0 1 1	19/31	Palette A9/B9/C9
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	Palette A2/B2/C2	1 0 1 0 1	21/31	Palette A10/B10/C10
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette A3/B3/C3	1 0 1 1 1	23/31	Palette A11/B11/C11
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31	Palette A4/B4/C4	1 1 0 0 1	25/31	Palette A12/B12/C12
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	Palette A5/B5/C5	1 1 0 1 1	27/31	Palette A13/B13/C13
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31	Palette A6/B6/C6	1 1 1 0 1	29/31	Palette A14/B14/C14
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette A7/B7/C7	1 1 1 1 1	31/31	Palette A15/B15/C15

NOTE1) "MON=0", "PWM=0", "C256=0"

NOTE2) Applied to palette Aj, Bj and Cj (j=0 to 15)

(6-2) Grayscale Selection in Variable 8-grayscale Mode

Table 13-1 Grayscale selection

(Palette Aj and Bj)

Display Data MSB---LSB	Palette Name
0 0 0 *	Palette A1/B1/C1
0 0 1 *	Palette A3/B3/C3
0 1 0 *	Palette A5/B5/C5
0 1 1 *	Palette A7/B7/C7
1 0 0 *	Palette A9/B9/C9
1 0 1 *	Palette A11/B11/C11
1 1 0 *	Palette A13/B13/C13
1 1 1 *	Palette A15/B15/C15

Table 13-2 Grayscale Palette

(Palette Aj and Bj)

Palette Data MSB---LSB	Grayscale	Default Setting	Palette Data MSB---LSB	Grayscale	Default Setting
0 0 0 0 0	0		1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31	Palette A1/B1/C1	1 0 0 1 1	19/31	Palette A9/B9/C9
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31		1 0 1 0 1	21/31	
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette A3/B3/C3	1 0 1 1 1	23/31	Palette A11/B11/C11
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31		1 1 0 0 1	25/31	
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	Palette A5/B5/C5	1 1 0 1 1	27/31	Palette A13/B13/C13
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31		1 1 1 0 1	29/31	
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette A7/B7/C7	1 1 1 1 1	31/31	Palette A15/B15/C15

NOTE1) "MON=0", "PWM=0", "C256=1".

NOTE2) Applied to palette Aj and Bj (j=0 to 15)

NOTE3) Palette 0, 2, 4, 6, 8, 10, 12 and 14 are disabled.

Table 13-3 Grayscale selection

(Palette Cj)

Display Data MSB---LSB	Palette Name
0 0 **	Palette A3/B3/C3
0 1 **	Palette A7/B7/C7
1 0 **	Palette A11/B11/C11
1 1 **	Palette A15/B15/C15

Table 13-4 Grayscale Palette

(Palette Cj)

Palette Data MSB---LSB	Grayscale	Default Setting	Palette Data MSB---LSB	Grayscale	Default Setting
0 0 0 0 0	0		1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31		1 0 0 1 1	19/31	
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31		1 0 1 0 1	21/31	
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette A3/B3/C3	1 0 1 1 1	23/31	Palette A11/B11/C11
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31		1 1 0 0 1	25/31	
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31		1 1 0 1 1	27/31	
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31		1 1 1 0 1	29/31	
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette A7/B7/C7	1 1 1 1 1	31/31	Palette A15/B15/C15

NOTE1) "MON=0", "PWM=0", "C256=1"

NOTE2) Applied to palette Cj (j=0 to 15)

NOTE3) Palette 0, 1, 2, 4, 5, 6, 8, 9, 10, 12, 13 and 14 are disabled.

(6-3) Grayscale Selection in Fixed 8-grayscale Mode

Table 14-1 Grayscale Selection

(Palette Aj and Bj)

Display Data MSB- - - -LSB	Grayscale
0 0 0 *	0/7
0 0 1 *	1/7
0 1 0 *	2/7
0 1 1 *	3/7
1 0 0 *	4/7
1 0 1 *	5/7
1 1 0 *	6/7
1 1 1 *	7/7

Table 14-2 Grayscale Palette

(Palette Cj)

Display Data MSB- - - -LSB	Grayscale
0 0 **	0/7
0 1 **	3/7
1 0 **	5/7
1 1 **	7/7

NOTE1) "MON=0", "PWM=1", "C256=0 or 1"

(6-4) Grayscale Selection in B&W Mode

Table 15 Grayscale Selection

Display Data MSB- - - -LSB	Grayscale
0 ***	0
1 ***	1

NOTE1) "MON=1", "PWM=0 or 1" and "C256=0 or 1"

(7) DISPLAY TIMING GENERATOR

The display timing generator generates timing clocks such as the CL (Line Clock), FR (Frame Rate) and FLM (First Line Maker) by dividing an oscillation frequency. These clocks are used inside the LSI, and are activated by setting “1” at the D₀ (SON) bit of the “Duty-1 /Display Clock ON/OFF” instruction.

The CL is used for the line counter and the data latch circuit. At the rising edge of the CL signal, the line counter is counted up, then 384-bit display data is latched into the data latch circuit. At the falling edge of the CL signal, the latch data is released to the grayscale control circuit, then segment drivers Ai, Bi and Ci (i=0 to 127) produce LCD driving waveforms. The internal data-transmission timing between the DDRAM and segment drivers is completely independent of external data-transmission timing, so that MPU makes access to the LSI without concern for the LSI's internal operation.

The FR and FLM are generated by the CL. The FR toggles once every frame in the default status, and is programmed to toggle once every N lines. And the FLM is used to specify an initial display line, which is preset whenever the FLM becomes “H”.

(8) DATA LATCH CIRCUIT

The data latch circuit is used to temporarily store display data which is released to the grayscale control circuit. The display data in this circuit is updated in synchronization with the CL. The “All Pixels ON/OFF”, “Display ON/OFF” and “Reverse Display ON/OFF” instructions control the data in this circuit, but does not change the data in the DDRAM.

(9) COMMON DRIVERS AND SEGMENT DRIVERS

The LSI includes 40 common drivers and 384-segment drivers. The common drivers generate LCD driving waveforms formed on the V_{LCD}, V₁, V₄ and V_{SSH} levels. The segment drivers generate waveforms formed on the V_{LCD}, V₂, V₃ and V_{SSH} levels.

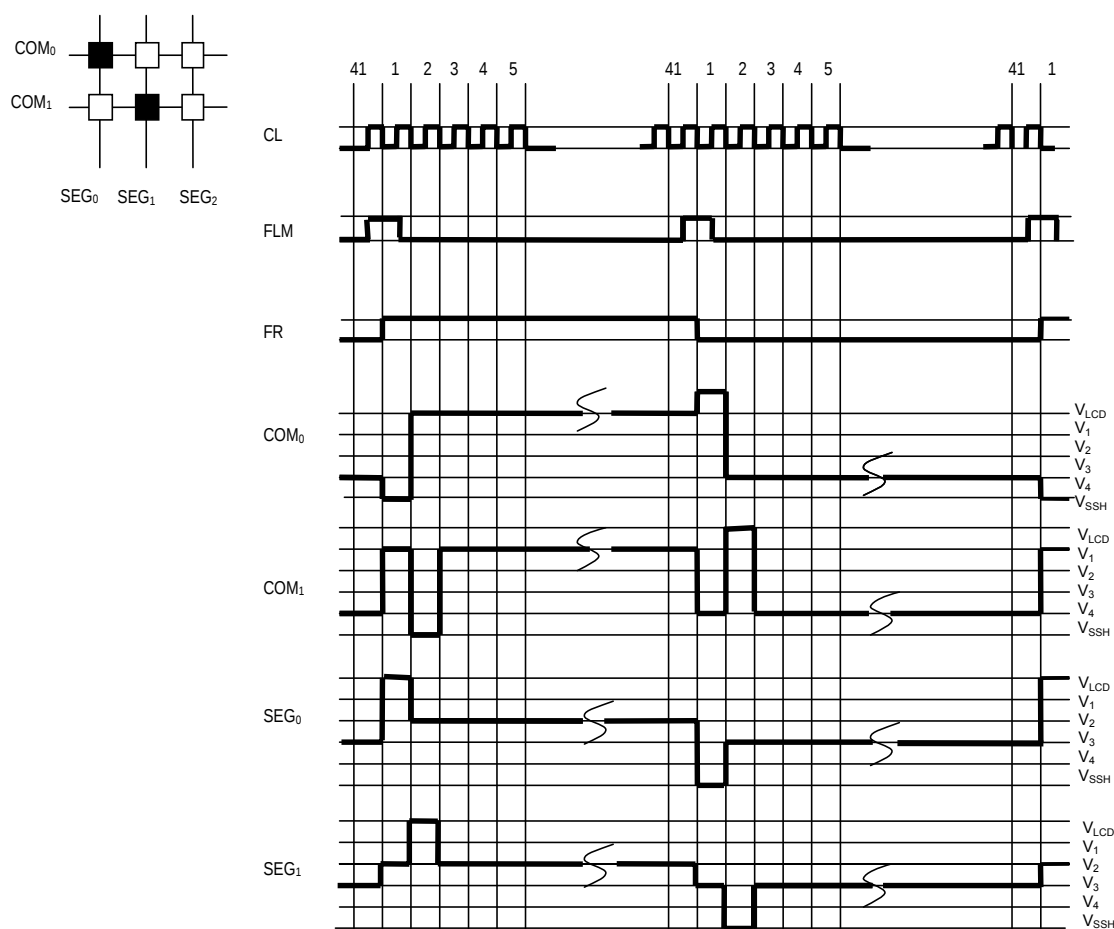


Fig 8 LCD Driving Waveforms (B&W Mode, Color Reverse OFF, 1/41 Duty)

(10) OSCILLATOR

The oscillator is equipped with a resistor and a capacitor, and generates internal clocks used for the display timing generator and the voltage booster. The internal resistor is enabled by setting “0” at the D₁ (CKS) bit of the “Bus Length” instruction. For more accurate frequency, using an external resistor or external clock is recommended.

When using the internal resistor, the resistance is controlled to optimize frame frequency for different LCD panels, by setting the D₂-D₀ (RF2-RF0) bits of the “Frequency Control” instruction. For more safety, make sure what is the best frequency in the particular application.

(10-1) Using Internal Resistor (CKS=0)

In this case, the OSC1 should be fixed at “H” or “L” and the OSC2 is open. The oscillation frequency is varied according to the display mode, as follows.

Table 16 Oscillation Frequency vs. Display Mode

Symbol	MON	PWM	Display Mode
f _{OSC1}	0	0	Variable 8-/16-grayscale Mode
f _{OSC2}	0	1	Fixed 8-grayscale Mode
f _{OSC3}	1	*	B&W Mode

*: Don't care

(10-2) Using External Resistor (CKS=1)

Be sure to connect the OSC1 and OSC2 with an external resistor. The frequency of the oscillator should be adjusted to the same value generated by the internal resistor.

(10-3) Using External Clock (CKS=1)

Input external clock to the OSC1 and leave the OSC2 open. The external clock with 50% duty is recommended. The frequency of the external clock should be the same value generated by the internal resistor.

(11) LCD POWER SUPPLY

The internal LCD power supply is organized into the voltage converter and the voltage booster. The voltage converter consists of the reference voltage generator, the voltage regulator with EVR and the LCD bias voltage generator. The configuration of the LCD power supply is arranged by setting the D₃ (AMPON) and D₁ (DCON) bits of the “Power Control” instruction. For this configuration, the internal LCD power supply can be partially used in combination with an external supply voltage, as shown in Table 17.

Table 17 Configuration of LCD Power Supply

DCON	AMPON	Voltage Booster	Voltage Converter	External Supply Voltage	NOTE
0	0	Inactive	Inactive	V _{OUT} , V _{LCD} , V ₁ , V ₂ , V ₃ , V ₄	1, 3, 4
0	1	Inactive	Active	V _{OUT}	2, 3, 4
1	1	Active	Active	—	-

NOTE1) No internal LCD power supply is used. The LCD bias voltages are externally supplied, and the C₁₊, C₁₋, C₂₊, C₂₋, C₃₊, C₃₋, C₄₊, C₄₋, V_{REF}, V_{REG} and V_{EE} are open.

NOTE2) Only the voltage converter is used. The V_{OUT} is externally supplied, and the C₁₊, C₁₋, C₂₊, C₂₋, C₃₊, C₃₋, C₄₊, C₄₋, and V_{EE} are open. The reference voltage is supplied on the V_{REF}.

NOTE3) The following relation among each LCD bias voltages must be maintained.

$$V_{OUT} \geq V_{LCD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SSH}$$

NOTE4) If the internal LCD power supply doesn't have enough capability to drive the particular LCD panel, use the external LCD power supply. Otherwise, it may affect display quality.

(11-1) Voltage Booster

The internal voltage booster generates up to $5 \times V_{EE}$ voltage. The boost level is selected from 2x, 3x, 4x or 5x, by setting the D_2 - D_0 ($VU2$ - $VU0$) bits of the “Boost Level” instruction. The boost voltage V_{OUT} must not exceed 18.0V, otherwise the voltage stress may cause a permanent damage to the LSI.

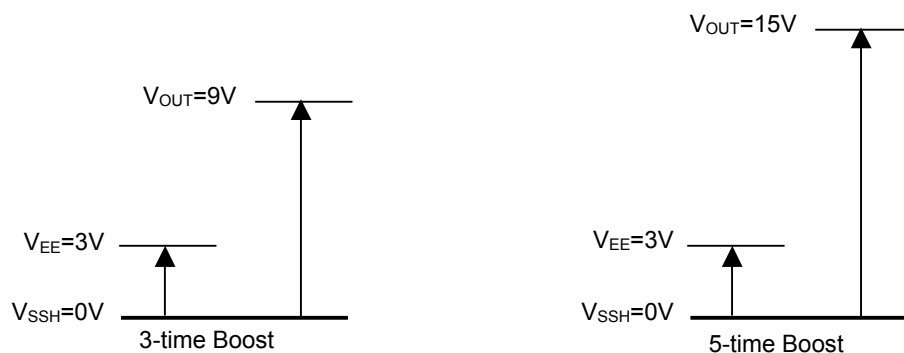


Fig 9 Boost Voltage

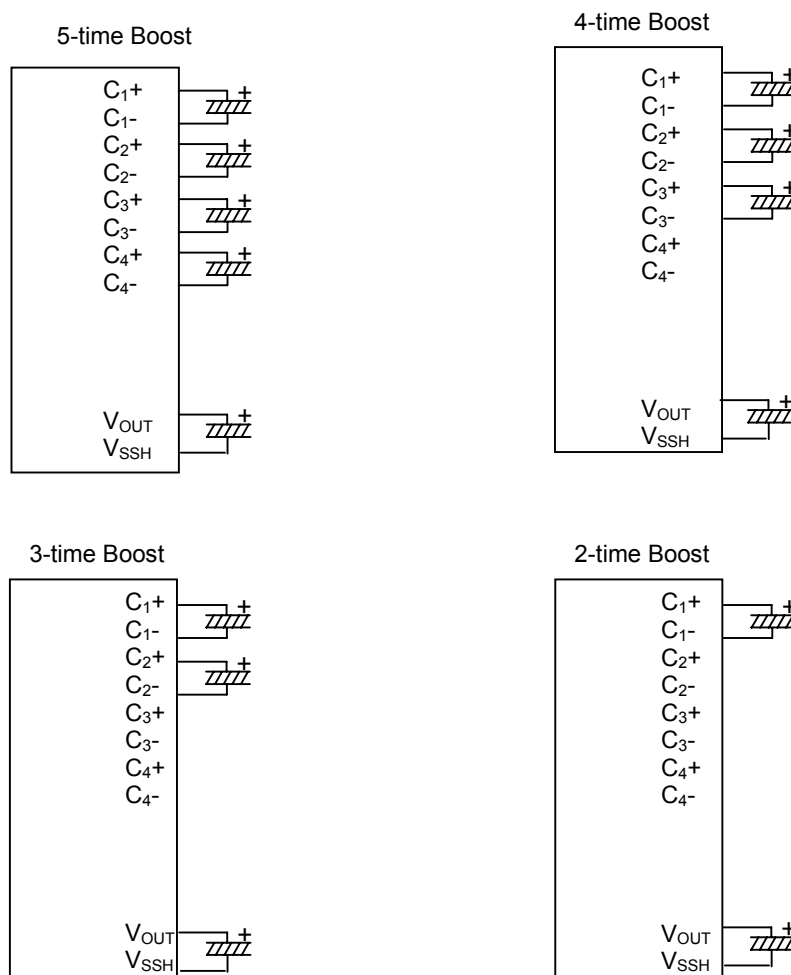


Fig 10 External Capacitor Connection of Voltage Booster

(11-2) Voltage Converter

(11-2-1) Reference Voltage Generator

The reference voltage generator produces the reference voltage ($V_{BA}=0.9 \times V_{EE}$). When using the internal LCD power supply, connect the V_{BA} and the V_{REF} , or supply $0.9 \times V_{EE}$ or lower voltage on the V_{REF} . When using an external LCD power supply, the V_{BA} should be open.

(11-2-2) Voltage Regulator

The voltage regulator consists of an operational amplifier with gain control and EVR. The V_{REF} voltage is multiplied to obtain the V_{REG} voltage, and its multiple (boost level) is set by the D_2 - D_0 ($VU2$ - $VU0$) bits of the “Boost Level” instruction. The formula is shown below.

$$V_{REG} = V_{REF} \times N \quad (N: \text{Boost Level})$$

(11-2-3) Electrical Variable Resistor (EVR)

The EVR is used to fine-tune the V_{LCD} voltage to optimize display contrast. The EVR value is controlled in 128 steps by setting the D_3 - D_0 (DV_6 - DV_0) bits of the “EVR Control” instruction. The formula is shown below.

$$V_{LCD} = 0.5 \times V_{REG} + M (V_{REG} - 0.5 \times V_{REG}) / 127 \quad (M: \text{EVR Value})$$

(11-2-4) LCD Bias Voltage Generator

The LCD bias voltage generator consists of buffer amplifiers and bleeder resistors to generate the LCD bias voltages such as the V_{LCD} , V_1 , V_2 , V_3 and V_4 , and its bias ratio is selected from 1/4, 1/5, 1/6, 1/7 or 1/8..

As shown in Fig 11, when using only the internal LCD power supply, the capacitors CA2 are connected to the V_{LCD} , V_1 , V_2 , V_3 and V_4 respectively.

As shown in Fig 12, when using no internal LCD power supply, the LCD bias voltages are externally supplied on the V_{LCD} , V_1 , V_2 , V_3 and V_4 , and the internal LCD power supply should be turned off by setting “0” at the “DCON” and “AMPON” bits. And the C_{1+} , C_{1-} , C_{2+} , C_{2-} , C_{3+} , C_{3-} , C_{4+} , C_{4-} , V_{EE} , V_{REF} and V_{REG} are open.

Fig 13 and 14 show typical peripheral circuits when partially using the LCD power supply without the reference voltage generator.

Fig 15 shows the circuit when partially using the LCD power supply without the voltage booster.

(11-3) External Components for LCD Power Supply

Using Only Internal LCD Power Supply (5x boost)

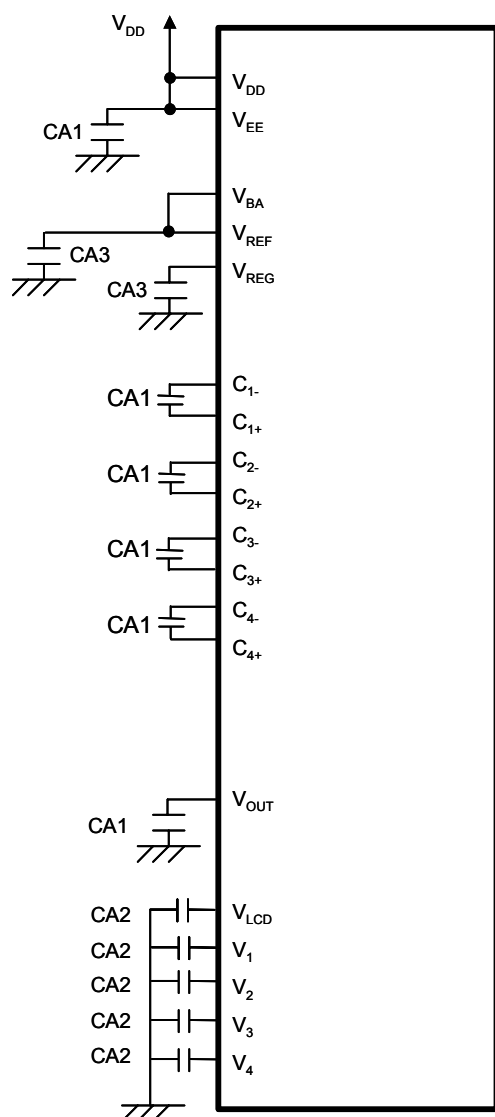


Fig 11

Using Only External LCD Power Supply

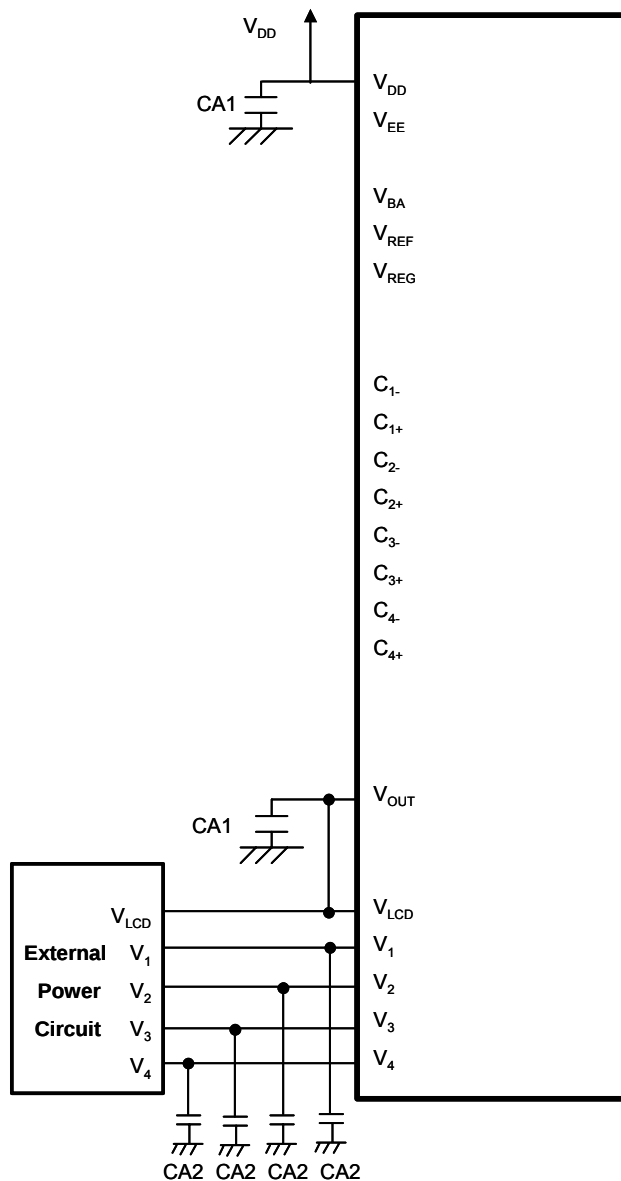


Fig 12

Reference Values

CA1	1.0 to 4.7 μ F
CA2	1.0 to 2.2 μ F
CA3	0.1 μ F

NOTE1) B grade capacitor is recommended for CA1-CA3. Make sure what is the best capacitor value in the particular application.

NOTE2) Parasitic resistance on the power supply lines (V_{DD} , V_{SS} , V_{EE} , V_{SSH} , V_{OUT} , V_{LCD} , V_1 , V_2 , V_3 and V_4) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, be sure to lay out the shortest wires and place capacitors as close to the LSI as possible.

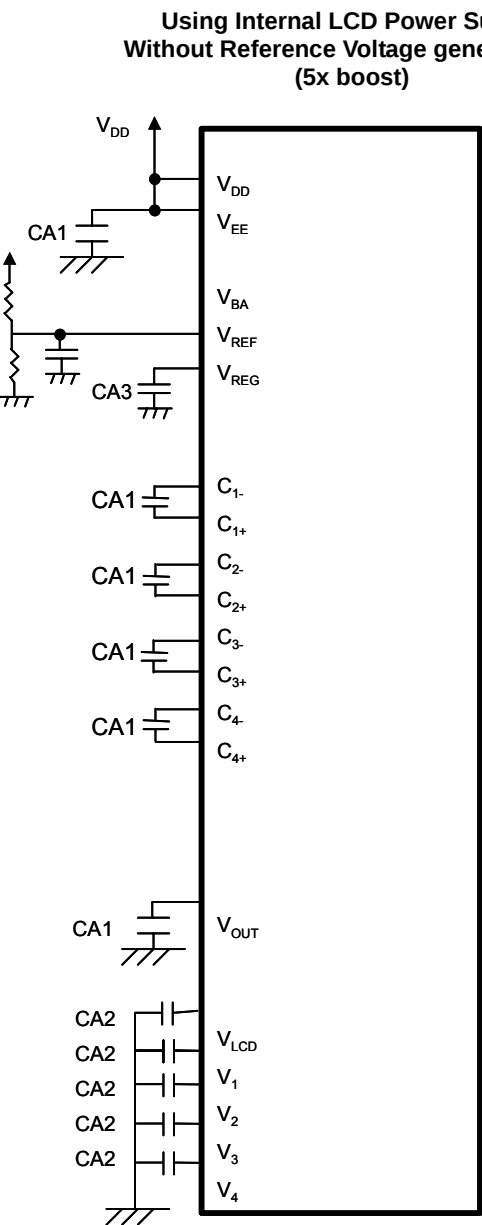


Fig 13

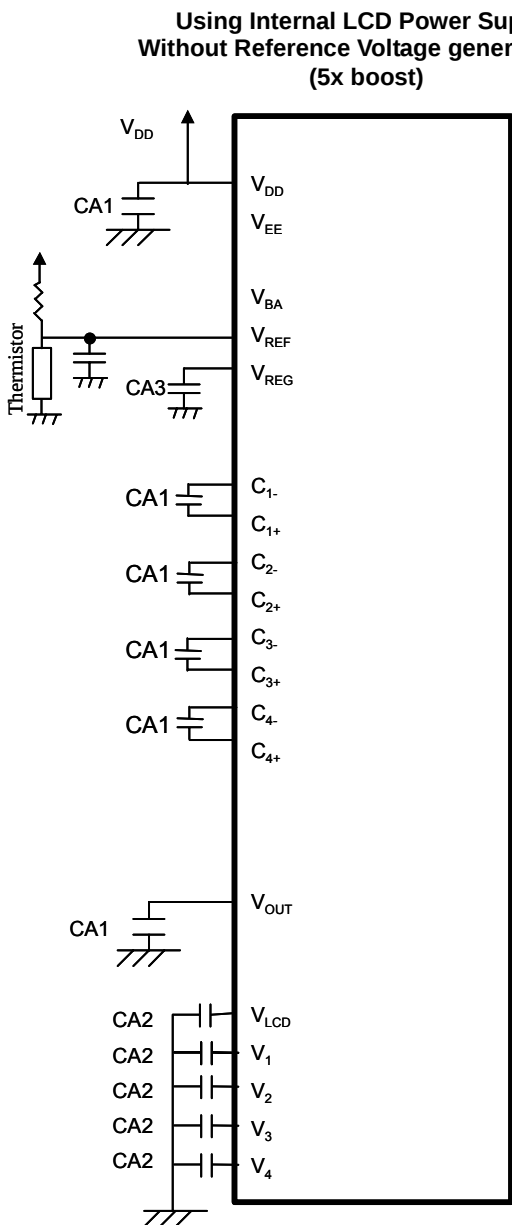


Fig 14

Reference Values

CA1	1.0 to 4.7 μ F
CA2	1.0 to 2.2 μ F
CA3	0.1 μ F

NOTE1) B grade capacitor is recommended for CA1-CA3. Make sure what is the best capacitor value in the particular application.

NOTE2) Parasitic resistance on the power supply lines (V_{DD} , V_{SS} , V_{EE} , V_{SSH} , V_{OUT} , V_{LCD} , V_1 , V_2 , V_3 and V_4) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, be sure to lay out the shortest wires and place capacitors as close to the LSI as possible.

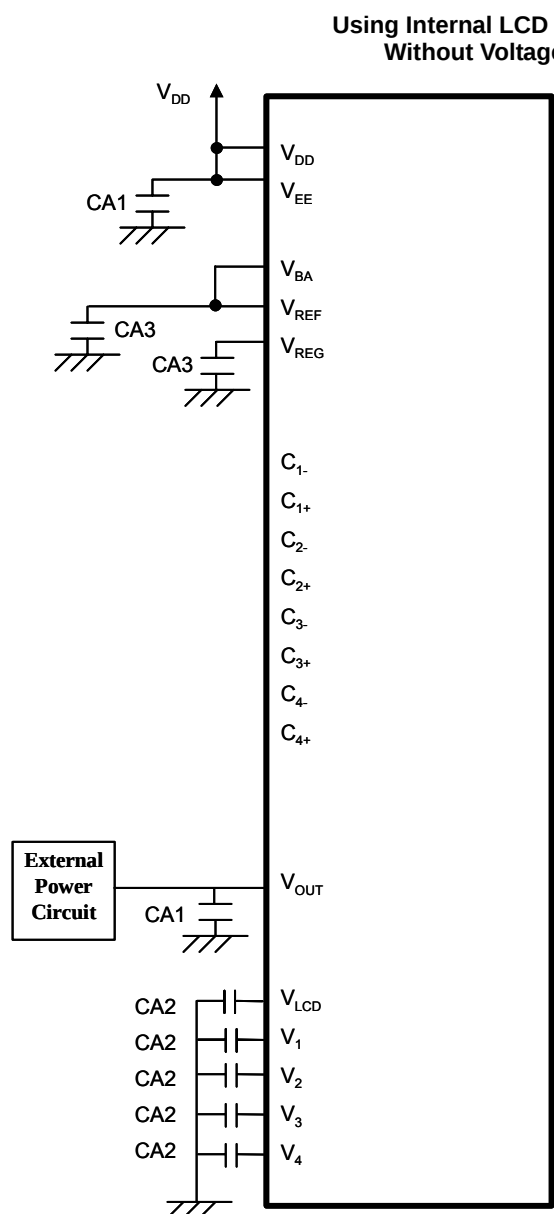


Fig 15

Reference Values

CA1	1.0 to 4.7 μ F
CA2	1.0 to 2.2 μ F
CA3	0.1 μ F

NOTE1) B grade capacitor is recommended for CA1-CA3. Make sure what is the best capacitor value in the particular application.

NOTE2) Parasitic resistance on the power supply lines (V_{DD} , V_{SS} , V_{EE} , V_{SSH} , V_{OUT} , V_{LCD} , V_1 , V_2 , V_3 and V_4) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, be sure to lay out the shortest wires and place capacitors as close to the LSI as possible.

(11-4) Discharge Circuit

The LSI incorporates two discharge circuits which are independently controlled for the V_{LCD} and V_1 - V_4 and for the V_{OUT} . The V_{LCD} and V_1 - V_4 are discharged by setting "1" at the D_0 (DIS) bit of the "Discharge ON/OFF" instruction or the reset by the RESb. And the V_{OUT} (100K Ω internal resistor between V_{OUT} and V_{EE}) is discharged by setting "1" at the D_1 (DIS2) bit of this instruction. Be sure to turned off the internal or external LCD power supply when this instruction is executed, otherwise it may function as a current load and affect an operating current. Refer to "(14-22) Discharge ON/OFF".

(11-5) Power ON/OFF

To protect the LSI from overcurrent, the following sequences must be maintained to turn on and off the power supply. In addition to the following discussions, refer to "(18) TYPICAL INSTRUCTION SEQUENCES".

(11-5-1) Power ON/OFF in Using Internal LCD Power Supply

Power ON

First " V_{DD} and V_{EE} ON", next "Reset by RESb", then "Internal LCD power supply ON". Be sure to execute the "Display ON" instruction later than the completion of this power ON sequence. Otherwise, unexpected pixels may be turned on instantly.

Power OFF

First "Reset by RESb or "HALT" instruction", next " V_{DD} and V_{EE} OFF". If using different power sources for the V_{DD} and the V_{EE} individually, the V_{EE} must be turned off after the reset or the "HALT". After that, the V_{DD} can be turned off, waiting until the LCD bias voltages (V_{LCD} , V_1 , V_2 , V_3 and V_4) drop below the threshold level of LCD pixels.

(11-5-2) Power ON/OFF in Using External LCD Power Supply

Power ON

First " V_{DD} and V_{EE} ON", next "Reset by RESb", then "External LCD power supply ON". When using only external V_{OUT} , first " V_{DD} ON", next "Reset by RESb", then "External V_{OUT} ON", as well.

Power OFF

First "Reset by RESb or "HALT" instruction" to isolate external LCD bias voltages, next " V_{DD} OFF". For more safety, placing a resistor in series on the V_{LCD} line (or the V_{OUT} line in using only the external V_{OUT}) is recommended. That resistance is usually between 50 Ω and 100 Ω .

(12) RESET FUNCTION

The reset function initializes the LSI to the following default status by setting the RESb to “L”. Connecting the RESb with MPU’s reset is recommended so that the LSI and MPU is initialized at a time.

Default Status

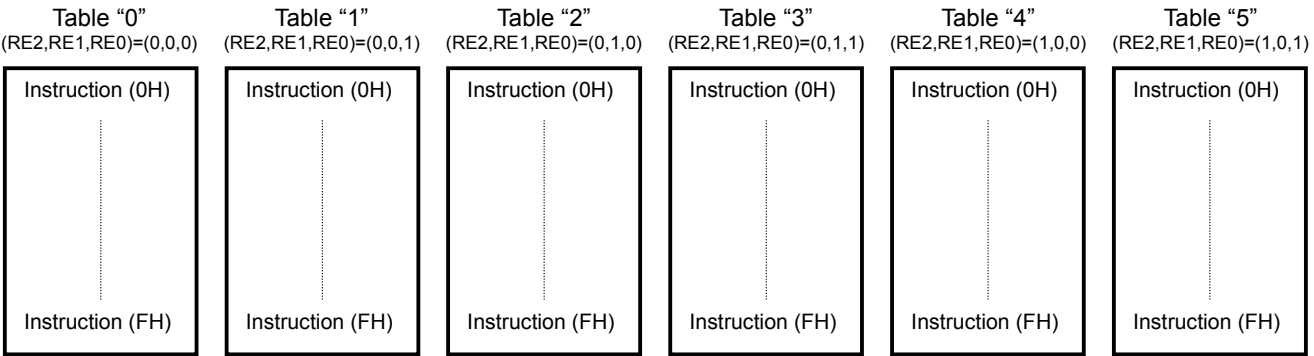
1. Display Data in DDRAM	:Undefined
2. Column Address	:(00)H
3. Row Address	:(00)H
4. Initial Display Line	:(0)H (1st line)
5. Display ON/OFF	:OFF
6. Reverse Display ON/OFF	:OFF (Normal)
7. Duty Cycle Ratio	:1/41Duty (DSE=0)
8. N-line Inversion ON/OFF	:OFF
9. COM Scan Direction	:COM ₀ → COM ₃₉
10. Increment Control	:Auto-increment OFF (AIM, AXI, AYI)=(0, 0, 0)
11. REF	:REF=0 (Normal)
12. Swap	:OFF (Normal)
13. EVR Value	:(0, 0, 0, 0, 0, 0, 0)
14. Internal LCD Power Supply	:OFF
15. Display Mode	:Grayscale Mode
16. LCD Bias Ratio	:1/8 Bias
17. Palette 0	:(0, 0, 0, 0, 0)
18. Palette 1	:(0, 0, 0, 1, 1)
19. Palette 2	:(0, 0, 1, 0, 1)
20. Palette 3	:(0, 0, 1, 1, 1)
21. Palette 4	:(0, 1, 0, 0, 1)
22. Palette 5	:(0, 1, 0, 1, 1)
23. Palette 6	:(0, 1, 1, 0, 1)
24. Palette 7	:(0, 1, 1, 1, 1)
25. Palette 8	:(1, 0, 0, 0, 1)
26. Palette 9	:(1, 0, 0, 1, 1)
27. Palette 10	:(1, 0, 1, 0, 1)
28. Palette 11	:(1, 0, 1, 1, 1)
29. Palette 12	:(1, 1, 0, 0, 1)
30. Palette 13	:(1, 1, 0, 1, 1)
31. Palette 14	:(1, 1, 1, 0, 1)
32. Palette 15	:(1, 1, 1, 1, 1)
33. Display Mode Control	:Variable 16-grayscale Mode (4,096 Colors)
34. Bus Length	:8-bit Bus Length
35. Discharge ON/OFF	:OFF (DIS2, DIS)=(0,0)

(13) INSTRUCTION TABLES

(13-1) Instruction Table and Register Address

The LSI incorporates 6 instruction tables as shown in Fig 16, and each instruction table has a specific address in between “0” and “5”. And each instruction register has a specific address in between (0H) and (FH), and instruction is read out from the register by the “Register Address” and “Register Read” instructions.

Fig 17 shows part of the instruction sequence, where the instruction table should be specified prior to other instructions. However, when some instructions of the same table are sequentially executed, the table selection may be omitted. In addition, the “Display Data Write”, “Display Data Read” and “Register Read” instructions can be performed in any table.



NOTE) Address (FH) is assigned to “Instruction Table Select” in any table.

Fig 16 Instruction Table Overview

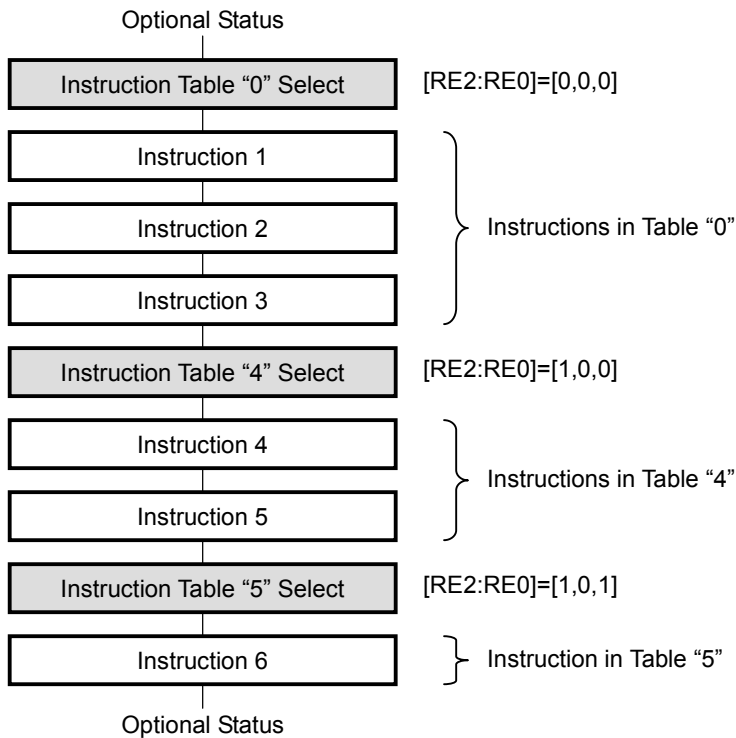


Fig 17 Outline of Instruction Sequence

(13-2) Instruction Table 0 (RE2, RE1, RE0)=(0, 0, 0)

Instructions/ Register Address [NH]		Code (80 Series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
1	Display Data Write	0	0	1	0	0/1	0/1	0/1	Write Data								Writing Display Data
2	Display Data Read	0	0	0	1	0/1	0/1	0/1	Read Data								Reading Display Data
3	Column Address (Lower) [0H]	0	1	1	0	0	0	0	0	0	0	0	AX3	AX2	AX1	AX0	Setting Column Address for start point
	Column Address (Upper) [1H]	0	1	1	0	0	0	0	0	0	0	1	AX7	AX6	AX5	AX4	Setting Column Address for start point
4	Row Address (Lower) [2H]	0	1	1	0	0	0	0	0	0	1	0	AY3	AY2	AY1	AY0	Setting Row Address for start point
	Row Address (Upper) [3H]	0	1	1	0	0	0	0	0	0	1	1	*	*	AY5	AY4	Setting Row Address for start point
5	Initial Display Line (Lower) [4H]	0	1	1	0	0	0	0	0	1	0	0	LA3	LA2	LA1	LA0	Setting Row Address for Initial COM
	Initial Display Line (Upper) [5H]	0	1	1	0	0	0	0	0	1	0	1	*	*	LA5	LA4	Setting Row Address for Initial COM
6	N-line Inversion (Lower) [6H]	0	1	1	0	0	0	0	0	1	1	0	N3	N2	N1	N0	Setting the Number of N-line Inversion
	N-line Inversion (Upper) [7H]	0	1	1	0	0	0	0	0	1	1	1	*	*	N5	N4	Setting the Number of N-line Inversion
7	Display Control (1) [8H]	0	1	1	0	0	0	0	1	0	0	0	SHIFT	MON	ALL ON	ON/ OFF	SHIFT : Common Scan Direction MON : Grayscale/B/W Mode ALLON : All Pixels ON/OFF ON/OFF : Display ON/OFF
8	Display Control (2) [9H]	0	1	1	0	0	0	0	1	0	0	1	REV	NLIN	SWAP	REF	REV : Reverse Display ON/OFF NLIN : N-line Inversion ON/OFF SWAP : SWAP ON/OFF REF : Segment Direction
9	Increment Control [AH]	0	1	1	0	0	0	0	1	0	1	0	WIN	AIM	AYI	AXI	WIN : Window Area ON/OFF AIM : Read-Modify-Write ON/OFF AYI : Row Increment AXI : Column Increment
10	Power Control [BH]	0	1	1	0	0	0	0	1	0	1	1	AMP ON	HALT	DC ON	ACL	AMPON : Voltage Converter ON/OFF HALT : Power Save ON/OFF DCON : Voltage Booster ON/OFF ACL : Reset
11	Duty Cycle Ratio [CH]	0	1	1	0	0	0	0	1	1	0	0	DS3	DS2	DS1	DS0	Setting LCD Duty Cycle Ratio
12	Boost Level [DH]	0	1	1	0	0	0	0	1	1	0	1	*	VU2	VU1	VU0	VU2-0 : Setting Boost Level
13	LCD Bias Ratio [EH]	0	1	1	0	0	0	0	1	1	1	0	*	B2	B1	B0	Setting LCD Bias Ratio
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table

NOTE1) * : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(13-3) Instruction Table 1 (RE2, RE1, RE0)=(0, 0, 1)

Instructions/ Register Address [NH]		Code (80 series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
15	Palette A0/A8 (Lower) [0H]	0	1	1	0	0	0	1	0	0	0	0	PA03/ PA83	PA02/ PA82	PA01/ PA81	PA00/ PA80	Setting Palette Data : A0(PS=0) /A8(PS=1)
	Palette A0/A8 (Upper) [1H]	0	1	1	0	0	0	1	0	0	0	1	*	*	*	PA04/ PA84	Setting Palette Data : A0(PS=0) /A8(PS=1)
	Palette A1/A9 (Lower) [2H]	0	1	1	0	0	0	1	0	0	1	0	PA13/ PA93	PA12/ PA92	PA11/ PA91	PA10/ PA90	Setting Palette Data : A1(PS=0) /A9(PS=1)
	Palette A1/A9 (Upper) [3H]	0	1	1	0	0	0	1	0	0	1	1	*	*	*	PA14/ PA94	Setting Palette Data : A1(PS=0) /A9(PS=1)
	Palette A2/A10 (Lower) [4H]	0	1	1	0	0	0	1	0	1	0	0	PA23/ PA103	PA22/ PA102	PA21/ PA101	PA20/ PA100	Setting Palette Data : A2(PS=0) /A10(PS=1)
	Palette A2/A10 (Upper) [5H]	0	1	1	0	0	0	1	0	1	0	1	*	*	*	PA24/ PA104	Setting Palette Data : A2(PS=0) /A10(PS=1)
	Palette A3/A11 (Lower) [6H]	0	1	1	0	0	0	1	0	1	1	0	PA33/ PA113	PA32/P A112	PA31/ PA111	PA30/ PA110	Setting Palette Data : A3(PS=0) /A11(PS=1)
	Palette A3/A11 (Upper) [7H]	0	1	1	0	0	0	1	0	1	1	1	*	*	*	PA34/ PA114	Setting Palette Data : A3(PS=0) /A11(PS=1)
	Palette A4/A12 (Lower) [8H]	0	1	1	0	0	0	1	1	0	0	0	PA43/ PA123	PA42/P A122	PA41/ PA121	PA40/ PA120	Setting Palette Data : A4(PS=0) /A12(PS=1)
	Palette A4/A12 (Upper) [9H]	0	1	1	0	0	0	1	1	0	0	1	*	*	*	PA44/ PA124	Setting Palette Data : A4(PS=0) /A12(PS=1)
	Palette A5/A13 (Lower) [AH]	0	1	1	0	0	0	1	1	0	1	0	PA53/ PA133	PA52/P A132	PA51/ PA131	PA50/ PA130	Setting Palette Data : A5(PS=0) /A13(PS=1)
	Palette A5/A13 (Upper) [BH]	0	1	1	0	0	0	1	1	0	1	1	*	*	*	PA54/ PA134	Setting Palette Data : A5(PS=0) /A13(PS=1)
	Palette A6/A14 (Lower) [CH]	0	1	1	0	0	0	1	1	1	0	0	PA63/ PA143	PA62/P A142	PA61/ PA141	PA60/ PA140	Setting Palette Data : A6(PS=0) /A14(PS=1)
	Palette A6/A14 (Upper) [DH]	0	1	1	0	0	0	1	1	1	0	1	*	*	*	PA64/ PA144	Setting Palette Data : A6(PS=0) /A14(PS=1)
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table

NOTE1) * : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(13-4) Instruction Table 2 (RE2, RE1, RE0)=(0, 1, 0)

Instructions/ Register Address [NH]		Code (80 series MPU I/F)							Code								Functions	
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
15	Palette A7/A15 (Lower) [0H]	0	1	1	0	0	1	0	0	0	0	0	PA73/ PA153	PA72/P A152	PA71/ PA151	PA70/ PA150	Setting Palette Data : A7(PS=0) /A15(PS=1)	
	Palette A7/A15 (Upper) [1H]	0	1	1	0	0	1	0	0	0	0	1	*	*	*	PA74/ PA154	Setting Palette Data : A7(PS=0) /A15(PS=1)	
	Palette B0/B8 (Lower) [2H]	0	1	1	0	0	1	0	0	0	1	0	PB03/ PB83	PB02/ PB82	PB01/ PB81	PB00/ PB80	Setting Palette Data : B0(PS=0) /B8(PS=1)	
	Palette B0/B8 (Upper) [3H]	0	1	1	0	0	1	0	0	0	1	1	*	*	*	PB04/ PG84	Setting Palette Data : B0(PS=0) /B8(PS=1)	
	Palette B1/B9 (Lower) [4H]	0	1	1	0	0	1	0	0	1	0	0	PB13/ PB93	PB12/ PB92	PB11/ PB91	PB10/ PB90	Setting Palette Data : B1(PS=0) /B9(PS=1)	
	Palette B1/B9 (Upper) [5H]	0	1	1	0	0	1	0	0	1	0	1	*	*	*	PB14/ PB94	Setting Palette Data : B1(PS=0) /B9(PS=1)	
	Palette B2/B10 (Lower) [6H]	0	1	1	0	0	1	0	0	1	1	0	PB23/ PB103	PB22/ PB102	PB21/ PB101	PB20/ PB100	Setting Palette Data : B2(PS=0) /B10(PS=1)	
	Palette B2/B10 (Upper) [7H]	0	1	1	0	0	1	0	0	1	1	1	*	*	*	PB24/ PB104	Setting Palette Data : B2(PS=0) /B10(PS=1)	
	Palette B3/B11 (Lower) [8H]	0	1	1	0	0	1	0	1	0	0	0	0	PB33/ PB113	PB32/ PB112	PB31/ PB111	PB30/ PB110	Setting Palette Data : B3(PS=0) /B11(PS=1)
	Palette B3/B11 (Upper) [9H]	0	1	1	0	0	1	0	1	0	0	1	*	*	*	PB34/ PB114	Setting Palette Data : B3(PS=0) /B11(PS=1)	
	Palette B4/B12 (Lower) [AH]	0	1	1	0	0	1	0	1	0	1	0	0	PB43/ PB123	PB42/ PB122	PB41/ PB121	PB40/ PB120	Setting Palette Data : B4(PS=0) /B12(PS=1)
	Palette B4/B12 (Upper) [BH]	0	1	1	0	0	1	0	1	0	1	1	*	*	*	PB44/ PB124	Setting Palette Data : B4(PS=0) /B12(PS=1)	
	Palette B5/B13 (Lower) [CH]	0	1	1	0	0	1	0	1	1	0	0	0	PB53/ PB133	PB52/ PB132	PB51/ PB131	PB50/ PB130	Setting Palette Data : B5(PS=0) /B13(PS=1)
	Palette B5/B13 (Upper) [DH]	0	1	1	0	0	1	0	1	1	0	1	*	*	*	PB54/ PB134	Setting Palette Data : B5(PS=0) /B13(PS=1)	
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Tablet	

NOTE1) * : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(13-5) Instruction Table 3 (RE2, RE1, RE0)=(0, 1, 1)

Instructions/ Register Address [NH]		Code (80 series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
15	Palette B6/B14 (Lower) [0H]	0	1	1	0	0	1	1	0	0	0	0	PB63/ PB143	PB62/ PB142	PB61/ PB141	PB60/ PB140	Setting Palette Data : B6(PS=0) /B14(PS=1)
	Palette B6/B14 (Upper) [1H]	0	1	1	0	0	1	1	0	0	0	1	*	*	*	PB64/ PB144	Setting Palette Data : B6(PS=0) /B14(PS=1)
	Palette B7/B15 (Lower) [2H]	0	1	1	0	0	1	1	0	0	1	0	PB73/ PB153	PB72/ PB152	PB71/ PB151	PB70/ PB150	Setting Palette Data : B7(PS=0) /B15(PS=1)
	Palette B7/B15 (Upper) [3H]	0	1	1	0	0	1	1	0	0	1	1	*	*	*	PB74/ PB154	Setting Palette Data : B7(PS=0) /B15(PS=1)
	Palette C0/C8 (Lower) [4H]	0	1	1	0	0	1	1	0	1	0	0	PC03/ PC83	PC02/ PC82	PC01/ PC81	PC00/ PC80	Setting Palette Data : C0(PS=0) /C8(PS=1)
	Palette C0/C8 (Upper) [5H]	0	1	1	0	0	1	1	0	1	0	1	*	*	*	PC04/ PC84	Setting Palette Data : C0(PS=0) /C8(PS=1)
	Palette C1/C9 (Lower) [6H]	0	1	1	0	0	1	1	0	1	1	0	PC13/ PC93	PC12/ PC92	PC11/ PC91	PC10/ PC90	Setting Palette Data : C1(PS=0) /C9(PS=1)
	Palette C1/C9 (Upper) [7H]	0	1	1	0	0	1	1	0	1	1	1	*	*	*	PC14/ PC94	Setting Palette Data : C1(PS=0) /C9(PS=1)
	Palette C2/C10 (Lower) [8H]	0	1	1	0	0	1	1	1	0	0	0	PC23/ PC103	PC22/ PC102	PC21/ PC101	PC20/ PC100	Setting Palette Data : C2(PS=0) /C10(PS=1)
	Palette C2/C10 (Upper) [9H]	0	1	1	0	0	1	1	1	0	0	1	*	*	*	PC24/ PC104	Setting Palette Data : C2(PS=0) /C10(PS=1)
	Palette C3/C11 (Lower) [AH]	0	1	1	0	0	1	1	1	0	1	0	PC33P C113	PC32/ PC112	PC31/ PC111	PC30/ PC110	Setting Palette Data : C3(PS=0) /C11(PS=1)
	Palette C3/C11 (Upper) [BH]	0	1	1	0	0	1	1	1	0	1	1	*	*	*	PC34/ PC114	Setting Palette Data : C3(PS=0) /C11(PS=1)
	Palette C4/C12 (Lower) [CH]	0	1	1	0	0	1	1	1	1	1	0	PC43/ PC123	PC42/ PC122	PC41/ PC121	PC40/ PC120	Setting Palette Data : C4(PS=0) /C12(PS=1)
	Palette C4/C12 (Upper) [DH]	0	1	1	0	0	1	1	1	1	1	0	1	*	*	*	PC44/ PC124
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table

NOTE1) * : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(13-6) Instruction Table 4 (RE2, RE1, RE0)=(1, 0, 0)

Instructions/ Register Address [NH]		Code (80 series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
15	Palette C5/C13 (Lower) [0H]	0	1	1	0	1	0	0	0	0	0	0	PC53/ PC133	PC52/ PC132	PC51/ PC131	PC50/ PC130	Setting Palette Data : C5(PS=0) /C13(PS=1)
	Palette C5/C13 (Upper) [1H]	0	1	1	0	1	0	0	0	0	0	1	*	*	*	PC54/ PC134	Setting Palette Data : C5(PS=0) /C13(PS=1)
	Palette C6/C14 (Lower) [2H]	0	1	1	0	1	0	0	0	0	1	0	PC63/P C143	PC62/ PC142	PC61/ PC141	PC60/ PC140	Setting Palette Data : C6(PS=0) /C14(PS=1)
	Palette C6/C14 (Upper) [3H]	0	1	1	0	1	0	0	0	0	1	1	*	*	*	PC64/ PC144	Setting Palette Data : C6(PS=0) /C14(PS=1)
	Palette C7/C15 (Lower) [4H]	0	1	1	0	1	0	0	0	1	0	0	PC73/ PC153	PC72/ PC152	PC71/ PC151	PC70/ PC150	Setting Palette Data : C7(PS=0) /C15(PS=1)
	Palette C7/C15 (Upper) [5H]	0	1	1	0	1	0	0	0	1	0	1	*	*	*	PC74/ PC154	Setting Palette Data : C7(PS=0) /C15(PS=1)
16	Initial COM [6H]	0	1	1	0	1	0	0	0	1	1	0	SC3	SC2	SC1	SC0	Setting start COM for scanning
17	Duty-1 /Display Clock ON/OFF [7H]	0	1	1	0	1	0	0	0	1	1	1	*	*	DSE	SON	SON : Display Clock ON/OFF DSE : Duty-1 ON/OFF
18	Display Mode Control [8H]	0	1	1	0	1	0	0	1	0	0	0	PWM	C256	*	*	PWM : Variable/Fixed Grayscale Mode C256 : 256-color Mode ON/OFF.
19	Bus Length [9H]	0	1	1	0	1	0	0	1	0	0	1	HSW	ABS	CKS	WLS	HSW : High Speed Writing ABS : Bit Assignment CKS : Oscillator Set WLS : 8-/16-bit Bus Length
20	EVR Control (Lower) [AH]	0	1	1	0	1	0	0	1	0	1	0	DV3	DV2	DV1	DV0	Setting EVR Value (Lower Bit)
	EVR Control (Upper) [BH]	0	1	1	0	1	0	0	1	0	1	1	*	DV6	DV5	DV4	Setting EVR Value (Upper Bit)
21	Frequency Control [DH]	0	1	1	0	1	0	0	1	1	0	1	*	RF2	RF1	RF0	Adjusting Oscillation Frequency
22	Discharge ON/OFF [EH]	0	1	1	0	1	0	0	1	1	1	0	*	*	DIS2	DIS	Discharge ON/OFF
23	Register Address [CH]	0	1	1	0	1	0	0	1	1	0	0	Register Address				Setting Register Address
24	Register Read	0	1	0	1	0/1	0/1	0/1					Read Data				Reading Instruction
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table Select

NOTE1) * : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(13-7) Instruction Table 5 (RE2, RE1, RE0)=(1, 0, 1)

Instructions/ Register Address [NH]		Code (80 series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
25	Window End Column Address (Lower) [0H]	0	1	1	0	1	0	1	0	0	0	0	EX3	EX2	EX1	EX0	Setting Column Address for end point
	Window End Column Address (Upper) [1H]	0	1	1	0	1	0	1	0	0	0	1	EX7	EX6	EX5	EX4	Setting Column Address for end point
26	Window End Row Address (Lower) [2H]	0	1	1	0	1	0	1	0	0	1	0	EY3	EY2	EY1	EY0	Setting Row Address for end point
	Window End Row Address (Upper) [3H]	0	1	1	0	1	0	1	0	0	1	1	*	*	EY5	EY4	Setting Row Address for end point
27	Initial Line-reverse Address (Lower) [4H]	0	1	1	0	1	0	1	0	1	0	0	LS3	LS2	LS1	LS0	Setting Start Line for Line-reverse Display
	Initial Line-reverse Address (Upper) [5H]	0	1	1	0	1	0	1	0	1	0	1	*	*	LS5	LS4	Setting Start Line for Line-reverse Display
28	Last Line-reverse Address (Lower) [6H]	0	1	1	0	1	0	1	0	1	1	0	LE3	LE2	LE1	LE0	Setting End Line for Line-reverse Display
	Last Line-reverse Address (Upper) [7H]	0	1	1	0	1	0	1	0	1	1	1	*	*	LE5	LE4	Setting End Line for Line-reverse Display
29	Line Reverse ON/OFF [8H]	0	1	1	0	1	0	1	1	0	0	0	*	*	BT	LREV	BT : Blink Set LREV : Line-reverse ON/OFF
30	Upper/Lower Palette Select [9H]	0	1	1	0	1	0	1	1	0	0	1	*	*	*	PS	PS : Upper/Lower Palette Register
31	PWM Control [AH]	0	1	1	0	1	0	1	1	0	1	0	PWMS	PWMA	PWMB	PWMC	Setting PWM Mode
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table

NOTE1) * : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(14) INSTRUCTION DESCRIPTIONS

This chapter provides detailed descriptions about each instruction. These descriptions are written with the assumption that 80-series MPU is used. When using 68-series MPU, the polarities of the E and R/W signals differ from those of the RDb and WRb signals.

(14-1) Display Data Write

The “Display Data Write” instruction writes display data on a specified DDRAM address.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	0	1	0	0/1	0/1	0/1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Display Data							

(14-2) Display Data Read

The “Display Data Read” instruction reads out display data from a specified DDRAM address. One dummy read is necessary right after DDRAM address setting.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	0	0	1	0/1	0/1	0/1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Display Data							

(14-3) Column Address

The “Column Address” instruction specifies the column address of the start point. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	AX3	AX2	AX1	AX0

(Default: AX3-AX0=0H / Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	AX7	AX6	AX5	AX4

(Default: AX7-AX4=0H / Register Address: 1H)

(14-4) Row Address

The “Row Address” instruction specifies the row address of the start point. Available setting range is from (00H) to (27H), and outside this range is not allowed. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	AY3	AY2	AY1	AY0

(Default: AY3-AY0=0H / Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	AY5	AY4

(Default: AY5-AY4=0H / Register Address: 3H)

(14-5) Initial Display Line

This instruction sets the row address, which corresponds to an initial COM and is normally positioned on top of a screen in full display. For more information, refer to “(14-16) Initial COM”. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	LA3	LA2	LA1	LA0

(Default: LA3-LA0=0H / Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	LA5	LA4

(Default: LA5-LA4=0H / Register Address: 5H)

Table 18 Initial Display Line Address

LA ₅	LA ₄	LA ₃	LA ₂	LA ₁	LA ₀	Line Address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
⋮						⋮
1	0	0	1	1	1	39

(14-6) N-line Inversion

The number of N line is selected in between “2” and “40”. When the N-line inversion is enabled by setting “1” at the D₂ (NLIN) bit of the “Display Control (2)” instruction, the FR toggles once every N lines. When the N-line inversion is disabled by setting “0” at this bit, the FR toggles by the frame.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	N3	N2	N1	N0

(Default: N3-N0=0H / Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	N5	N4

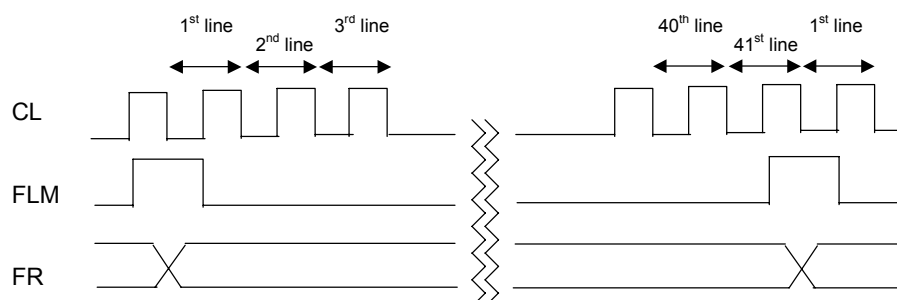
(Default: N5-N4=0H / Register Address: 7H)

Table 19 N-line Inversion

N ₅	N ₄	N ₃	N ₂	N ₁	N ₀	N value
0	0	0	0	0	0	Inhibited*
0	0	0	0	0	1	2
⋮						⋮
1	0	0	1	1	1	40

NOTE1) N Line=(N Value)+1

N-line inversion OFF



N-line inversion ON

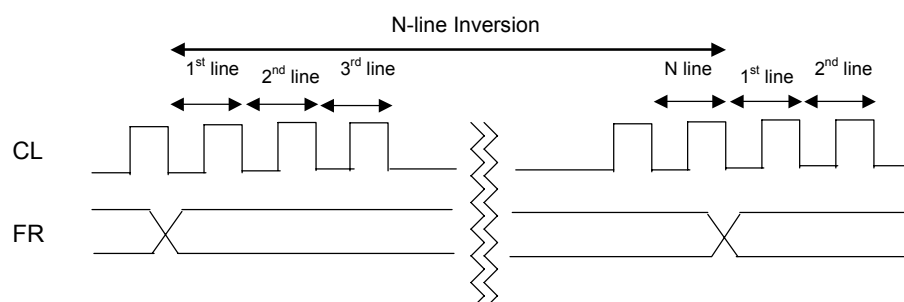


Fig 18 N-line Inversion Timing (1/41 Duty)

(14-7) Display Control (1)

The “Display Control (1)” instruction controls display conditions.

CSb	RS	RDb	WRb	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	0	0	0	1	0	0	0	SHIFT	MON	ALL ON	ON /OFF

(Default: [SHIFT,MON,ALLON,ON/OFF]=0H / Register Address: 8H)

D₀ (ON/OFF)

ON/OFF=0 : Display OFF (All COM/SEG fixed at V_{SSH} level)
ON/OFF=1 : Display ON

D₁ (ALLON)

This bit forcibly turns on all pixels regardless of display data. This bit has a priority over the “REV” bit of the “Display Control (2)” instruction.

ALLON=0 : Normal
ALLON=1 : All pixels ON

D₂ (MON)

MON=0 : Grayscale Mode (Variable 16-grayscale, Variable 8-grayscale or Fixed 8-grayscale Mode)
MON=1 : B&W Mode

D₃ (SHIFT)

SHIFT=0 : COM₀ → COM₃₉
SHIFT=1 : COM₀ ← COM₃₉

(14-8) Display Control (2)

The “Display Control (2)” instruction controls display conditions.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	REV	NLIN	SWAP	REF

(Default: [REV,NLIN,SWAP,REF]=0H / Register Address: 9H)

D₀ (REF)

This bit controls the DDRAM access direction which reverses the segment direction for reducing the restrictions on the IC position of an LCD module. For more information, refer to “(16) SWAP FUNCTION”.

D₁ (SWAP)

This bit swaps palettes A_j and palettes C_j (j=0-15). This function reduces the restrictions on the IC position of an LCD module. Refer to “(16) SWAP FUNCTION”.

SWAP=0 : SWAP OFF
SWAP=1 : SWAP ON

D₂ (NLIN)

This bit enables the N-line inversion.

NLIN=0 : N-line Inversion OFF (FR toggles by the frame.)
NLIN=1 : N-line Inversion ON (FR toggles once every N lines.)

D₃ (REV)

This bit enables the reverse display function that reverses the polarities of all display data without changing the DDRAM.

REV=0 : Reverse Display OFF (Normal)
REV=1 : Reverse Display ON

Table 20 Reverse Display ON/OFF

REV	Display	DDRAM Data → Display Data	
0	Normal	0	0
		1	1
1	Reverse	0	1
		1	0

(14-9) Increment Control

The “AIM”, “AYI” and “AXI” bits set an auto-increment operation to the column address and row address individually. Once this mode is set up, the column address, row address or both are automatically counted up, whenever the DDRAM is accessed. The “WIN” bits enables/disables the window area access.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	WIN	AIM	AYI	AXI

(Default: [WIN,AIM,AYI,AXI]=0H / Register Address: AH)

D₂ (AIM)

Table 21 Read-modify-write ON/OFF

AIM	Increment Mode	NOTE
0	Read-modify-write OFF	1
1	Read-modify-write ON	2

NOTE1) Increment in writing and reading display data

NOTE2) Increment in writing display data only

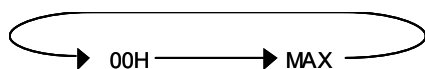
D₁, D₀ (AYI, AXI)

Table 22 Column/Row Increment

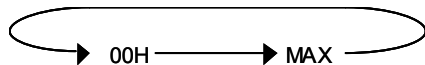
AYI	AXI	Column/Row Increment	NOTE
0	0	Non Increment	1
0	1	Column Address Increment	2
1	0	Row Address Increment	3
1	1	Column & Row Addresses Increment	4

NOTE1) Non increment. The “AIM” bit is disabled.

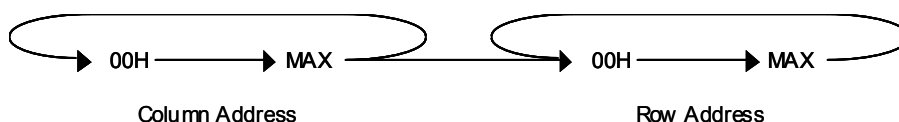
NOTE2) Increment operation of column address. The “AIM” bit is enabled.



NOTE3) Row address increment. The “AIM” bit is enabled.



NOTE4) Column & row addresses increment. The “AIM” bit is enabled.

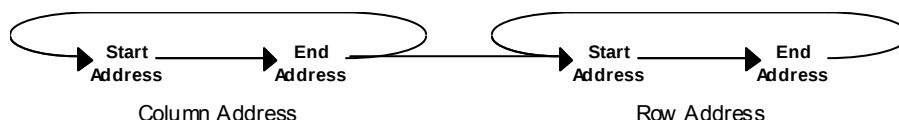


D₃ (WIN)

The window access should be enabled (WIN=1) in combination with the auto-increment operation (AXI=1, AYI=1). The typical sequence of the window area setting is discussed in “(4-2) Window Area for DDRAM Access”.

WIN=0 : Window Area Access OFF (Normal DDRAM Access)

WIN=1 : Window Area Access ON



(14-10) Power Control

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	AMPON	HALT	DCON	ACL

(Default: [AMPON,HALT,DCON,ACL]=0H / Register Address: BH)

D₀ (ACL)

This bit initializes the internal LCD power supply.

ACL=0 : Initialization OFF (Normal)
 ACL=1 : Initialization ON

NOTE) During the initialization, "1" is read out as the status of the "ACL" bit by the "Register Read" instruction. After the initialization, it is "0". As the CLK triggers the initialization, the "wait time" at least equivalent to 2 cycles of the CLK is required for the next instruction.

D₁ (DCON)

The "DCON" bit activates the voltage booster.

DCON=0 : Voltage Booster OFF
 DCON=1 : Voltage Booster ON

D₂ (HALT)

The "HALT" bit enables the power save mode. During the power save, operating current is down to the stand-by level. The internal state of the LSI in the power save mode is listed below.

HALT=0 : Power Save OFF (Normal)
 HALT=1 : Power Save ON

Internal State in Power Save Mode (HALT="1")

- Internal oscillator and internal LCD power supply are halted.
- All segment and common drivers are fixed at V_{SSH} level.
- External clock to the OSC1 cannot be accepted.
- Display data in the DDRAM is being maintained.
- Data in the instruction registers are being maintained.
- V_{LCD}, V₁, V₂, V₃ and V₄ are in high impedance.

NOTE) In the power save ON sequence, execute the "Display OFF" prior to the "Power Save ON". In the power save OFF sequence, execute the "Power save OFF" prior to the "Display ON". If the "Power Save ON/OFF" instruction is executed during the "Display ON", unexpected pixels may be turned on instantly.

D₃ (AMPON)

The "AMPON" bit activates the voltage converter which includes the reference voltage generator, the voltage regulator and the LCD bias generator.

AMPON=0 : Voltage Converter OFF
 AMPON=1 : Voltage Converter ON

(14-11) Duty Cycle Ratio

The “Duty Cycle Ratio” instruction selects LCD duty cycle ratio, and is used to carry out the partial display in combination with other instructions such as the “Boost Level”, the “LCD Bias Ratio” and the “EVR Control”.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	DS3	DS2	DS1	DS0

(Default: DS3-DS0=0H / Register Address: CH)

Table 23 Duty Cycle Ratio

DS ₃	DS ₂	DS ₁	DS ₀	Duty cycle ratio		# of Commons
				DSE=0	DSE=1	
0	0	0	0	1/41	1/40	40 commons
0	0	0	1	1/37	1/36	36 commons
0	0	1	0	1/33	1/32	32 commons
0	0	1	1	1/29	1/28	28 commons
0	1	0	0	1/25	1/24	24 commons
0	1	0	1	1/21	1/20	20 commons
0	1	1	0	1/17	1/16	16 commons
0	1	1	1	1/13	1/12	12 commons
1	0	0	0	1/9	1/8	8 commons
1	0	0	1	1/5	1/4	4 commons
1	0	1	0	Inhibited		
1	0	1	1	Inhibited		
1	1	0	0	Inhibited		
1	1	0	1	Inhibited		
1	1	1	0	Inhibited		
1	1	1	1	Inhibited		

NOTE) Duty cycle ratio is subtracted by 1 (Duty-1) from the original duty cycle ratio by setting “1” at the D₁ (DSE) bit of the “Duty-1 ON/OFF” instruction. Refer to “(14-17) Duty-1 /Display Clock ON/OFF”.

(14-12) Boost Level

The “Boost Level” selects the multiple of the voltage booster.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	VU2	VU1	VU0

(Default: VU2-VU0=0H / Register Address: DH)

D₂, D₁, D₀ (VU2, VU1, VU0)

Table 24 Boost Level

VU2	VU1	VU0	Boost Level
0	0	0	1 time (No boost)
0	0	1	2 times
0	1	0	3 times
0	1	1	4 times
1	0	0	5 times
1	0	1	Inhibited
1	1	0	Inhibited
1	1	1	Inhibited

(14-13) LCD Bias Ratio

The “LCD bias ratio” selects LCD bias ratio.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	1	0	*	B2	B1	B0

(Default: B2-B0=0H / Register Address: EH)

Table 25 LCD Bias Ratio

B2	B1	B0	LCD Bias Ratio
0	0	0	1/8
0	0	1	1/7
0	1	0	1/6
0	1	1	1/5
1	0	0	1/4
1	0	1	Inhibited
1	1	0	Inhibited
1	1	1	Inhibited

(14-14) Instruction Table Select

This instruction specifies an instruction table, and should be executed prior to other instructions.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0/1	0/1	0/1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	1	1	TST0	RE2	RE1	RE0

(Default: TST0, RE2-RE0=0H / Register Address: FH)

Table 26 Instruction Table Select

RE2	RE1	RE0	Instructions
0	0	0	Instruction Table (0)
0	0	1	Instruction Table (1)
0	1	0	Instruction Table (2)
0	1	1	Instruction Table (3)
1	0	0	Instruction Table (4)
1	0	1	Instruction Table (5)

NOTE) “TST0” bit must be “0”. This is used for maker tests only.

(14-15) Palette A / B / C

Palette A0 (PS=0) / Palette A8 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

(Register Address: 0H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PA03/ PA83	PA02/ PA82	PA01/ PA81	PA00/ PA80

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PA04/ PA84

(Register Address: 1H)

Palette A1 (PS=0) / Palette A9 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PA13/ PA93	PA12/ PA92	PA11/ PA91	PA10/ PA90

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PA14/ PA94

(Register Address: 3H)

Palette A2 (PS=0) / Palette A10 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PA23/ PA103	PA22/ PA102	PA21/ PA101	PA20/ PA100

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PA24/ PA104

(Register Address: 5H)

Palette A3 (PS=0) / Palette A11 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	PA33/ PA113	PA32/ PA112	PA31/ PA111	PA30/ PA110

(Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	*	PA34/ PA114

(Register Address: 7H)

Palette A4 (PS=0) / Palette A12 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PA43/ PA123	PA42/ PA122	PA41/ PA121	PA40/ PA120

(Register Address: 8H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	*	PA44/ PA124

(Register Address: 9H)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette A5 (PS=0) / Palette A13 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	PA53/ PA133	PA52/ PA132	PA51/ PA131	PA50/ PA130

(Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	*	*	PA54/ PA134

(Register Address: BH)

Palette A6 (PS=0) / Palette A14 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	PA63/ PA143	PA62/ PA142	PA61/ PA141	PA60/ PA140

(Register Address: CH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	*	*	PA64/ PA144

(Register Address: DH)

Palette A7 (PS=0) / Palette A15 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PA73/ PA153	PA72/ PA152	PA71/ PA151	PA70/ PA150

(Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PA74/ PA154

(Register Address: 1H)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette B0 (PS=0) / Palette B8 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PB03/ PB83	PB02/ PB82	PB01/ PB81	PB00/ PB80

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PB04/ PB84

(Register Address: 3H)

Palette B1 (PS=0) / Palette B9 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PB13/ PB93	PB12/ PB92	PB11/ PB91	PB10/ PB90

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PB14/ PB94

(Register Address: 5H)

Palette B2 (PS=0) / Palette B10 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	PB23/ PB103	PB22/ PB102	PB21/ PB101	PB20/ PB100

(Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	*	PB24/ PB104

(Register Address: 7H)

Palette B3 (PS=0) / Palette B11 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PB33/ PB113	PB32/ PB112	PB31/ PB111	PB30/ PB110

(Register Address: 8H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	*	PB34/ PB114

(Register Address: 9H)

Palette B4 (PS=0) / Palette B12 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	PB43/ PB123	PB42/ PB122	PB41/ PB121	PB40/ PB120

(Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	*	*	PB44/ PB124

(Register Address: BH)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette B5 (PS=0) / Palette B13 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	PB53/ PB133	PB52/ PB132	PB51/ PB131	PB50/ PB130

(Register Address: CH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	*	*	PB54/ PB134

(Register Address: DH)

Palette B6 (PS=0) / Palette B14 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PB63/ PB143	PB62/ PB142	PB61/ PB141	PB60/ PB140

(Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PB64/ PB144

(Register Address: 1H)

Palette B7 (PS=0) / Palette B15 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PB73/ PB153	PB72/ PB152	PB71/ PB151	PB70/ PB150

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PB74/ PB154

(Register Address: 3H)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette C0 (PS=0) / Palette C8 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PC03/ PC83	PC02/ PC82	PC01/ PC81	PC00/ PC80

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PC04/ PC84

(Register Address: 5H)

Palette C1 (PS=0) / Palette C9 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	PC13/ PC93	PC12/ PC92	PC11/ PC91	PC10/ PC90

(Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	*	PC14/ PC94

(Register Address: 7H)

Palette C2 (PS=0) / Palette C10 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PC23/ PC103	PC22/ PC102	PC21/ PC101	PC20/ PC100

(Register Address: 8H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	*	PC24/ PC104

(Register Address: 9H)

Palette C3 (PS=0) / Palette C11 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	PC33/ PC113	PC32/ PC112	PC31/ PC111	PC30/ PC110

(Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	*	*	PC34/ PC114

(Register Address: BH)

Palette C4 (PS=0) / Palette C12 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	PC43/ PC123	PC42/ PC122	PC41/ PC121	PC40/ PC120

(Register Address: CH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	*	*	PC44/ PC124

(Register Address: DH)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette C5 (PS=0) / Palette C13 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PC53/ PC133	PC52/ PC132	PC51/ PC131	PC50/ PC130

(Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PC54/ PC134

(Register Address: 1H)

Palette C6 (PS=0) / Palette C14 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PC63/ PC143	PC62/ PC142	PC61/ PB141	PC60/ PB140

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PC64/ PC144

(Register Address: 3H)

Palette C7 (PS=0) / Palette C15 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PC73/ PC153	PC72/ PC152	PC71/ PC151	PC70/ PC150

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PC74/ PC154

(Register Address: 5H)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

(14-16) Initial COM

The “Initial COM” instruction specifies the common driver for a scan start common.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	SC3	SC2	SC1	SC0

(Default: SC3-SC0=0H / Register Address: 6H)

Table 27 Initial COM

SC3	SC2	SC1	SC0	Initial COM (SHIFT=0)	Initial COM (SHIFT=1)
0	0	0	0	COM ₀	COM ₃₉
0	0	0	1	COM ₄	COM ₃₅
0	0	1	0	COM ₈	COM ₃₁
0	0	1	1	COM ₁₂	COM ₂₇
0	1	0	0	COM ₁₆	COM ₂₃
0	1	0	1	COM ₂₀	COM ₁₉
0	1	1	0	COM ₂₄	COM ₁₅
0	1	1	1	COM ₂₈	COM ₁₁
1	0	0	0	COM ₃₂	COM ₇
1	0	0	1	COM ₃₆	COM ₃
1	0	1	0	Inhibited	Inhibited
1	0	1	1	Inhibited	Inhibited
1	1	0	0	Inhibited	Inhibited
1	1	0	1	Inhibited	Inhibited
1	1	1	0	Inhibited	Inhibited
1	1	1	1	Inhibited	Inhibited

(14-17) Duty-1 /Display Clock ON/OFF

This instruction controls ON (Duty-1) /OFF (Duty-0) and Display Clock ON/OFF.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	DSE	SON

(Default: SON,DSE=0H / Register Address: 7H)

D₀ (SON)

SON=0 : CL, FLM, FR, and CLK are fixed at “L” level.

SON=1 : CL, FLM, FR, and CLK are enabled.

D₁ (DSE)

The duty cycle ratio is subtracted by 1 (Duty-1) from the original duty cycle ratio by setting “1” at the “DSE” bit.

DSE=0 : OFF (Duty-0)

DSE=1 : ON (Duty-1)

NOTE) For the last common timing at “DSE=0”, all common drivers generate non-selective waveforms, and segment drivers generate the same waveforms as for the previous common timing. For instance, in 1/41 duty cycle, the segment waveforms for 41st common timing are the same as for 40th common timing (last line).

(14-18) Display Mode Control

The “Display Mode Control” instruction sets up display modes such as the variable or fixed grayscale mode and the variable 8- or 16-grayscale mode. The D₂ (MON) bit of the “Display Control (1)” is used in combination. Refer to “(5) GRAY SCALE CONTROL CIRCUIT” and “(14-7) Display Control (1).”

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PWM	C256	*	*

(Default: PWM,C256=0H / Register Address: 8H)

D₃ (PWM)

PWM=0 : Variable grayscale Mode (Variable 8-/16-grayscale Mode)

PWM=1 : Fixed 8-grayscale Mode

D₂ (C256)

C256=0 : Variable 16-grayscale Mode at “PWM=0” (4096 colors)
 C256=1 : Variable 8-grayscale Mode at “PWM=0” (256 colors)

(14-19) Bus Length

This instruction selects 8- or 16-bit bus length, and sets oscillator configuration, ABS mode ON/OFF and high speed writing ON/OFF as well.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	HSW	ABS	CKS	WLS

(Default: HSW,ABS,CKS,WLS=0H / Register Address: 9H)

D₀ (WLS)

WLS=0: 8-bit Bus Length
 WLS=1: 16-bit Bus Length

D₁ (CKS)

CKS =0: Internal Oscillator using an internal resistor
 CKS =1: External Clock, or Internal Oscillator using an external resistor

NOTE) Refer to “(10) OSCILLATOR”.

D₂ (ABS)

ABS=0: ABS Mode OFF (Normal)
 ABS=1: ABS Mode ON

D₃ (HSW)

HSW=0: High Speed Writing OFF (Normal)
 HSW=1: High Speed Writing ON

(14-20) EVR Control

The “EVR Control” instruction adjusts V_{LCD} to optimize display contrast. This instruction is finally effective when both upper and lower bytes are transmitted in order to prevent high V_{LCD} . The setting order is upper byte first, then lower byte. Refer to “(11-2-3) Electrical Variable Resistor (EVR)”.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	DV ₃	DV ₂	DV ₁	DV ₀

(Default: DV₃-DV₀=0H / Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	DV ₆	DV ₅	DV ₄

(Default: DV₆-DV₄=0H / Register Address: BH)

Table 28 EVR Control

DV ₆	DV ₅	DV ₄	DV ₃	DV ₂	DV ₁	DV ₀	V_{LCD}
0	0	0	0	0	0	0	Low
0	0	0	0	0	0	1	:
			:				:
			:				:
1	1	1	1	1	1	1	High

Formula of VLCD

$$VLCD [V] = 0.5 \times VREG + M (VREG - 0.5 \times VREG) / 127$$

VBA = VEE x 0.9

VREG = VREF x N

VBA : Output of the reference voltage generator

VREF : Input of the voltage regulator

VREG : Output of the voltage regulator

N : Boost level

M : EVR Value

(14-21) Frequency Control

The “Frequency Control” instruction adjusts the frame frequency.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	Rf2	Rf1	Rf0

(Default: DV₃-DV₀=0H / Register Address: DH)

Table 29 Frequency Control

Rf 2	Rf 1	Rf 0	Feedback Resistor Value
0	0	0	Reference Value
0	0	1	0.8 x Reference Value
0	1	0	0.9 x Reference Value
0	1	1	1.1 x Reference Value
1	0	0	1.2 x Reference Value
1	0	1	0.7 x Reference Value
1	1	0	1.3 x Reference Value
1	1	1	Inhibited

(14-22) Discharge ON/OFF

Discharge circuit is used to discharge out of the stabilizing capacitors placed on the V_{LCD}, V₁, V₂, V₃, V₄ and V_{OUT}. Refer to “(11-4) Discharge Circuit”.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	1	0	*	*	DIS2	DIS

(Default: DIS2, DIS1=0H / Register Address: EH)

D₀ (DIS)

DIS=0 : Discharge OFF

DIS=1 : Discharge ON (Discharge from V_{LCD}, V₁, V₂, V₃ and V₄)

D₁ (DIS2)

DIS2=0 : Discharge OFF

DIS2=1 : Discharge ON (Discharge from V_{OUT} through the internal resistor between V_{OUT} and V_{EE})

NOTE) Resistance is 100KΩ typical.

(14-23) Register Address

The “Register Address” instruction specifies a register address.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	RA3	RA2	RA1	RA0

(Default: RA3-RA0=BH / Register Address: CH)

(14-24) Register Read

The “Register Read” instruction reads out instruction data from the register which address is specified by the “Register Address” instruction.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	0	1	0/1	0/1	0/1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
*	*	*	*	Internal register data			

(14-25) Window End Column Address

The “Window End Column Address” instruction specifies the column address of the end point. Refer to “(4-2) Window Area for DDRAM Access”. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	EX3	EX2	EX1	EX0

(Default: EX3-EX0=0H / Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	EX7	EX6	EX5	EX4

(Default: EX7-EX4=0H / Register Address: 1H)

(14-26) Window End Row Address

The “Window End Row Address” instruction specifies the row address of the end point. Refer to “(4-2) Window Area for DDRAM Access”. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	EY3	EY2	EY1	EY0

(Default: EY3-EY0=0H / Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	EY5	EY4

(Default: EY5-EY4=0H / Register Address: 3H)

(14-27) Initial Line-reverse Address

The “Initial Line-reverse Address” instruction specifies the start line of the line-reverse display area. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	LS3	LS2	LS1	LS0

(Default: LS3-LS0=0H / Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	LS5	LS4

(Default: LS5-LS4=0H / Register Address: 5H)

(14-28) Last Line-reverse Address

The “Last Line-reverse Address” instruction specifies the end line of the line-reverse display area. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	LE3	LE2	LE1	LE0

(Default: LE3-LE0=0H / Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	LE5	LE4

(Default: LE5-LE4=0H / Register Address: 7H)

(14-29) Line Reverse ON/OFF

The “Line Reverse ON/OFF” instruction enables the line-reverse display, and blink function as well. Note that the line reverse display cannot be used for entire display area. In this case, use the reverse display function by the D₃ (REV) bit of the “Display Control (2)” instruction.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	*	*	BT	LREV

(Default: BT,LREV=0H / Register Address: 8H)

D₀ (LREV)

LREV =0 : Line Reverse OFF (Normal)
LREV =1 : Line Reverse ON

D₁ (BT)

BT =0 : No Blink
BT =1 : Blink once every 32 frames

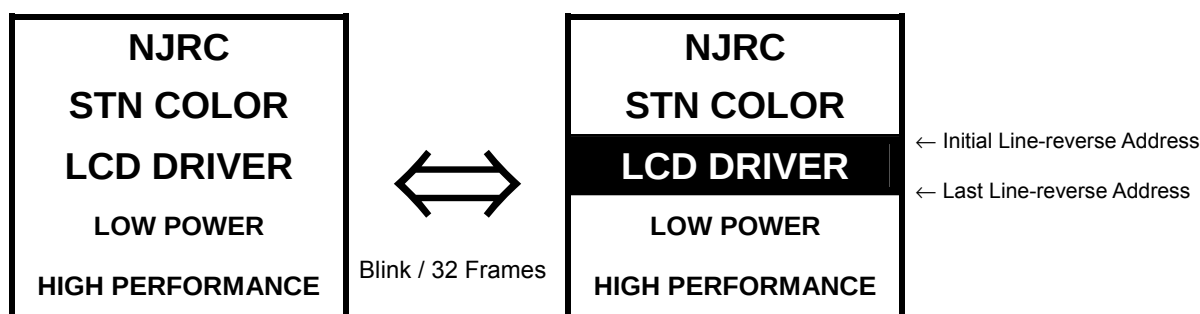
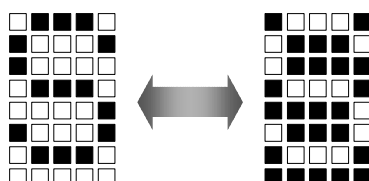


Fig 19 On-screen Image in Using Line-reverse Display and Blink Function

(14-30) Upper/Lower Palette Select

The “Upper/Lower Palette Select” instruction selects either upper or lower palette register.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	*	PS

(Default: PS=0 / Register Address: 9H)

D₀ (PS)

PS=0 : Lower Palettes (PA00, PA01, PA02, PA03, ..., PC74)
 PS=1 : Upper Palettes (PA80, PA81, PA82, PA83, ..., PC154)

(14-31) PWM Control

The “PWM control” instruction selects PWM type, as shown in Fig 20.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	PWMS	PWMA	PWMB	PWMC

(Default: PWMS,PWMA,PWMB,PWMC=0H / Register Address: AH)

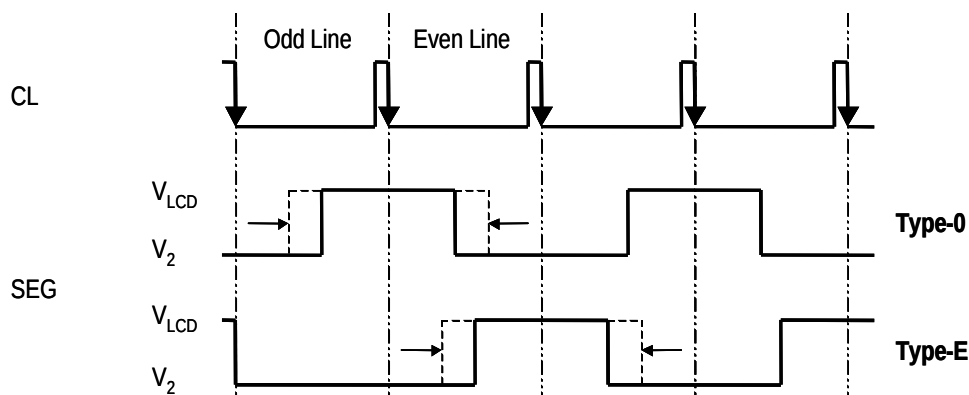
D₃ (PWMS)

PWMS=0 : Type 1
 PWMS=1 : Type 2

D₂ (PWMA), D₁ (PWMB), D₀ (PWMC)

PWMZ=0 (Z=A, B and C): Type 1-O
 PWMZ=1 (Z=A, B and C): Type 1-E

PWM Type 1 (PWMS=0)



PWM Type 2 (PWMS=1)

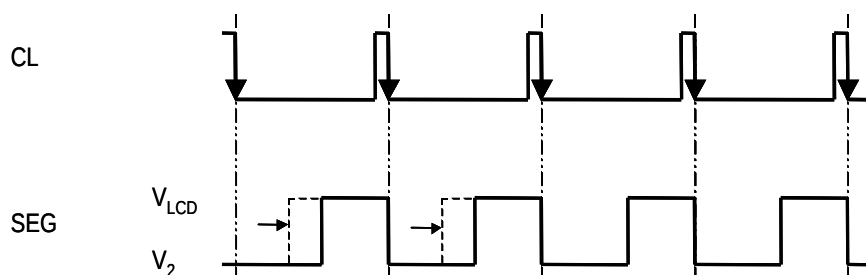


Fig 20 PWM Control

(15) PARTIAL DISPLAY FUNCTION

The partial display function activates specified area on an LCD screen, or equivalently, common drivers are simply scanning this specified area. This function allows LCD modules to work in a minimum duty cycle ratio to minimize power consumption. The partial display function is carried out by the combination of the “Duty Cycle Ratio”, “LCD Bias Ratio”, “Boost Level” and “EVR Control” instructions. For more information, refer to “(14-11) Duty Cycle Ratio”, “(14-12) Boost Level”, “(14-13) LCD Bias Ratio” and “(14-20) EVR Control”. Typical setting sequence is shown in “(18-4) Partial Display Sequence”.

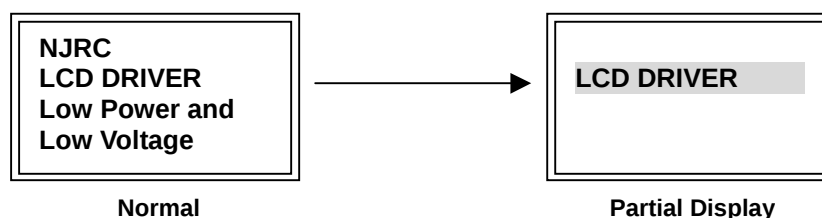
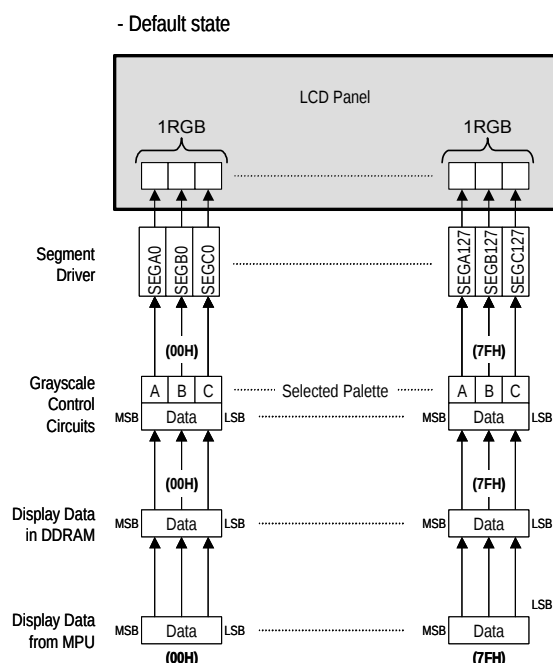


Fig 21 On-screen Image in Using Partial Display Function

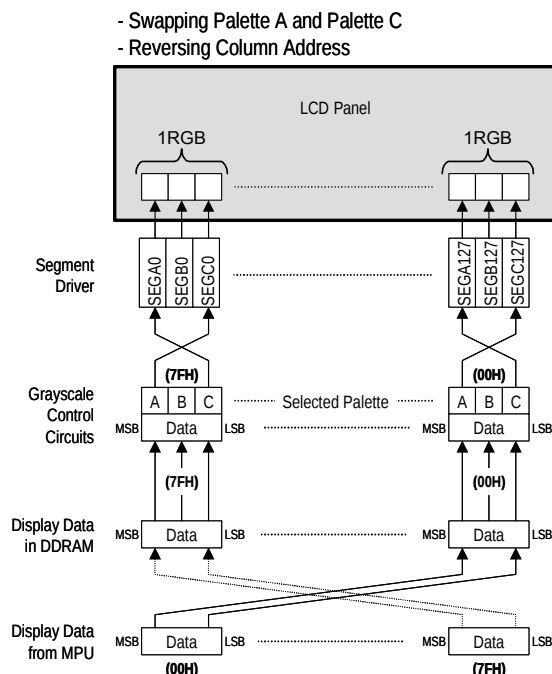
(16) SWAP FUNCTION

The swap function switches the palettes A_j and the palettes C_j ($j=0-15$), and is controlled by the D_1 (SWAP) bit of the “Display Control (2)” instruction. This function reduces the restrictions on the IC position of an LCD module. Fig 22 “Overview of Swap Function” illustrates general outlines of internal operations, and (16-1-1) through (16-1-4) show each configuration on a mode-by-mode basis.

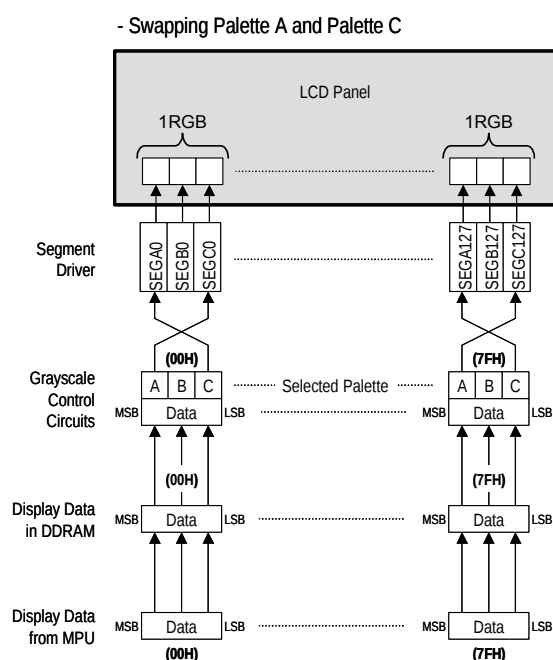
(SWAP, REF)=(0,0)



(SWAP, REF)=(0,1)



(SWAP, REF)=(1,0)



(SWAP, REF)=(1,1)

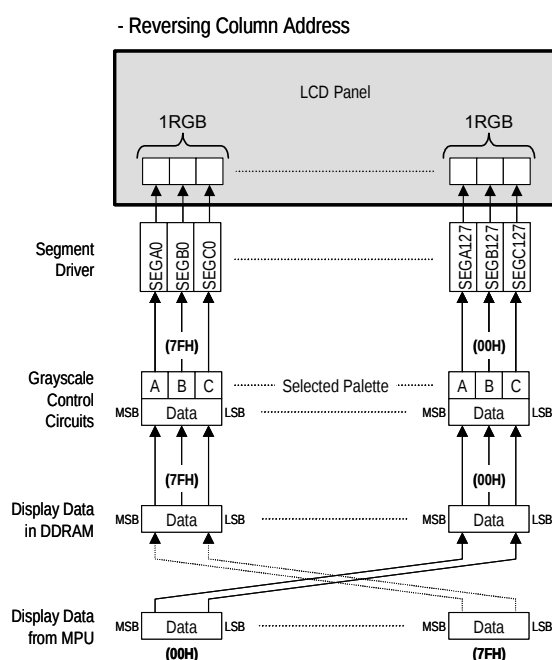
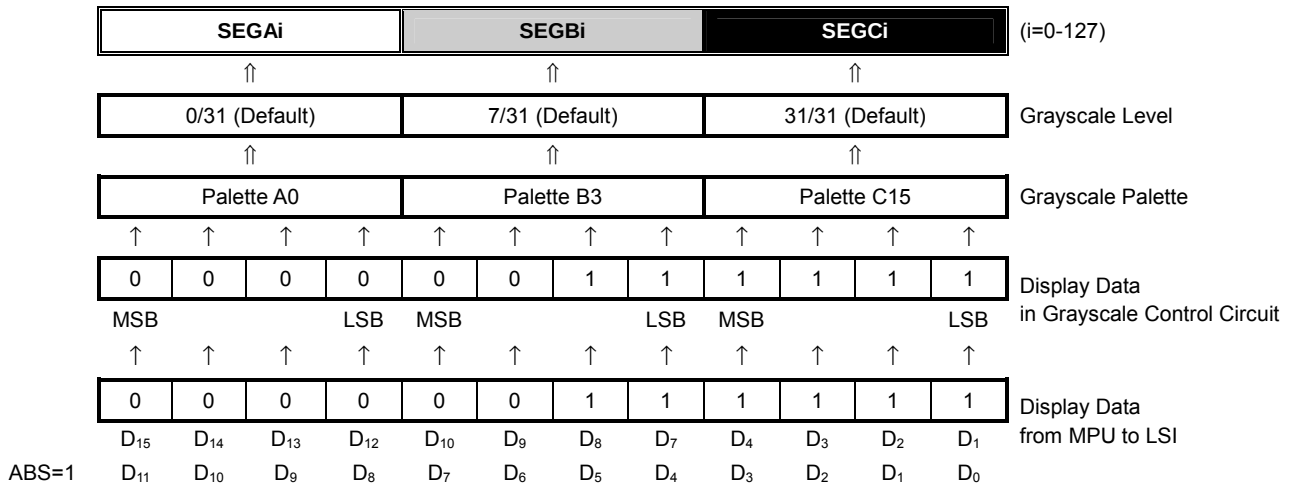


Fig 22 Overview of SWAP Function

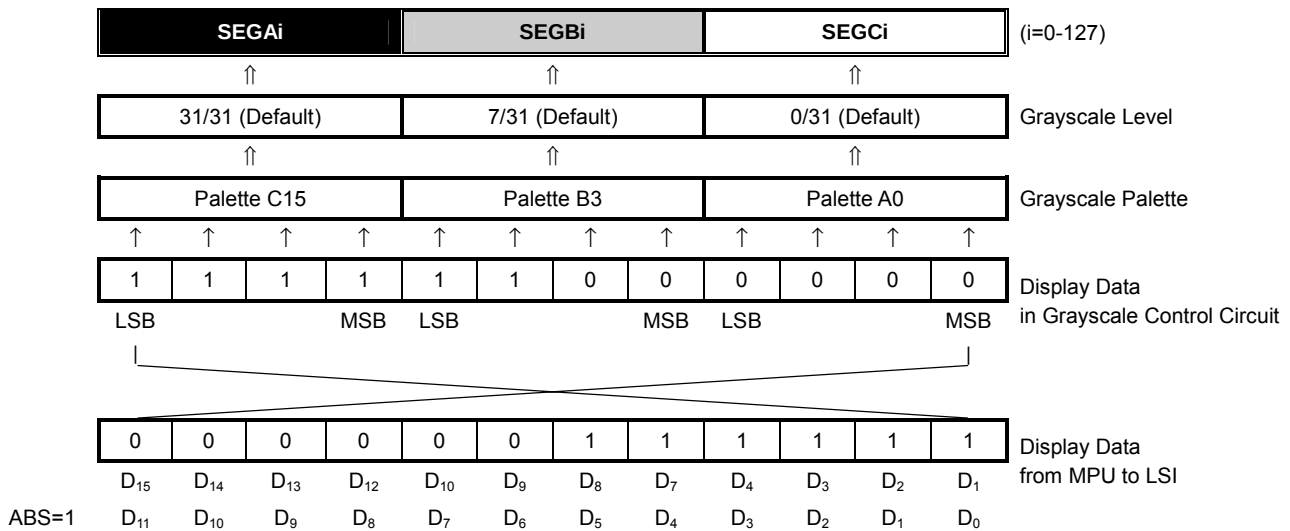
(16-1) Swap Function in Variable 16-grayscale Mode

16-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



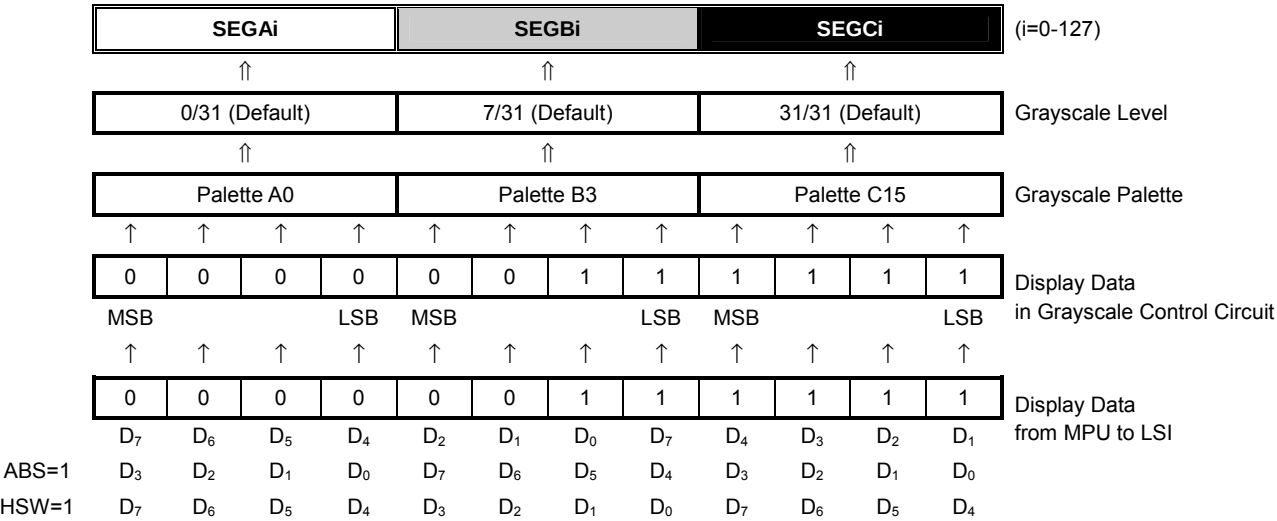
(REF, SWAP)=(0,1) or (1,0)



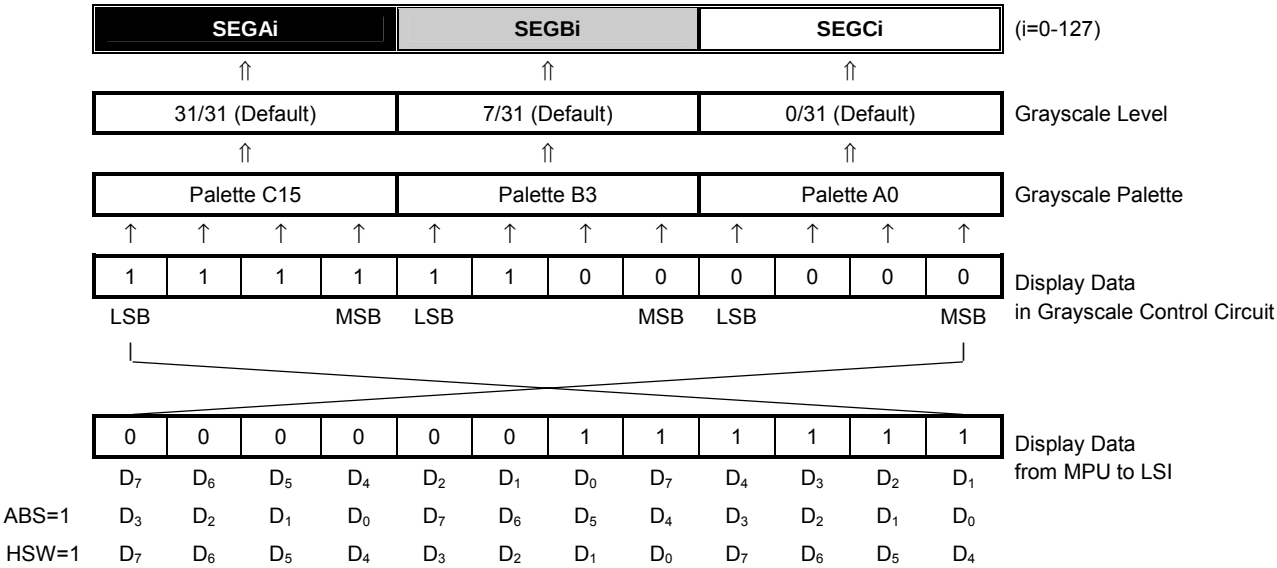
NOTE1) Without a special note on the left, the setting bit such as the ABS, HSW, and C256 are regarded as "0".

8-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



(REF, SWAP)=(0,1) or (1,0)

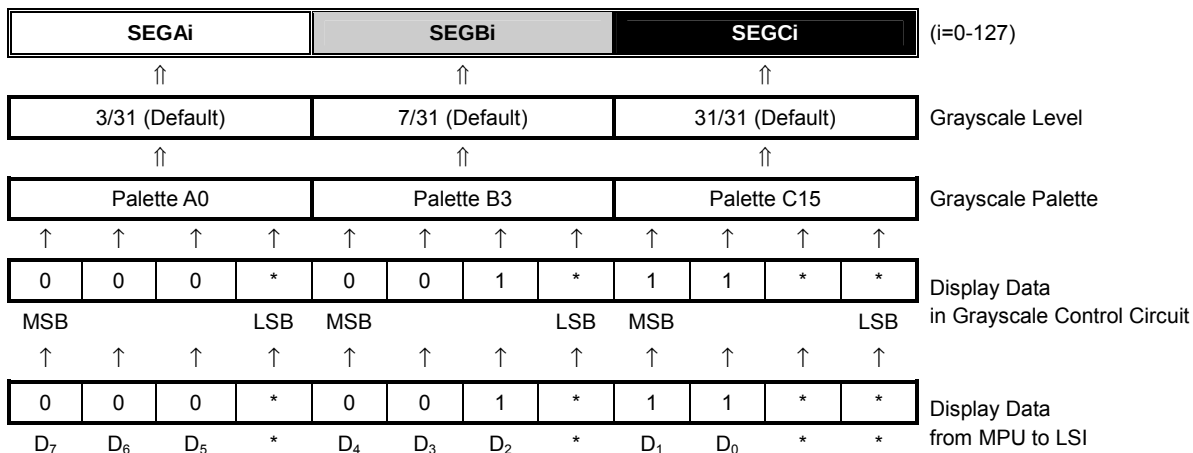


NOTE1) Without a special note on the left, the setting bit such as the ABS, HSW, and C256 are regarded as “0”.

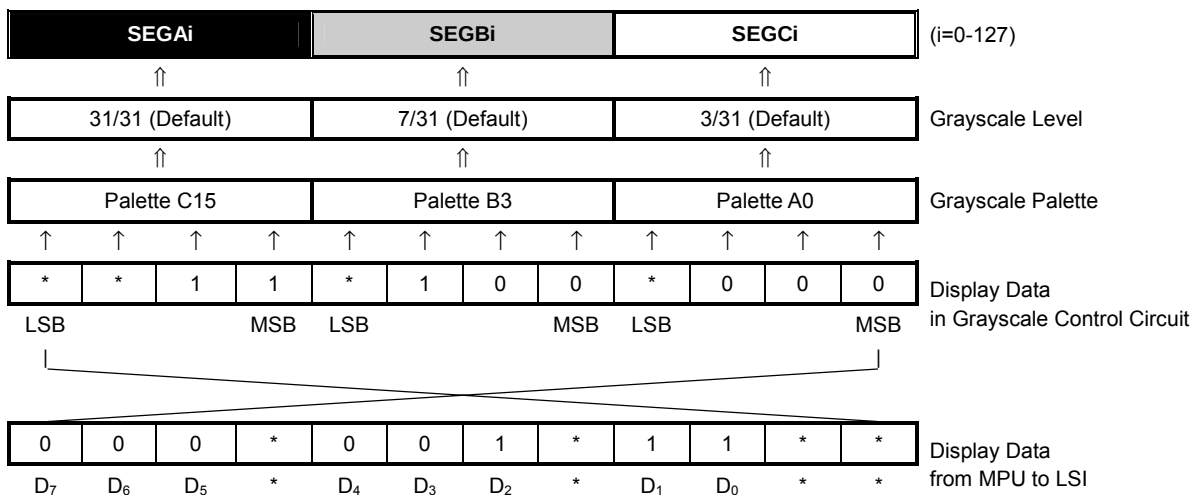
(16-2) Swap Function in Variable 8-grayscale Mode

8-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



(REF, SWAP)=(0,1) or (1,0)

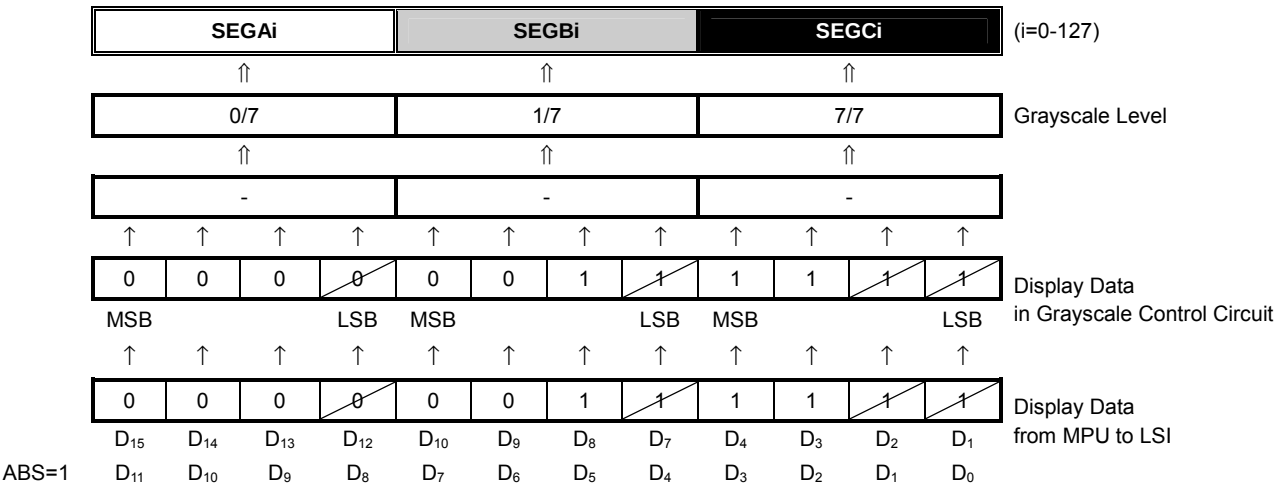


NOTE1) Without a special note on the left, the setting bit such as the ABS, HSW, and C256 are regarded as "0".

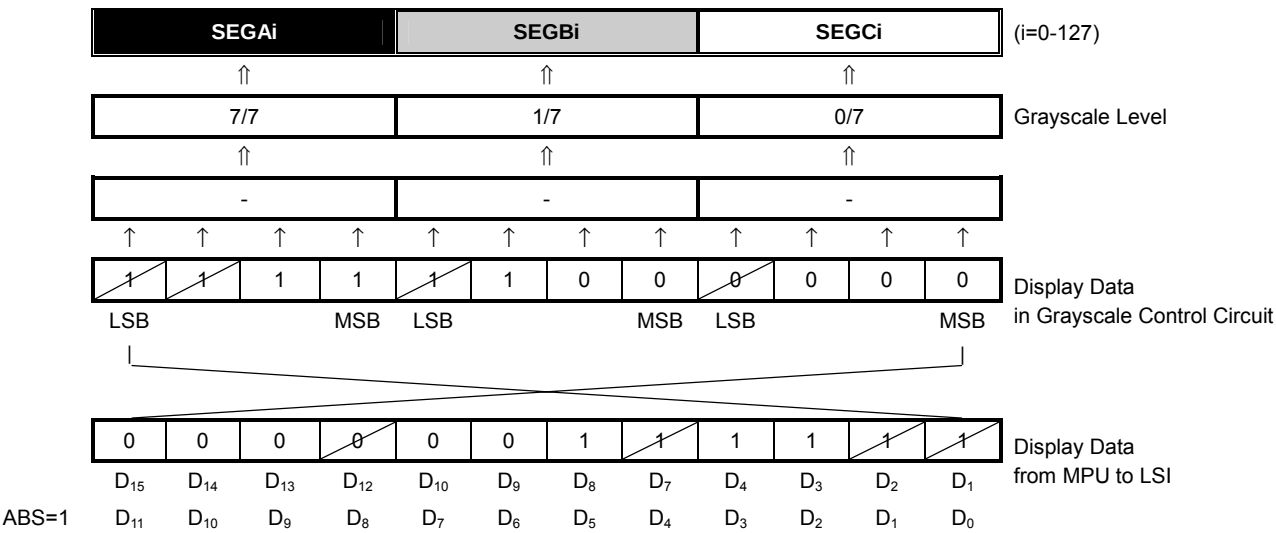
(16-3) Swap Function in Fixed 8-grayscale Mode

16-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



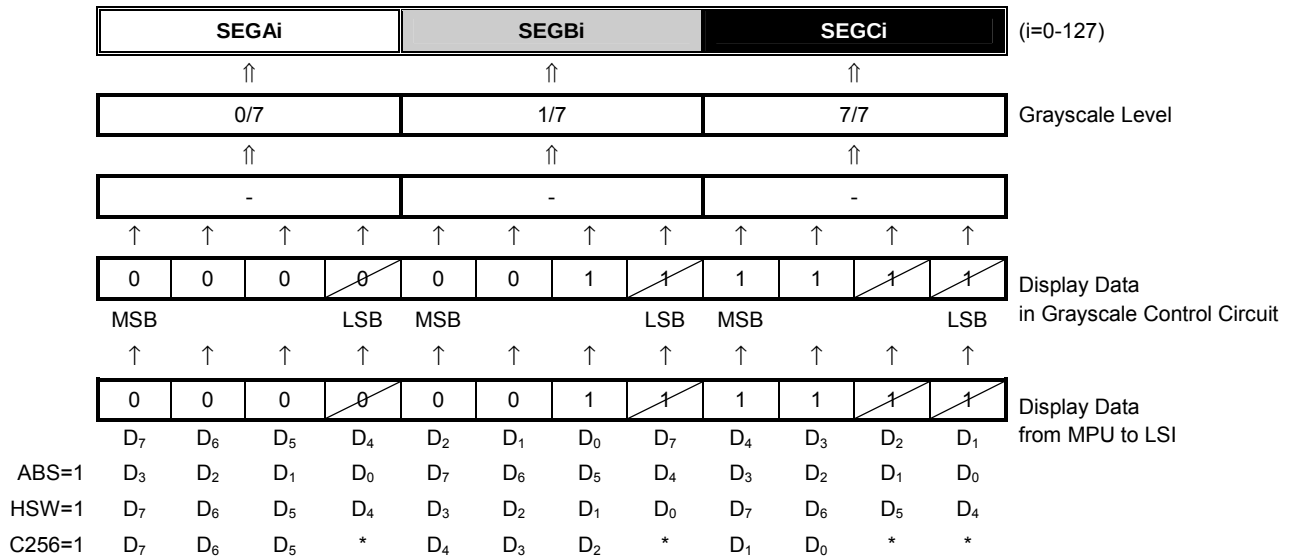
(REF, SWAP)=(0,1) or (1,0)



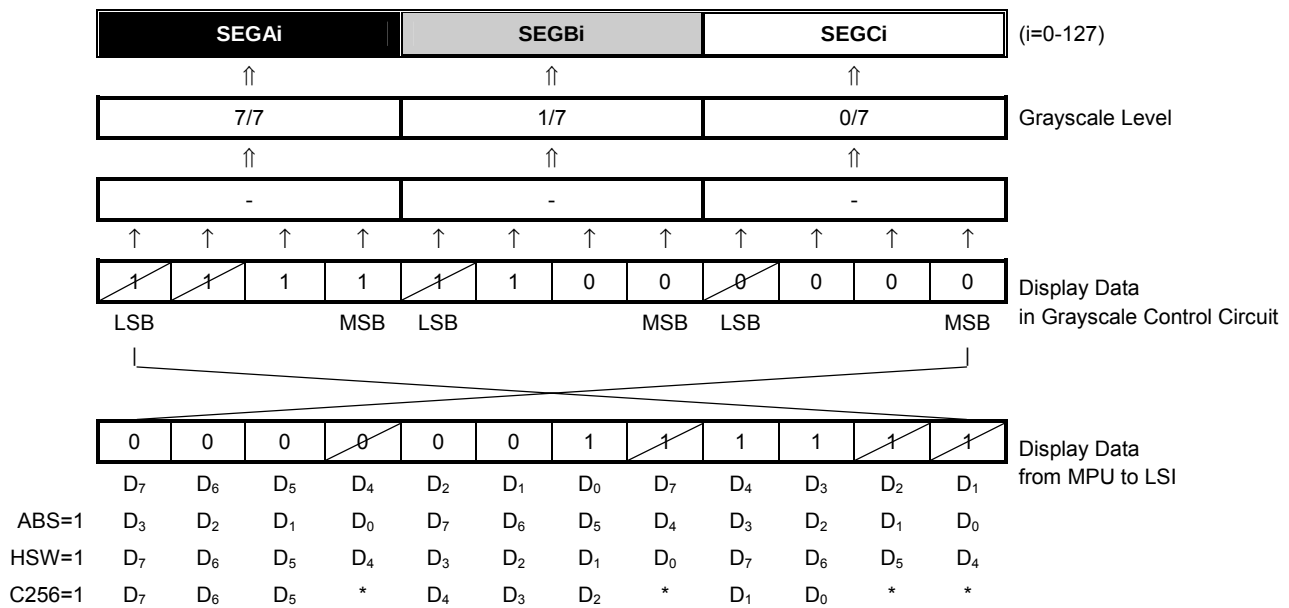
NOTE1) Without a special note on the left, the setting bit such as the ABS, HSW, and C256 are regarded as "0".
NOTE2) The data indicated with a slash mark (/) is invalid.

8-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



(REF, SWAP)=(0,1) or (1,0)

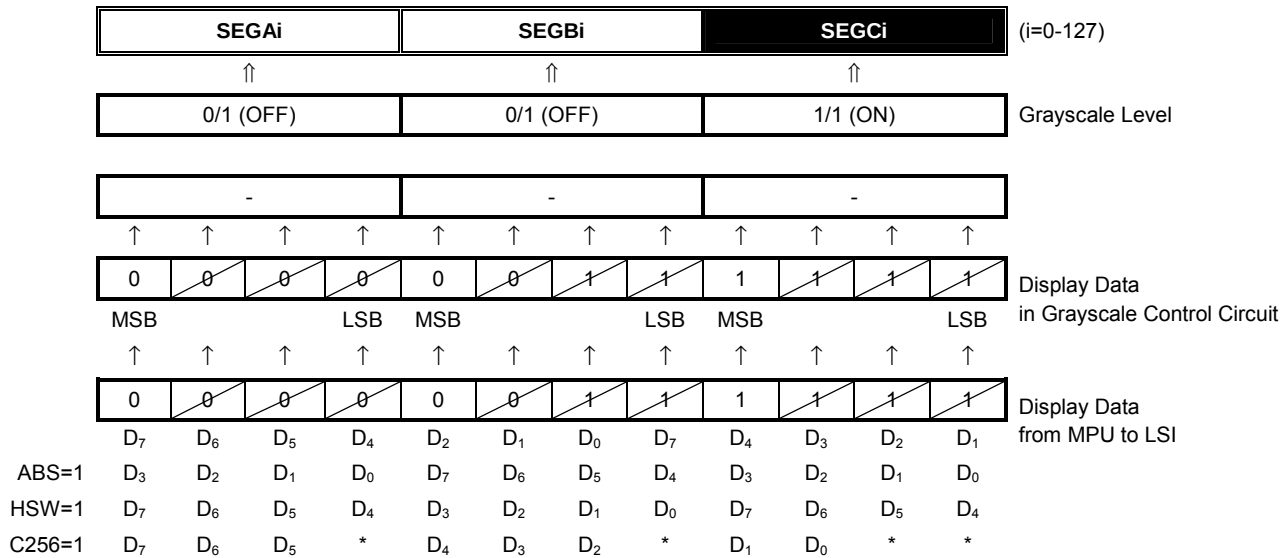


NOTE1) Without a special note on the left, the setting bit such as the ABS, HSW, and C256 are regarded as "0".

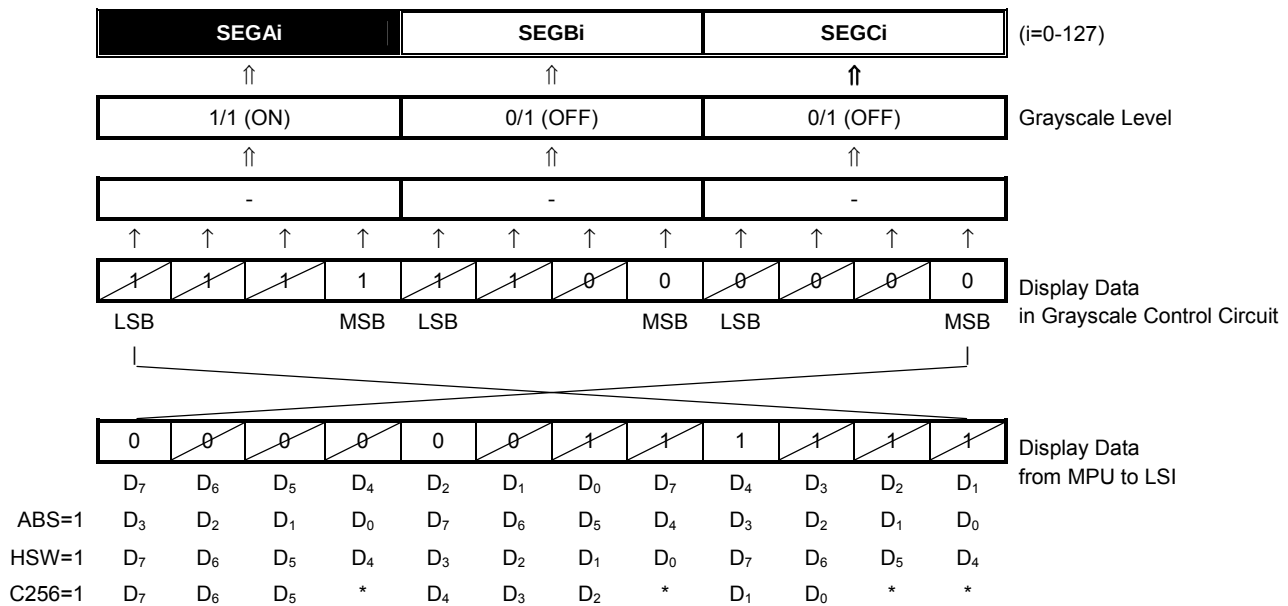
NOTE2) The data indicated with a slash mark (/) is invalid.

8-bit Bus Length

SWAP=0



SWAP=1



NOTE1) Without a special note on the left, the setting bit such as the ABS, HSW, and C256 are regarded as "0".

NOTE2) The data indicated with a slash mark (/) is invalid.

(17) RELATION BETWEEN ROW ADDRESS AND COMMON DRIVER

The relation between row address and common driver is changed by the D₃ (SHIFT) bit of the "Display Control (1)" and the "Duty Cycle Ratio", "Initial Display Line" and "Initial COM" instructions.

When the "Initial Display Line" is set to (LA7:LA0=00H: Address "0"), the row address corresponding to an initial COM is "0". However, if the "Initial Display Line" is other than "0", the row address is shifted from "0" by just that address. For instance, when the initial display line address is (LA7:LA0=05H: Address "5") and the initial COM is (SC3:SC0=1H), the row address on the initial COM is "5" and the initial COM is "COM₄".

(17-1) through (17-5) illustrate the examples of the relation between row address and common driver.

(17-1) Initial display line “0”, 1/41 duty cycle (Common forward scan, DSE=“0”)

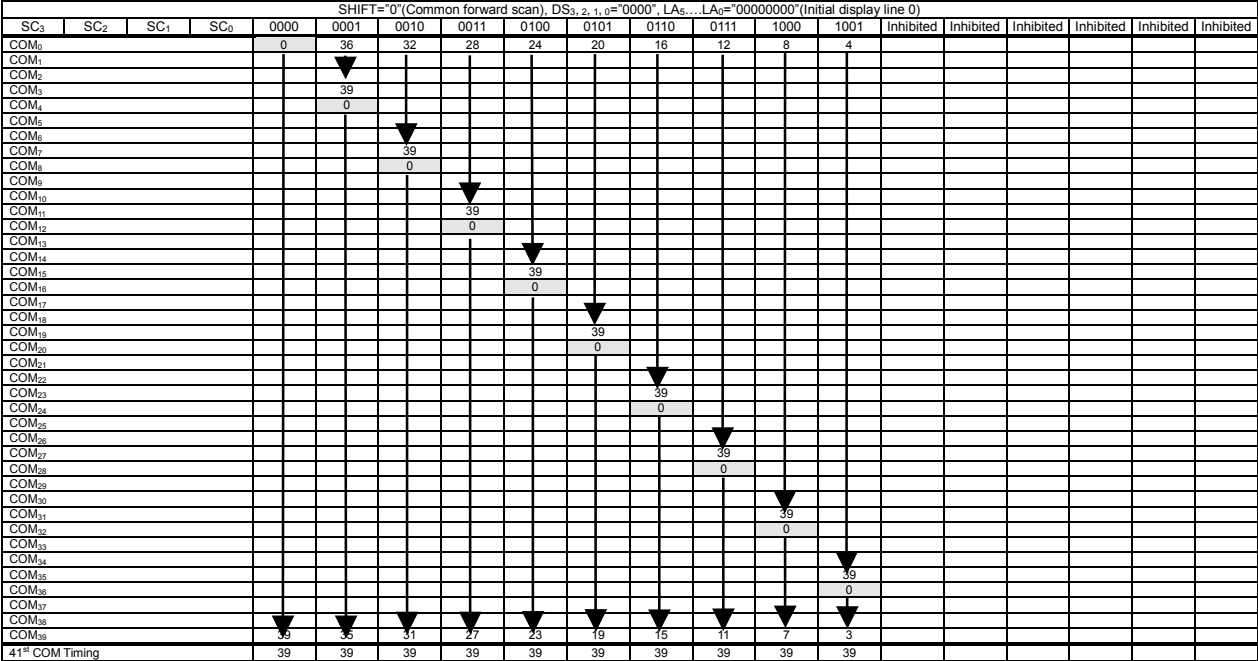


Fig 23 Relation between Row address and Common Driver (1)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address
NOTE2) Segment waveforms for 41st COM timing are the same as for 40th COM timing (Row address “27H”).

(17-2) Initial display line “0”, 1/41 duty cycle (Common backward scan, DSE=“0”)

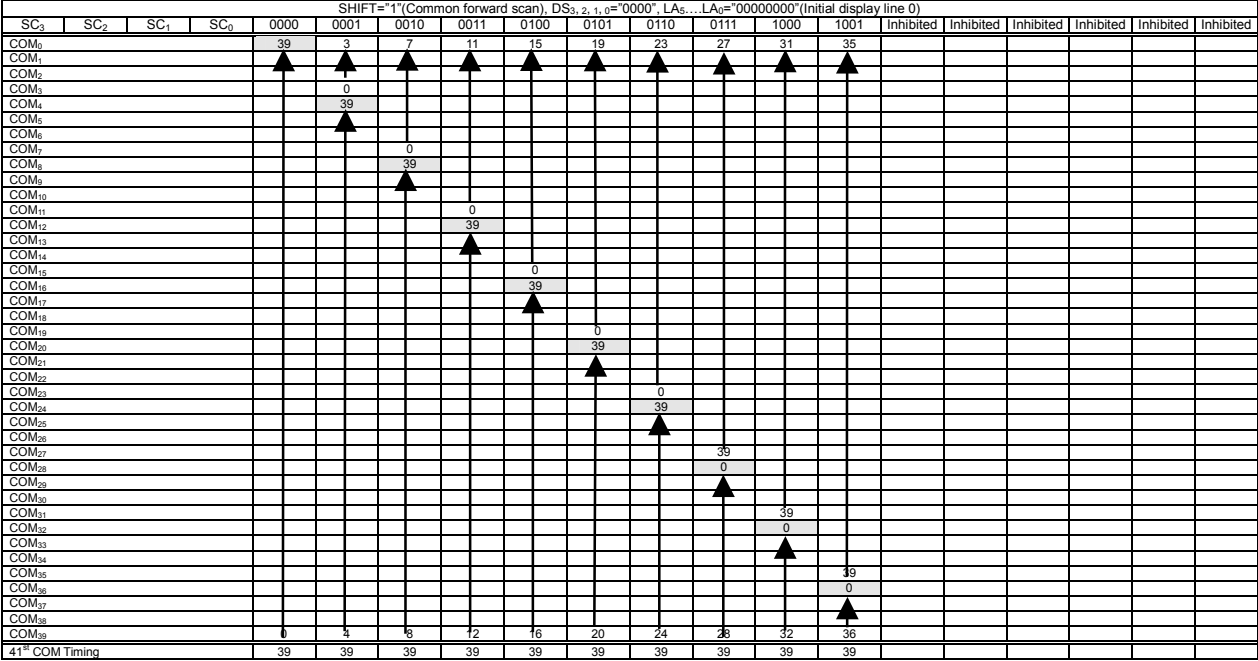


Fig 24 Relation between Row address and Common Driver (2)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address
NOTE2) Segment waveforms for 41st COM timing are the same as for 40th COM timing (Row address “27H”).

(17-3) Initial display line "0", 1/17 duty cycle (Common forward scan, DSE="0")

SC ₃	SC ₂	SC ₁	SC ₀	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited
COM ₀				0							12	8	4					
COM ₁											15							
COM ₂																		
COM ₃																		
COM ₄				0														
COM ₅																		
COM ₆																		
COM ₇																		
COM ₈																		
COM ₉																		
COM ₁₀																		
COM ₁₁																		
COM ₁₂																		
COM ₁₃																		
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COM ₂₅																		
COM ₂₆																		
COM ₂₇																		
COM ₂₈																		
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COM ₃₀																		
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COM ₃₄																		
COM ₃₅																		
COM ₃₆																		
COM ₃₇																		
COM ₃₈																		
COM ₃₉																		
17 th COM Timing				15	15	15	15	15	15	15	15	15	15					

Fig 25 Relation between Row address and Common Driver (3)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address.

NOTE2) Segment waveforms for 17th COM timing are the same as for 16th COM timing.

(17-4) Initial display line "5", 1/41 duty cycle (Common forward scan, DSE="0")

SC ₃	SC ₂	SC ₁	SC ₀	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited
COM ₀				5														
COM ₁																		
COM ₂																		
COM ₃																		
COM ₄																		
COM ₅																		
COM ₆																		
COM ₇																		
COM ₈																		
COM ₉																		
COM ₁₀																		
COM ₁₁																		
COM ₁₂																		
COM ₁₃																		
COM ₁₄																		
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COM ₃₄																		
COM ₃₅																		
COM ₃₆																		
COM ₃₇																		
COM ₃₈																		
COM ₃₉																		
41 th COM Timing				4	4	4	4	4	4	4	4	4	4					

Fig 26 Relation between Row address and Common Driver (4)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address

NOTE2) Segment waveforms for 41st COM timing are the same as for 40th COM timing.

(17-5) Initial display line “0”, 1/40 duty cycle (Common forward scan, DSE=“1”)

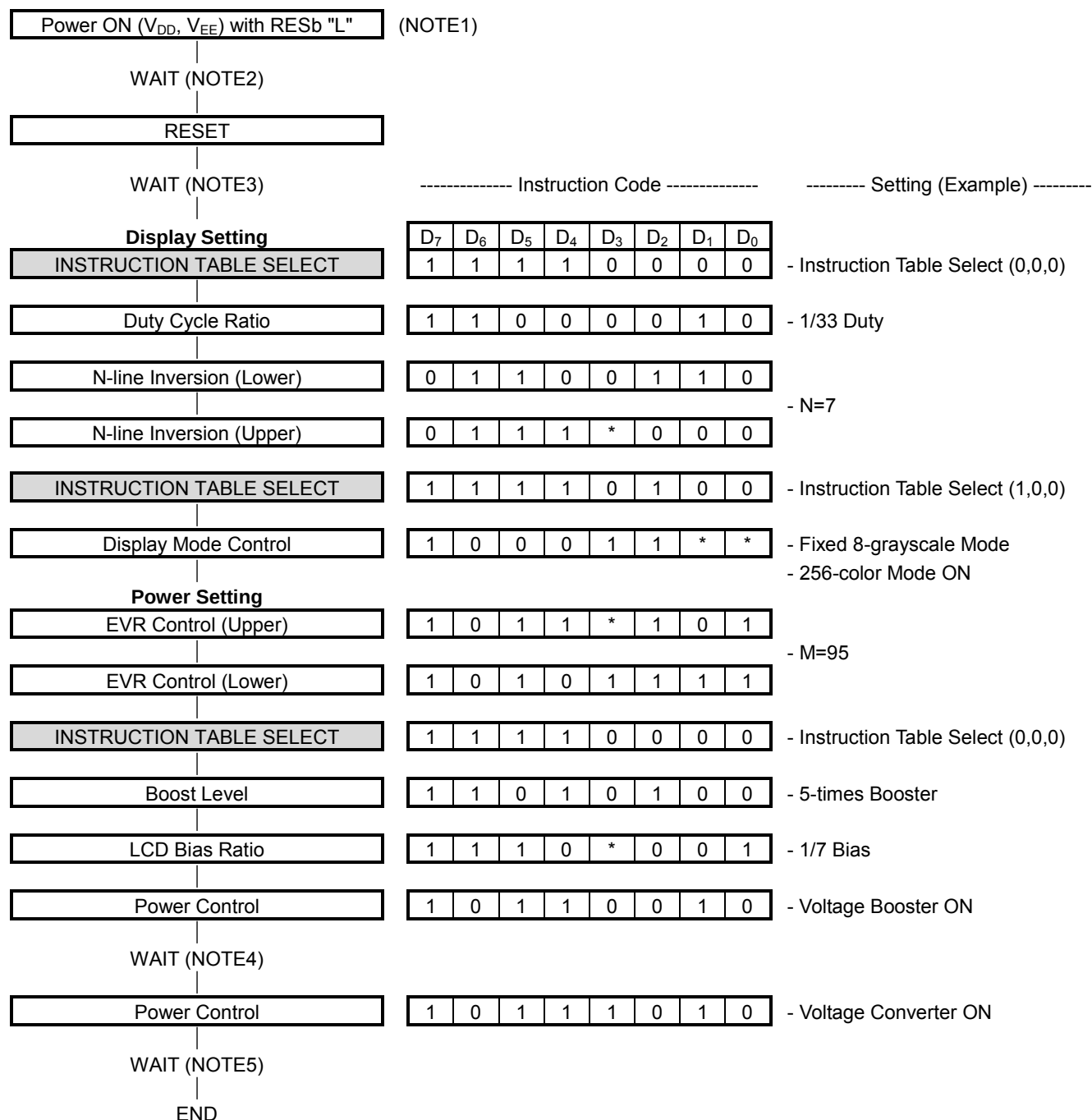
				SHIFT="0"(Common forward scan), DS _{3,2,1,0} ="0000", LA _{5...LA0} ="00000000"(Initial display line 0) DSE="1"										Inhibited				
SC ₃	SC ₂	SC ₁	SC ₀	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001					
COM ₀				0	36	32	28	24	20	16	12	8	4					
COM ₁					▼													
COM ₂					39													
COM ₃					0													
COM ₄						▼												
COM ₅						39												
COM ₆						0												
COM ₇							▼											
COM ₈							39											
COM ₉							0											
COM ₁₀								▼										
COM ₁₁								39										
COM ₁₂								0										
COM ₁₃									▼									
COM ₁₄									39									
COM ₁₅									0									
COM ₁₆										▼								
COM ₁₇										39								
COM ₁₈										0								
COM ₁₉											▼							
COM ₂₀											39							
COM ₂₁											0							
COM ₂₂												▼						
COM ₂₃												39						
COM ₂₄												0						
COM ₂₅													▼					
COM ₂₆													39					
COM ₂₇													0					
COM ₂₈														▼				
COM ₂₉														39				
COM ₃₀														0				
COM ₃₁															▼			
COM ₃₂															39			
COM ₃₃															0			
COM ₃₄																▼		
COM ₃₅																39		
COM ₃₆																0		
COM ₃₇																	▼	
COM ₃₈																	39	
COM ₃₉																	0	
					39	35	31	27	23	19	15	11	7	3				

Fig 27 Relation between Row address and Common Driver (5)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address

(18) TYPICAL INSTRUCTION SEQUENCES

(18-1) Initialization Sequence in Using Internal LCD Power Supply



NOTE1) If different power sources are applied to the V_{DD} and the V_{EE} , turn on the V_{DD} first.

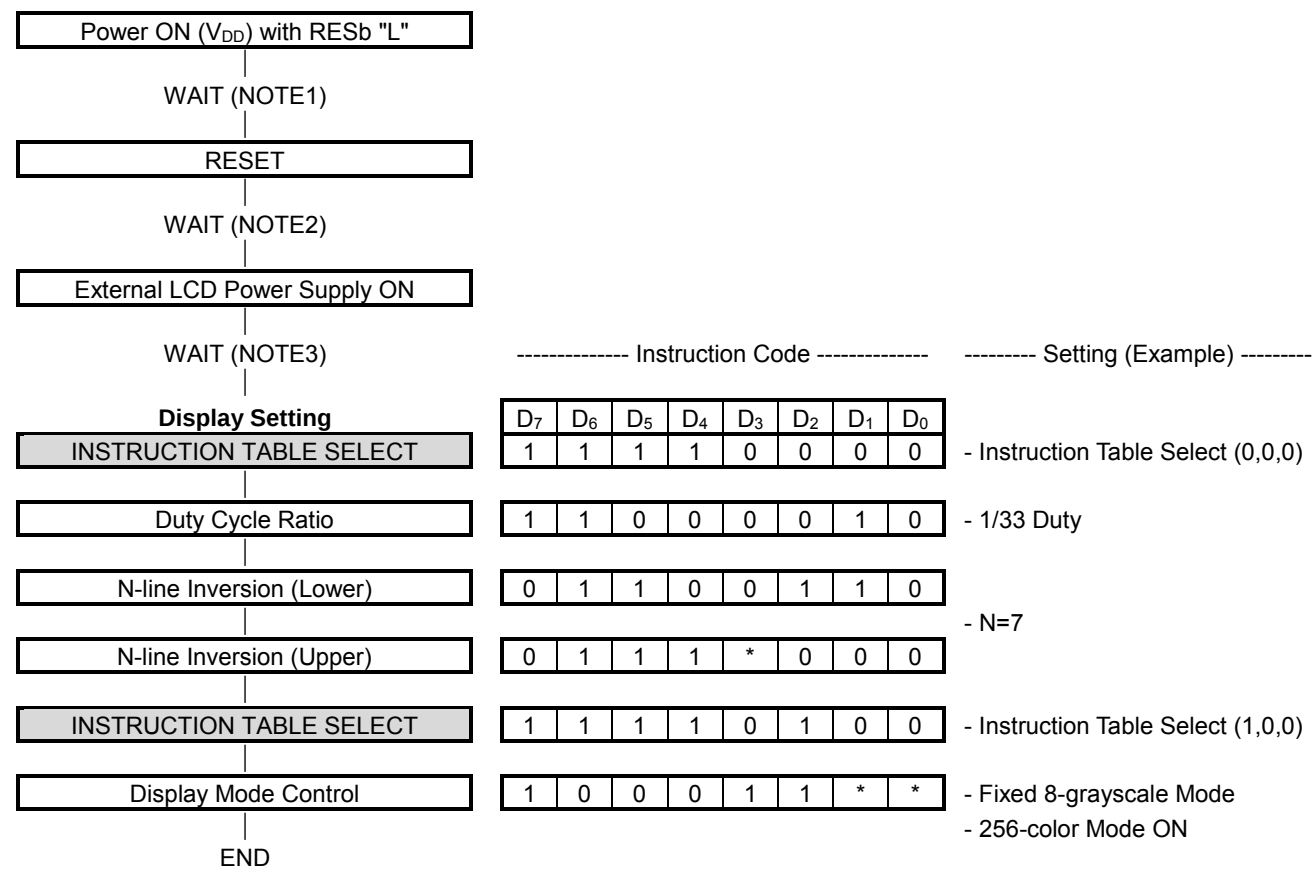
NOTE2) Wait until the V_{DD} and V_{EE} are stabilized.

NOTE3) Wait 10 [μ s] or more.

NOTE4) Wait until the V_{OUT} is stabilized.

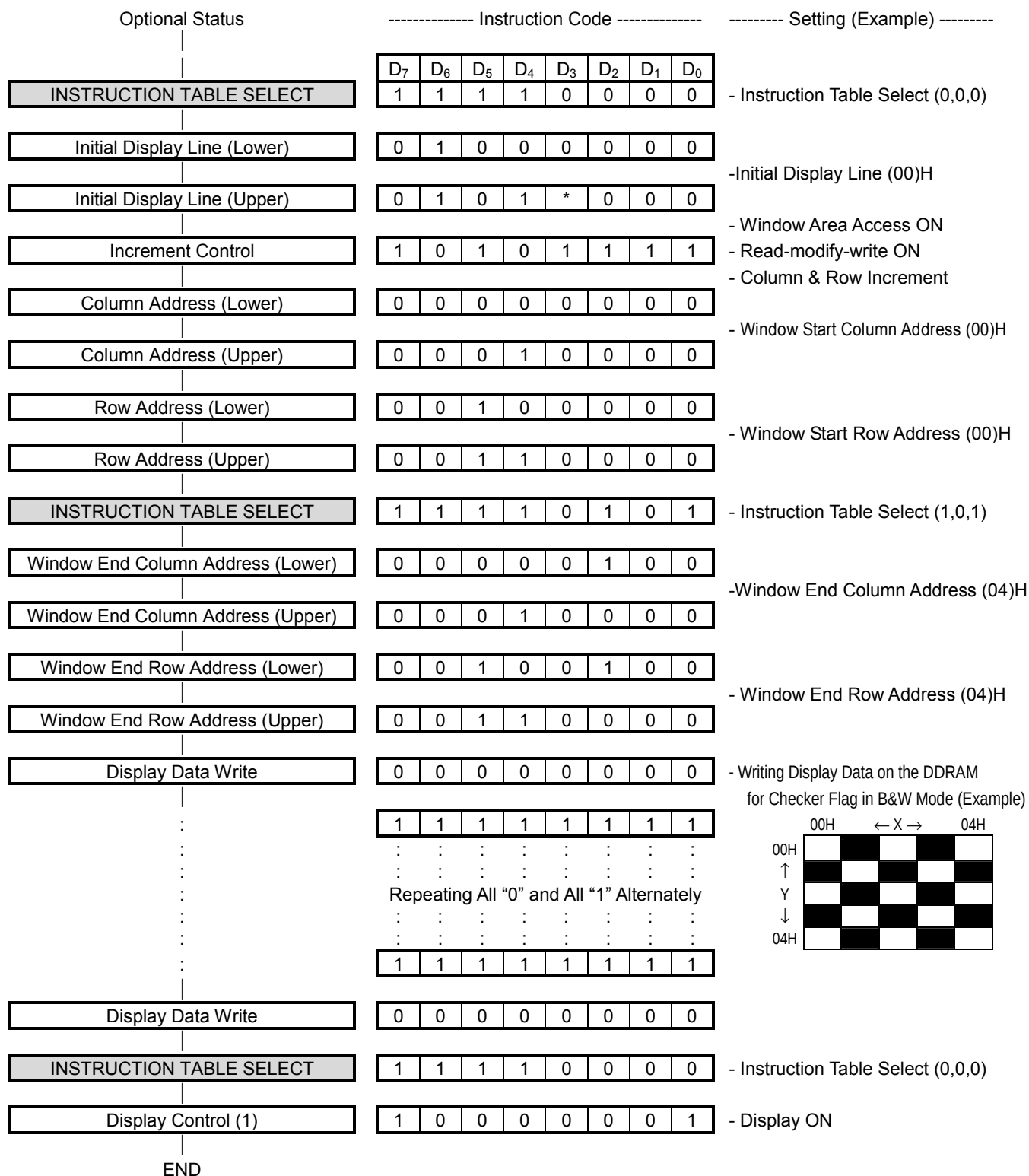
NOTE5) Wait until the V_{LCD} and V_1 - V_4 are stabilized.

(18-2) Initialization Sequence in Using External LCD Power Supply

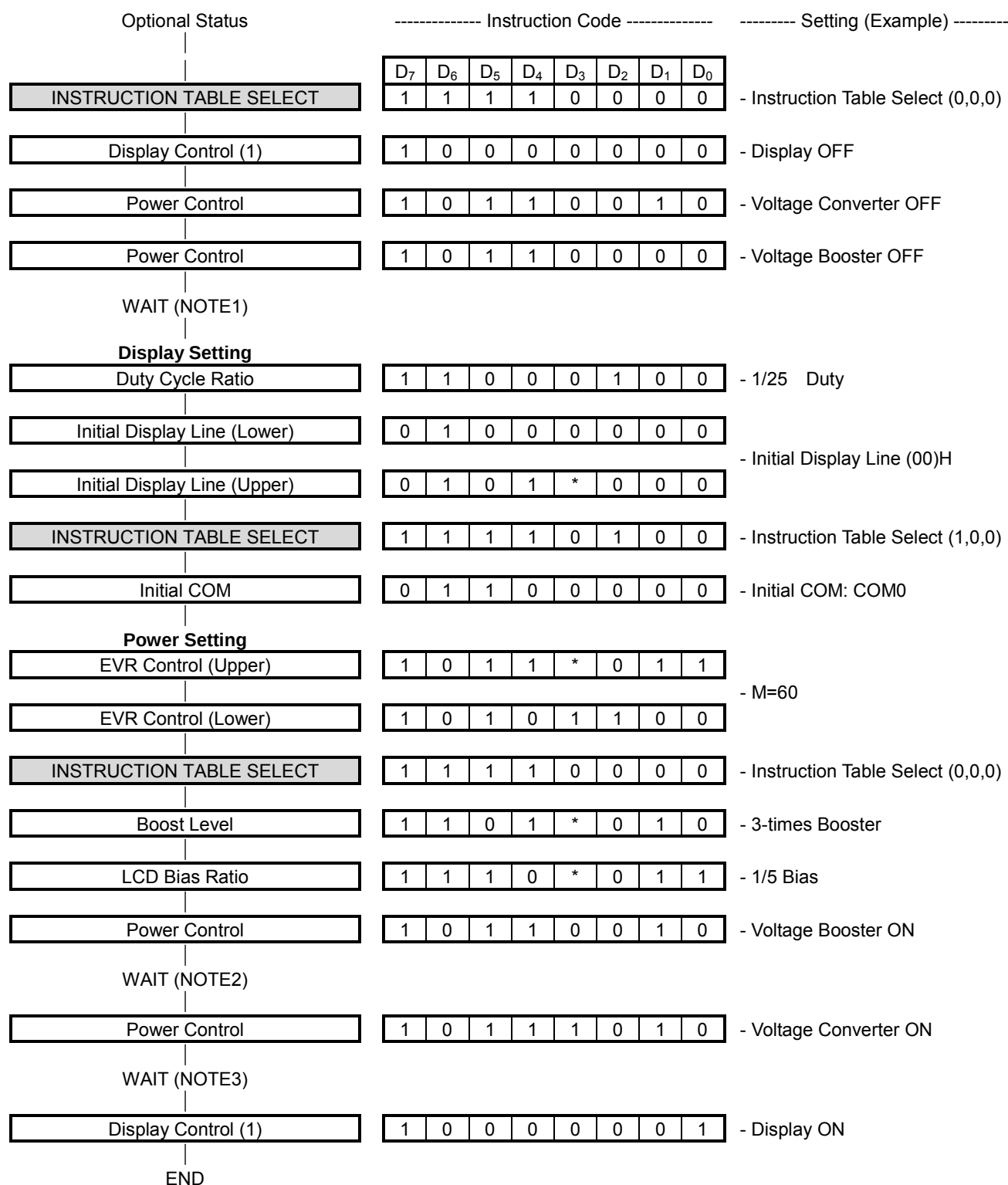


NOTE1) Wait until the V_{DD} is stabilized.
NOTE2) Wait 10 [us] or more.
NOTE3) Wait until the external LCD power supply (V_{OUT}, V_{LCD}, V₁-V₄) are stabilized.

(18-3) Display Data Write Sequence



(18-4) Partial Display Sequence

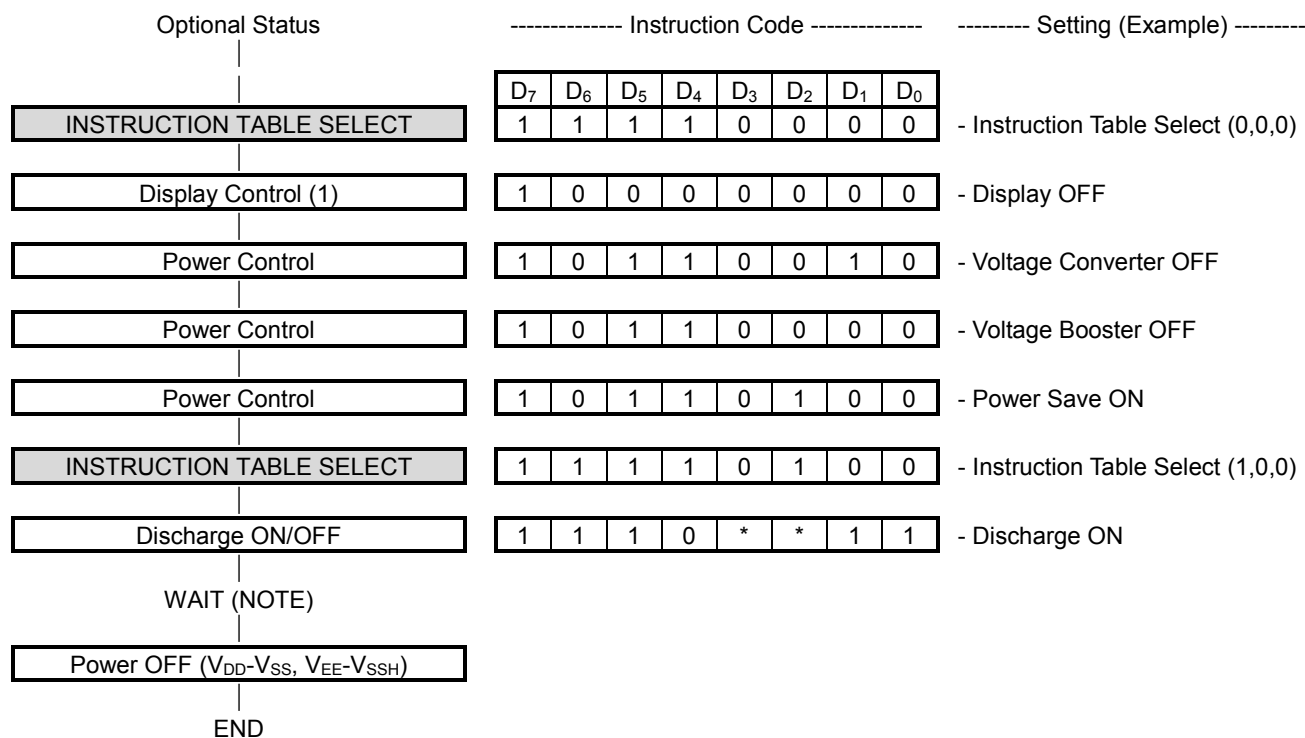


NOTE1) Wait until the voltage booster is completely turned off. Make sure what is the wait time in the particular application.

NOTE2) Wait until the V_{OUT} is stabilized.

NOTE3) Wait until the V_{LCD} and V_1 - V_4 are stabilized.

(18-5) Power OFF Sequence



NOTE) Wait until the Discharge is completed.

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITION	TERMINAL	RATING	UNIT
Supply Voltage (1)	V_{DD}	$V_{SS}=0V$ $T_a = +25^{\circ}C$	V_{DD}	-0.3 to +4.0	V
Supply Voltage (2)	V_{EE}		V_{EE}	-0.3 to +4.0	V
Supply Voltage (3)	V_{OUT}		V_{OUT}	-0.3 to +19.0	V
Supply Voltage (4)	V_{REG}		V_{REG}	-0.3 to +19.0	V
Supply Voltage (5)	V_{LCD}		V_{LCD}	-0.3 to +19.0	V
Supply Voltage (6)	V_1, V_2, V_3, V_4		V_1, V_2, V_3, V_4	-0.3 to $V_{LCD} + 0.3$	V
Input Voltage	V_I		*1	-0.3 to $V_{DD} + 0.3$	V
Storage Temperature	T_{stg}			-45 to +125	$^{\circ}C$

NOTE1) D_0 to D_{15} , CSb, RS, RDb, WRb, OSC1, RESb

NOTE2) To stabilize the LSI operation, place decoupling capacitors between V_{DD} and V_{SS} and between V_{EE} and V_{SSH} .

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TERMINAL	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{DD1}	V_{DD}	1.7		3.3	V	1
	V_{DD2}		2.4		3.3	V	2
	V_{EE}	V_{EE}	2.4		3.3	V	3
Operating Voltage	V_{LCD}	V_{LCD}	5		18.0	V	4
	V_{OUT}	V_{OUT}			18.0	V	
	V_{REG}	V_{REG}			$V_{OUT} \times 0.9$	V	
	V_{REF}	V_{REF}	2.1		3.3	V	5
Operating Temperature	T_{opr}		-30		85	$^{\circ}C$	

NOTE1) Applied to the condition when the reference voltage generator is not used.

NOTE2) Applied to the condition when the reference voltage generator is used.

NOTE3) Applied to the condition when the voltage booster is used.

NOTE4) The following relation among the LCD bias voltages must be maintained.

$$V_{SSH} < V_4 < V_3 < V_2 < V_1 < V_{LCD} < V_{OUT}$$

NOTE5) Relation: $V_{REF} < V_{EE}$ must be maintained.

■ DC CHARACTERISTICS

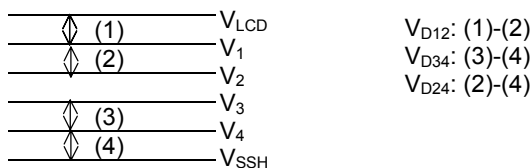
$V_{SS} = 0V$, $V_{DD} = +1.7$ to $+3.3V$, $T_a = -30$ to $+85^\circ C$

PARAMETER	SYM BOL	CONDITION	MIN	TYP	MAX	UNIT	NOTE
High level input voltage	V_{IH}		$0.8 V_{DD}$		V_{DD}	V	*1
Low level input voltage	V_{IL}		0		$0.2V_{DD}$	V	*1
High level output voltage	V_{OH1}	$I_{OH} = -0.4mA$	$V_{DD} - 0.4$			V	*2
Low level output voltage	V_{OL1}	$I_{OL} = 0.4mA$			0.4	V	*2
High level output voltage	V_{OH2}	$I_{OH} = -0.1mA$	$V_{DD} - 0.4$			V	*3
Low level output voltage	V_{OL2}	$I_{OL} = 0.1mA$			0.4	V	*3
Input leakage current	I_{LI}	$V_I = V_{SS}$ or V_{DD}	-10		10	μA	*4
Output leakage current	I_{LO}	$V_I = V_{SS}$ or V_{DD}	-10		10	μA	*5
Driver ON-resistance	R_{ON1}	$ \Delta V_{ON} = 0.5V$	$V_{LCD} = 10V$	1	2	$k\Omega$	*6
			$V_{LCD} = 6V$	2	4		
Stand-by current	I_{STB}	$CSb=H$, $T_a=25^\circ C$	$V_{DD} = 3V$		15	μA	*7
Internal oscillation Frequency	f_{OSC1}	$V_{DD} = 3V$ $T_a = 25^\circ C$	166	203	240	kHz	*8
	f_{OSC2}		37	46	55		*9
	f_{OSC3}		5.3	6.6	7.8		*10
External oscillation Frequency	f_1	$Rf=51k\Omega$		172		kHz	*11
	f_2	$Rf=240k\Omega$		40			
	f_3	$Rf=1800k\Omega$		5.5			
Voltage converter output voltage	V_{OUT}	N-time booster ($N=2$ to 5) $RL = 500k\Omega$ ($V_{OUT} - V_{SS}$)	$(N \times V_{EE})$ $\times 0.95$			V	*12
Supply current (1)	I_{DD1}	$V_{DD} = 3V$, 5-time booster Whole ON pattern		520	780	μA	*13
Supply current (2)	I_{DD2}	$V_{DD} = 3V$, 5-time booster Checker pattern		650	980		
Supply current (3)	I_{DD3}	$V_{DD} = 3V$, 4-time booster Whole ON pattern		360	540		
Supply current (4)	I_{DD4}	$V_{DD} = 3V$, 4-time booster Checker pattern		450	680		
V_{BA} Operating voltage	V_{BA}	$V_{EE} = 2.4$ to $3.3V$	$(0.9 V_{EE})$ $\times 0.98$	$0.9 V_{EE}$	$(0.9 V_{EE})$ $\times 1.02$	V	*14
V_{REG} Operating voltage	V_{REG}	$V_{EE} = 2.4$ to $3.3V$ $V_{REF} = 0.9 \times V_{EE}$ N-time booster ($N=2$ to 5)	$(V_{REF} \times N)$ $\times 0.97$	$(V_{REF} \times N)$	$(V_{REF} \times N)$ $\times 1.03$	V	*15
Output Voltage	V_2		-100	0	+100	mV	*16
	V_3		-100	0	+100		
	V_{D12}		-30	0	+30		
	V_{D34}		-30	0	+30		
	V_{D24}		-30	0	+30		

■ OSCILLATION FREQUENCY AND FRAME FREQUENCY

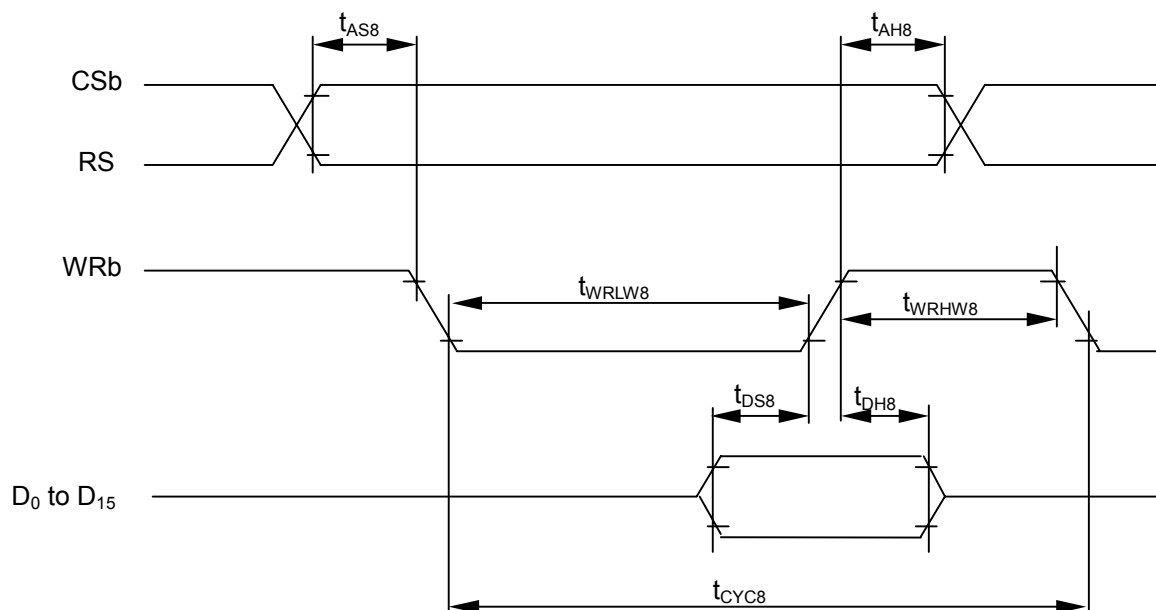
PARAMETER	SYMBOL	Display mode	Display duty cycle ratio (1/D) <DSE=0>				NOTE
			1/41 to 1/25	1/21 to 1/13	1/9	1/5	
Internal clock	f_{osc}	Variable 8-/16-level Grayscale Mode	$f_{osc} / (62xD)$	$f_{osc} / (62xD \times 2)$	$f_{osc} / (62xD \times 4)$	$f_{osc} / (62xD \times 8)$	FLM
		Fixed 8-level Grayscale Mode	$f_{osc} / (14xD)$	$f_{osc} / (14xD \times 2)$	$f_{osc} / (14xD \times 4)$	$f_{osc} / (14xD \times 8)$	
		B&W Mode	$f_{osc} / (2xD)$	$f_{osc} / (2xD \times 2)$	$f_{osc} / (2xD \times 4)$	$f_{osc} / (2xD \times 8)$	
External clock	f_{ck}	Variable 8-/16-level Grayscale Mode	$f_{ck} / (62xD)$	$f_{ck} / (62xD \times 2)$	$f_{ck} / (62xD \times 4)$	$f_{ck} / (62xD \times 8)$	
		Fixed 8-level Grayscale Mode	$f_{ck} / (14xD)$	$f_{ck} / (14xD \times 2)$	$f_{ck} / (14xD \times 4)$	$f_{ck} / (14xD \times 8)$	
		B&W Mode	$f_{ck} / (2xD)$	$f_{ck} / (2xD \times 2)$	$f_{ck} / (2xD \times 4)$	$f_{ck} / (2xD \times 8)$	

- NOTE1) D_0 - D_{15} , CSb, RS, RDb, WRb, P/S, SEL68 and RESb
- NOTE2) D_0 - D_{15}
- NOTE3) CL, FLM, FR and CLK
- NOTE4) CSb, RS, SEL68, RDb, WRb, P/S, RESb and OSC1
- NOTE5) D_0 - D_{15} in high impedance
- NOTE6) SEGA₀-SEGA₁₂₇, SEGB₀-SEGB₁₂₇, SEGC₀-SEGC₁₂₇ and COM₀-COM₃₉
This parameter defines the resistance between each COM/SEG and each LCD bias (V_{LCD} , V_1 , V_2 , V_3 and V_4).
- 0.5V Difference / 1/8 LCD Bias
- NOTE7) V_{DD}
Oscillator is halted.
- CSb=1 (Disabled) / No-load on COM/SEG
- NOTE8) CLK
This parameter defines the oscillation frequency by using the internal resistor, in the Variable grayscale mode.
- (Rf2, Rf1, Rf0)=(0,0,0)
- NOTE9) CLK
This parameter defines the oscillation frequency by using the internal resistor, in the 8-level fixed grayscale mode.
- (Rf2, Rf1, Rf0)=(0,0,0)
- NOTE10) CLK
This parameter defines the oscillation frequency by using the internal resistor, in the B&W mode.
- (Rf2, Rf1, Rf0)=(0,0,0)
- NOTE11) OSC2
- $V_{DD}=3V$ / $T_a=25^\circ C$
- NOTE12) V_{OUT}
This parameter is applied to the condition that the internal LCD power supply and the internal oscillator are used.
- $V_{EE}=2.4V$ to $3.3V$ / EVR= (1,1,1,1,1,1,1) / 1/4 to 1/8 LCD Bias / 1/41 Duty Cycle / No-load on COM/SEG / $RL=500k\Omega$ between V_{OUT} and V_{SSH} / CA1=CA2=1.0uF / CA3=0.1uF / DCON="1" / AMPON="1"
- NOTE13) V_{SS}
This parameter is applied to the condition that the internal LCD power supply and the internal oscillator are used.
- EVR= (1,1,1,1,1,1,1) / All Pixels ON or Checker Flag Display / No-load on COM/SEG / No-access from MPU / $V_{DD}=V_{EE}$ / $V_{REF}=0.9V_{EE}$ / CA1=CA2=1.0uF / CA3=0.1uF / DCON="1" / AMPON="1" / NLIN="0" / 1/41 Duty cycle / $T_a=25^\circ C$
- NOTE14) V_{BA}
- $V_{BA}=V_{REF}$ / Boost Level (N)="1", / DCON="0" / $V_{OUT}=13.5V$
- NOTE15) V_{REG}
- $V_{EE}=2.4V$ to $3.3V$ / $V_{REF}=0.9V_{EE}$ / $V_{OUT}=18V$ / 1/4 to 1/8 LCD bias ratio / 1/41 duty cycle / EVR=(1,1,1,1,1,1,1) / Checker flag display / No-load on COM/SEG / Boost Level (N)="2" to "5" / CA1=CA2=1.0uF / CA3=0.1uF / DCON="0" / AMPON="1" / NLIN="0"
- NOTE16) V_{LCD} , V_1 , V_2 , V_3 and V_4
- $V_{EE}=3.0V$ / $V_{REF}=0.9V_{EE}$ / $V_{OUT}=15V$ / 1/4 to 1/8 LCD Bias / EVR= (1,1,1,1,1,1,1) / Display OFF / No-load on COM/SEG / Boost Level (N)="5" / CA1=CA2=1.0uF / CA3=0.1uF / DCON="0" / AMPON="1"



■ AC CHARACTERISTICS

(1) Write Operation (Parallel Interface / 80-series MPU)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		90		ns	WRb
Enable "L" level pulse width	t_{WRLW8}		35		ns	
Enable "H" level pulse width	t_{WRHW8}		35		ns	
Data setup time	t_{DS8}		30		ns	D ₀ to D ₁₅
Data hold time	t_{DH8}		5		ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

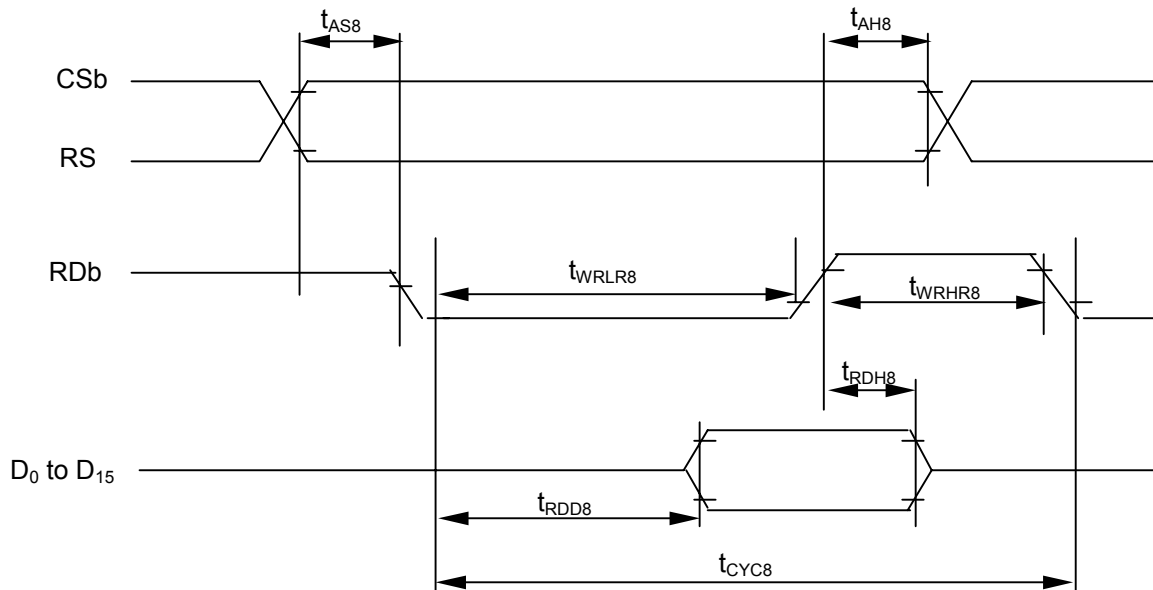
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		160		ns	WRb
Enable "L" level pulse width	t_{WRLW8}		70		ns	
Enable "H" level pulse width	t_{WRHW8}		70		ns	
Data setup time	t_{DS8}		40		ns	D ₀ to D ₁₅
Data hold time	t_{DH8}		5		ns	

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		180		ns	WRb
Enable "L" level pulse width	t_{WRLW8}		80		ns	
Enable "H" level pulse width	t_{WRHW8}		80		ns	
Data setup time	t_{DS8}		70		ns	D ₀ to D ₁₅
Data hold time	t_{DH8}		10		ns	

NOTE) Each timing is specified based on 20% and 80% of V_{DD} .

(2) Read Operation (Parallel Interface / 80-series MPU)



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t _{AH8}		0		ns	CSb
Address setup time	t _{AS8}		0		ns	RS
System cycle time	t _{CYC8}		180		ns	RDb
Enable "L" level pulse width	t _{WRLR8}		80		ns	
Enable "H" level pulse width	t _{WRHR8}		80		ns	
Read Data delay time	t _{RDD8}	CL=15pF	0	60	ns	D ₀ to D ₁₅
Read Data hold time	t _{RDH8}		0		ns	

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

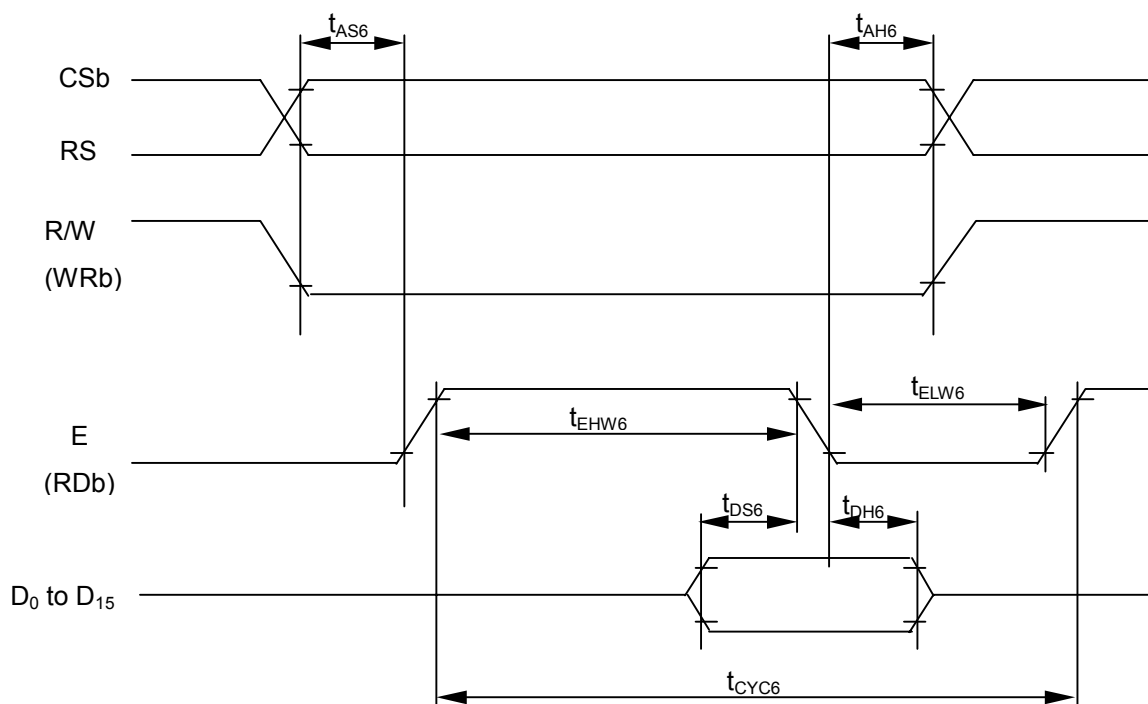
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t _{AH8}		0		ns	CSb
Address setup time	t _{AS8}		0		ns	RS
System cycle time	t _{CYC8}		180		ns	RDb
Enable "L" level pulse width	t _{WRLR8}		80		ns	
Enable "H" level pulse width	t _{WRHR8}		80		ns	
Read Data delay time	t _{RDD8}	CL=15pF	0	60	ns	D ₀ to D ₁₅
Read Data hold time	t _{RDH8}		0		ns	

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t _{AH8}		0		ns	CSb
Address setup time	t _{AS8}		0		ns	RS
System cycle time	t _{CYC8}		250		ns	RDb
Enable "L" level pulse width	t _{WRLR8}		120		ns	
Enable "H" level pulse width	t _{WRHR8}		120		ns	
Read Data delay time	t _{RDD8}	CL=15pF	0	110	ns	D ₀ to D ₁₅
Read Data hold time	t _{RDH8}		0		ns	

NOTE) Each timing is specified based on 20% and 80% of V_{DD}.

(3) Write Operation (Parallel Interface / 68-series MPU)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		90		ns	E
Enable "L" level pulse width	t_{ELW6}		35		ns	
Enable "H" level pulse width	t_{EHW6}		35		ns	
Data setup time	t_{DS6}		40		ns	D ₀ to D ₁₅
Data hold time	t_{DH6}		5		ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

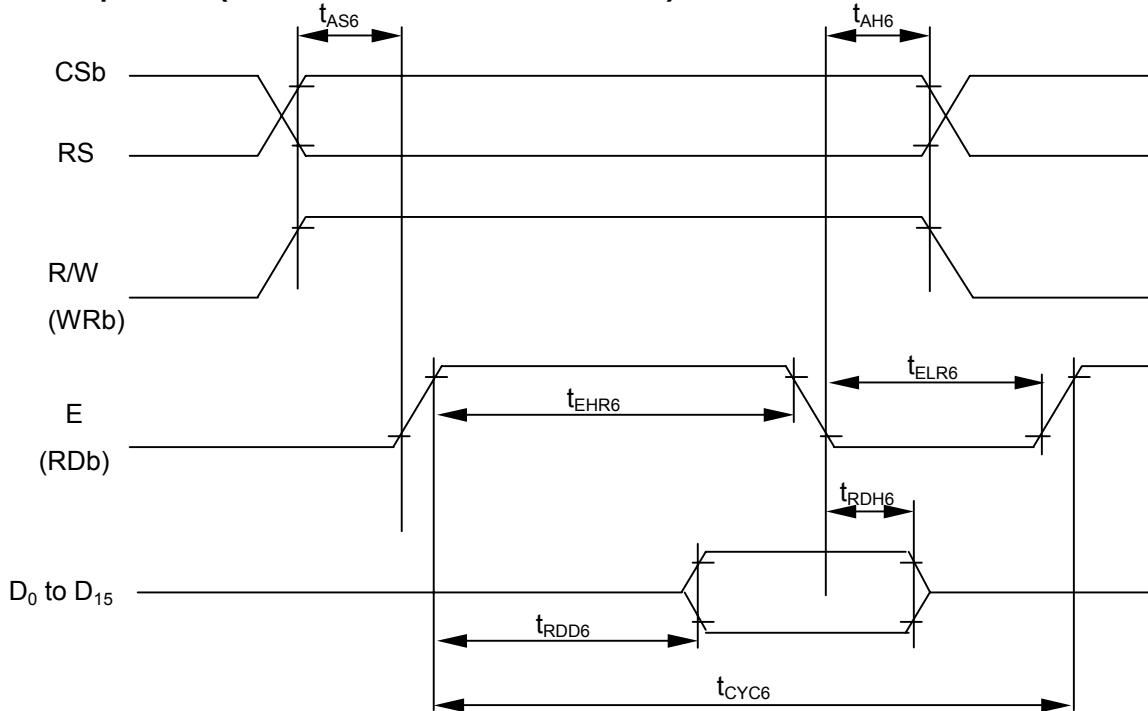
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		160		ns	E
Enable "L" level pulse width	t_{ELW6}		70		ns	
Enable "H" level pulse width	t_{EHW6}		70		ns	
Data setup time	t_{DS6}		50		ns	D ₀ to D ₁₅
Data hold time	t_{DH6}		5		ns	

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		180		ns	E
Enable "L" level pulse width	t_{ELW6}		80		ns	
Enable "H" level pulse width	t_{EHW6}		80		ns	
Data setup time	t_{DS6}		70		ns	D ₀ to D ₁₅
Data hold time	t_{DH6}		10		ns	

NOTE) Each timing is specified based on 20% and 80% of V_{DD} .

(4) Read Operation (Parallel Interface / 68-series MPU)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		180		ns	E
Enable "L" level pulse width	t_{ELR6}		80		ns	
Enable "H" level pulse width	t_{EHR6}		80		ns	
Read Data delay time	t_{RDD6}	CL=15pF	0	70	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH6}				ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

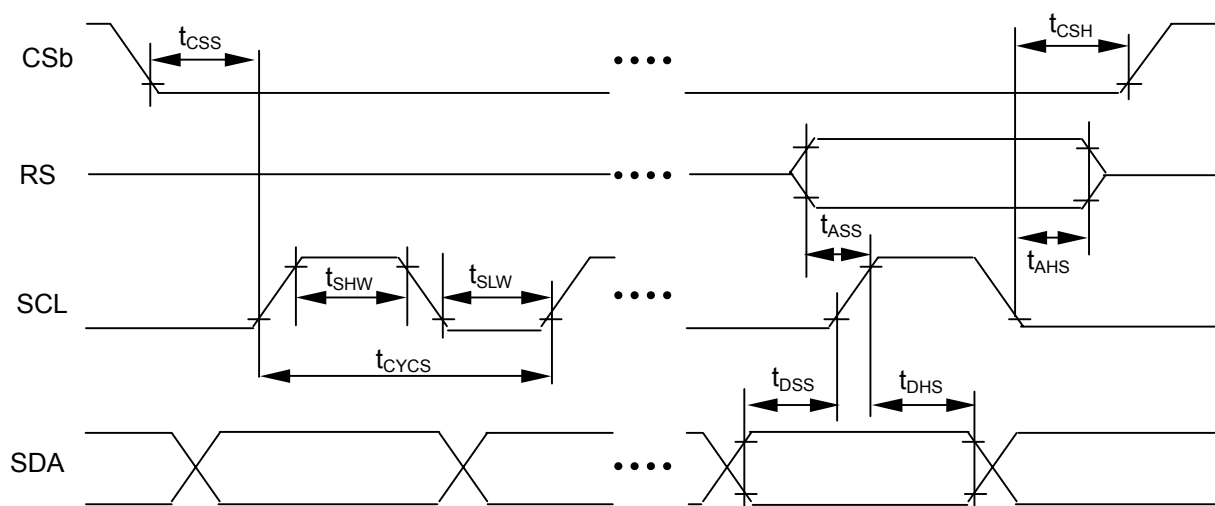
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		180		ns	E
Enable "L" level pulse width	t_{ELR6}		80		ns	
Enable "H" level pulse width	t_{EHR6}		80		ns	
Read Data delay time	t_{RDD6}	CL=15pF	0	70	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH6}				ns	

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		250		ns	E
Enable "L" level pulse width	t_{ELR6}		120		ns	
Enable "H" level pulse width	t_{EHR6}		120		ns	
Read Data delay time	t_{RDD6}	CL=15pF	0	110	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH6}				ns	

NOTE) Each timing is specified based on 20% and 80% of V_{DD} .

(5) Write Operation (Serial Interface)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		50		ns	SCL
SCL "H" level pulse width	t_{SHW}		20		ns	
SCL "L" level pulse width	t_{SLW}		20		ns	
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	
Data setup time	t_{DSS}		20		ns	SDA
Data hold time	t_{DHS}		20		ns	
CSb – SCL time	t_{CSS}		20		ns	CSb
CSb hold time	t_{CSH}		20		ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

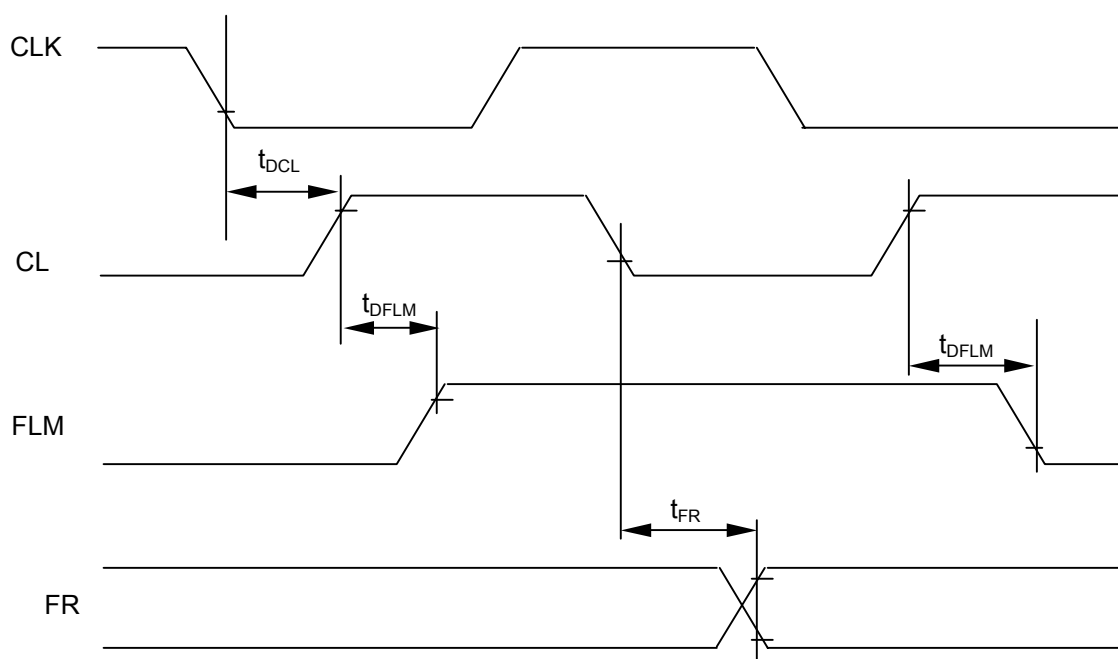
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		50		ns	SCL
SCL "H" level pulse width	t_{SHW}		20		ns	
SCL "L" level pulse width	t_{SLW}		20		ns	
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	
Data setup time	t_{DSS}		20		ns	SDA
Data hold time	t_{DHS}		20		ns	
CSb – SCL time	t_{CSS}		20		ns	CSb
CSb hold time	t_{CSH}		20		ns	

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		80		ns	SCL
SCL "H" level pulse width	t_{SHW}		35		ns	
SCL "L" level pulse width	t_{SLW}		35		ns	
Address setup time	t_{ASS}		35		ns	RS
Address hold time	t_{AHS}		35		ns	
Data setup time	t_{DSS}		35		ns	SDA
Data hold time	t_{DHS}		35		ns	
CSb – SCL time	t_{CSS}		35		ns	CSb
CSb hold time	t_{CSH}		35		ns	

NOTE) Each timing is specified based on 20% and 80% of V_{DD} .

(6) Display Control Timing



Output timing

($V_{DD}=2.4$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	t_{DCLM}	CL=15pF	0	500	ns	FLM
FR delay time	t_{FR}		0	500	ns	FR
CL delay time	t_{DCL}		0	200	ns	CL

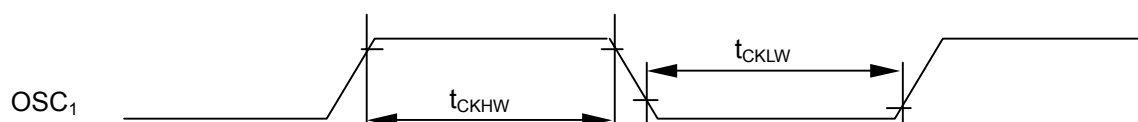
Output timing

($V_{DD}=1.7$ to $2.4V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	t_{DCLM}	CL=15pF	0	1000	ns	FLM
FR delay time	t_{FR}		0	1000	ns	FR
CL delay time	t_{DCL}		0	200	ns	CL

NOTE) Each timing is specified based on 20% and 80% of V_{DD} .

(7) Input Clock Timing



($V_{DD}=1.7$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
OSC1 "H" level pulse width (1)	t_{CKHW1}		2.27	3.29	μs	OSC1 (NOTE2)
OSC1 "L" level pulse width (1)	t_{CKLW1}		2.27	3.29	μs	
OSC1 "H" level pulse width (2)	t_{CKHW2}		10	14.7	μs	OSC1 (NOTE3)
OSC1 "L" level pulse width (2)	t_{CKLW2}		10	14.7	μs	
OSC1 "H" level pulse width (3)	t_{CKHW3}		70	103	μs	OSC1 (NOTE4)
OSC1 "L" level pulse width (3)	t_{CKLW3}		70	103	μs	

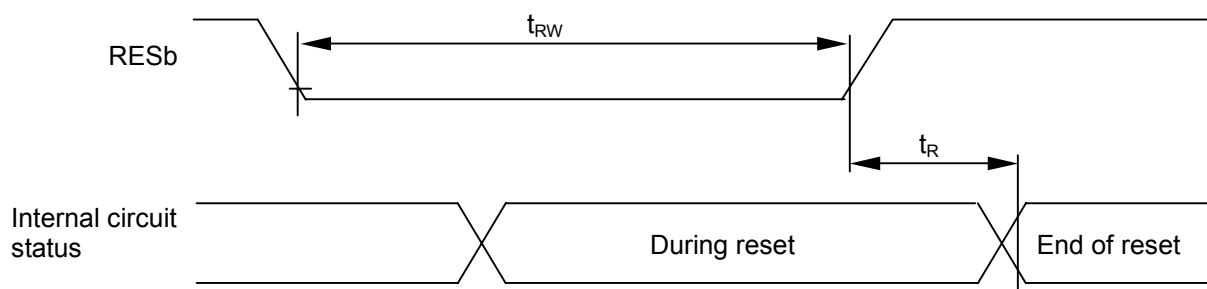
NOTE1) Each timing is specified based on 20% and 80% of V_{DD} .

NOTE2) Applied to Variable 8-/16-level grayscale mode (MON="0", PWM="0")

NOTE3) Applied to fixed 8-level grayscale mode (MON="0", PWM="1")

NOTE4) Applied to B&W mode (MON="1")

(8) Reset Input Timing



($V_{DD}=2.4$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.0	μs	
RESb "L" level pulse width	t_{RW}		10.0		μs	RESb

($V_{DD}=1.7$ to $2.4V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.5	μs	
RESb "L" level pulse width	t_{RW}		10.0		μs	RESb

NOTE) Each timing is specified based on 20% and 80% of V_{DD} .

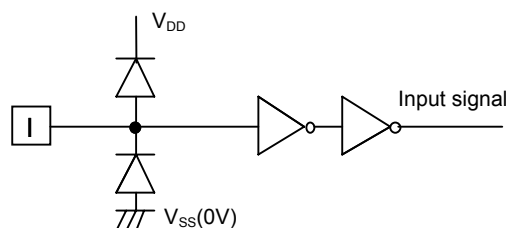
(9) Delay Time of Gate

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Delay time of gate	$T_a=+25^{\circ}C$, $V_{SS}=0V$, $V_{DD}=3.0V$		10		ns

INPUT/OUTPUT BLOCK DIAGRAMS

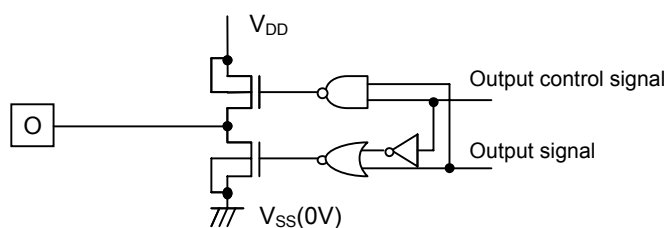
Input Block Diagram

Terminals CSb, RS, RDb, WRb, SEL68, P/S, RESb



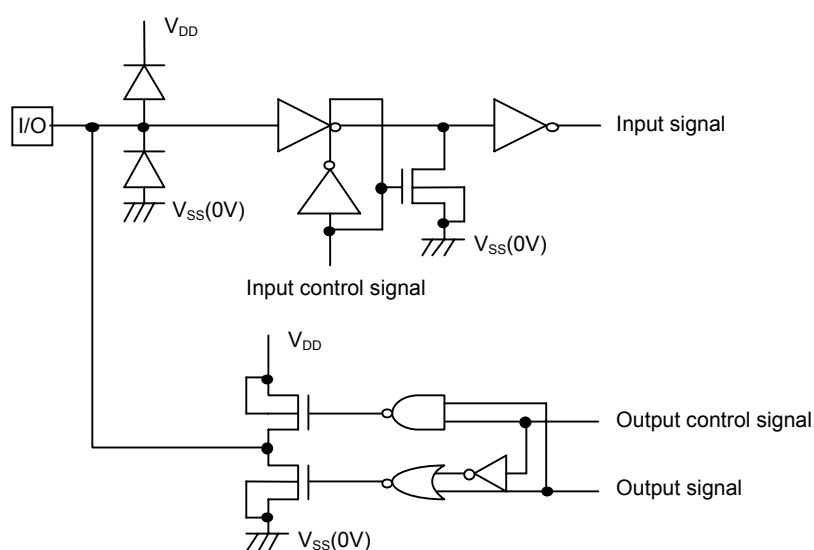
Output Block Diagram

Terminals : FLM, CL, FR, CLK



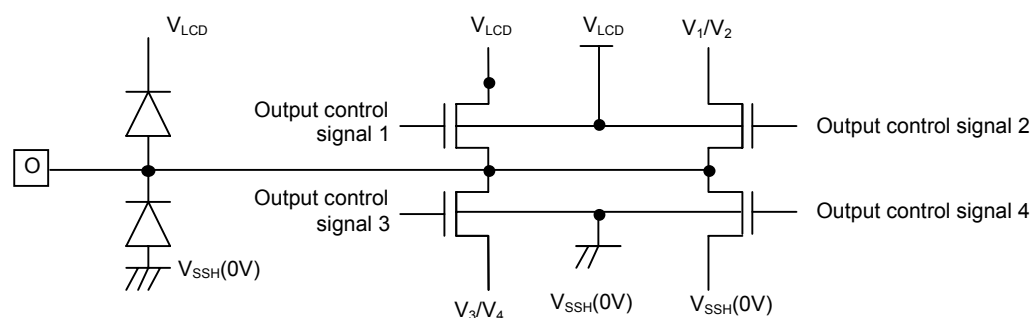
Input/Output Block Diagram

Terminals : D₀ - D₁₅



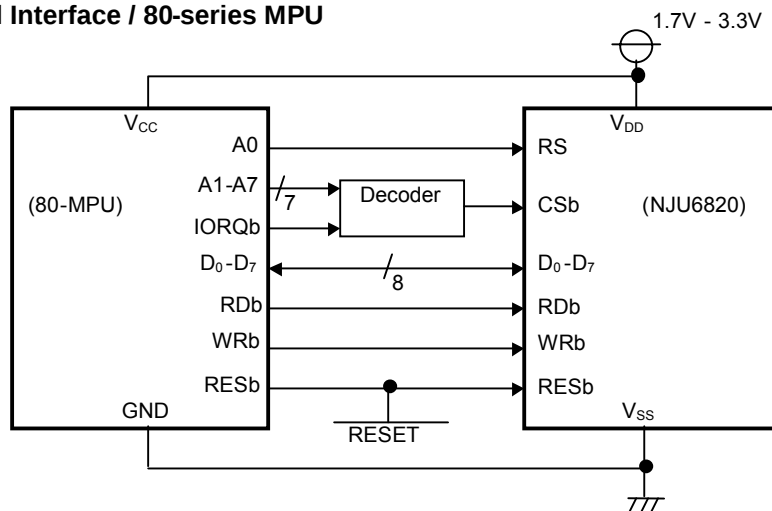
COM/SEG Driver Block Diagram

Terminals : SEGA₀/B₀/C₀ - SEGA₁₂₇/B₁₂₇/C₁₂₇, COM₀ - COM₃₉

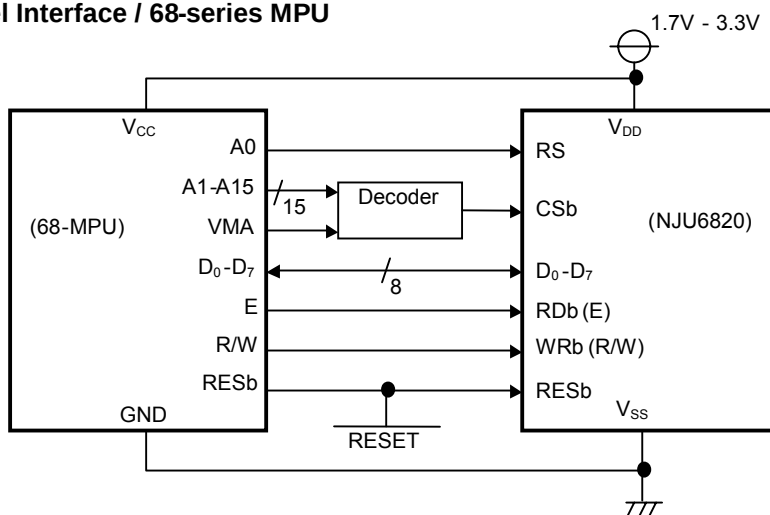


■ MPU CONNECTIONS

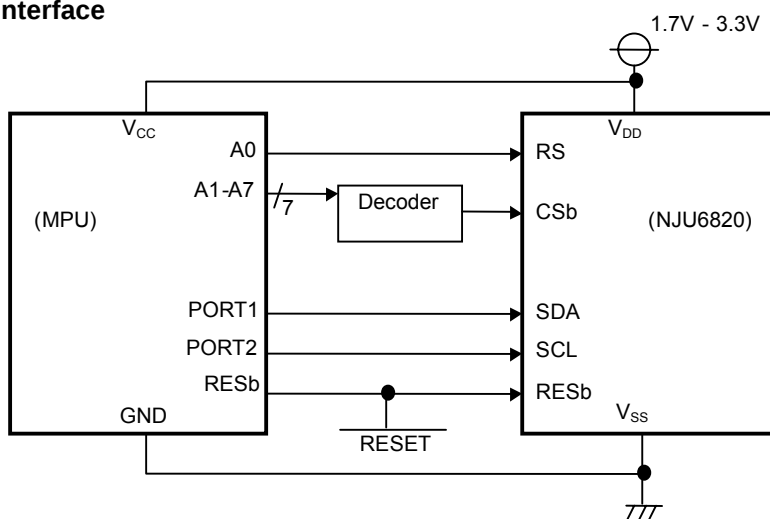
Parallel Interface / 80-series MPU



Parallel Interface / 68-series MPU



Serial Interface



[CAUTION]

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