TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS260A

January 1997

# CD74FCT573, CD74FCT573AT

## BiCMOS FCT Interface Logic, Octal Transparent Latches, Three-State

NOT RECOMMENDED FOR NEW DESIGNS
Use CMOS Technology

### Features

- **Buffered Inputs**
- **Typical Propagation Delay: 3.9ns at $V_{CC}$ = 5V, $T_A$ = 25°C, $C_L$ = 50pF (CD74FCT573AT)**
- **SCR Latchup Resistant BiCMOS Process and Circuit Design**
- **FCTXXX Types**
  - **Speed of Bipolar FAST™/AS/S**
- **FCTXXXAT Types**
  - **30% Faster than FAST™/AS/S with Significantly Reduced Power Consumption**
- **48mA Output Sink Current**
- **Output Voltage Swing Limited to 3.7V at $V_{CC}$ = 5V**
- **Controlled Output Edge Rates**
- **Input/Output Isolation to $V_{CC}$**
- **BiCMOS Technology with Low Quiescent Power**

### Description

The CD74FCT573 and CD74FCT573AT octal transparent latches use a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below $V_{CC}$. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes $V_{CC}$ bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 milliamperes.

The CD74FCT573 and CD74FCT573AT outputs are transparent to the inputs when the Latch Enable ($\overline{LE}$) is HIGH. When the Latch Enable ($\overline{LE}$) goes LOW, the data is latched. The Output Enable ($\overline{OE}$) controls the three-state outputs. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high impedance state. The latch operation is independent of the state of the Output Enable.

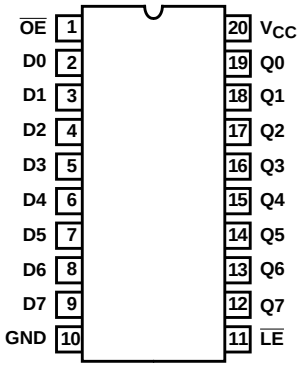
### Ordering Information

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE | PKG. NO. |
|---|---|---|---|
| CD74FCT573ATE | 0 to 70 | 20 Ld PDIP | E20.3 |
| CD74FCT573M | 0 to 70 | 20 Ld SOIC | M20.3 |
| CD74FCT573SM | 0 to 70 | 20 Ld SSOP | M20.209 |

NOTE: When ordering the suffix M and SM packages, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

### Pinout

**CD74FCT573, CD74FCT573AT**
**(PDIP, SOIC, SSOP)**
TOP VIEW




CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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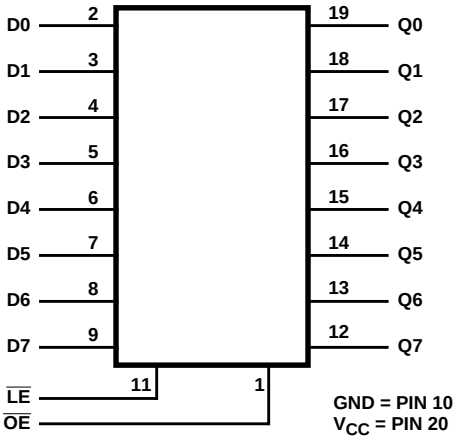
File Number **2304.2**

## Functional Diagram




**TRUTH TABLE** (Note 1)

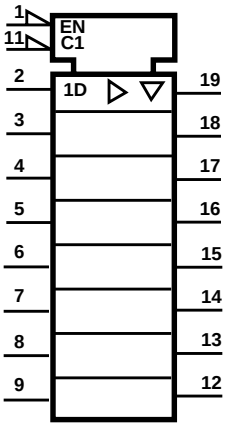
| $\overline{\text{OUTPUT}}$ ENABLE | $\overline{\text{LATCH}}$ ENABLE | DATA | OUTPUT |
|---|---|---|---|
| L | H | H | H |
| L | H | L | L |
| L | L | l | L |
| L | L | h | H |
| H | X | X | Z |

NOTE:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   l = Low voltage level one set up time prior to the high to low latch enable transition.
   h = High voltage level one set up time prior to the high to low latch enable transition.
   X = Irrelevant
   Z = High Impedance

## IEC Logic Symbol

**CD74FCT573, CD74FCT573AT**



## Absolute Maximum Ratings

DC Supply Voltage ($V_{CC}$) . . . . . -0.5V to 6V
DC Input Diode Current, $I_{IK}$ (For $V_I$ < -0.5V) . . . . . -20mA
DC Output Diode Current, $I_{OK}$ (for $V_O$ < -0.5V) . . . . . -50mA
DC Output Sink Current per Output Pin, IO . . . . . 70mA
DC Output Source Current per Output Pin, IO . . . . . -30mA
DC $V_{CC}$ Current ($I_{CC}$) . . . . . 140mA
DC Ground Current ($I_{GND}$) . . . . . 400mA

## Operating Conditions

Operating Temperature Range ($T_A$) . . . . . $0^oC$ to $70^oC$
Supply Voltage Range, $V_{CC}$ . . . . . 4.75V to 5.25V
DC Input Voltage, $V_I$ . . . . . 0 to $V_{CC}$
DC Output Voltage, $V_O$ . . . . . 0 to ≤ $V_{CC}$
Input Rise and Fall Slew Rate, dt/dv . . . . . 0 to 10ns/V

## Thermal Information

| Thermal Resistance (Typical, Note 2) | $\theta_{JA}$ ($^oC/W$) |
|---|---|
| PDIP Package | 135 |
| SOIC Package | 125 |
| SSOP Package | 130 |

Maximum Junction Temperature . . . . . $150^oC$
Maximum Storage Temperature Range . . . . . $-65^oC$ to $150^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^oC$
(SOIC and SSOP-Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

2. $\theta_{JA}$ is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications

Commercial Temperature Range $0^oC$ to $70^oC$, $V_{CC}$ Max = 5.25V, $V_{CC}$ Min = 4.75V (Note 5)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | AMBIENT TEMPERATURE ($T_A$) | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | $25^oC$ | | $0^oC$ TO $70^oC$ | | |
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | MAX | MIN | MAX | |
| High Level Input Voltage | $V_{IH}$ | | | 4.75 to 5.25 | 2 | - | 2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | | | 4.75 to 5.25 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -15 | Min | 2.4 | - | 2.4 | - | V |
| Low Level Output Voltage | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 48 | Min | - | 0.55 | - | 0.55 | V |
| High Level Input Current | $I_{IH}$ | $V_{CC}$ | | Max | - | 0.1 | - | 1 | µA |
| Low Level Input Current | $I_{IL}$ | GND | | Max | - | -0.1 | - | -1 | µA |
| Three-State Leakage Current | $I_{OZH}$ | $V_{CC}$ | | Max | - | 0.5 | - | 10 | µA |
| | $I_{OZL}$ | GND | | Max | - | -0.5 | - | -10 | µA |
| Input Clamp Voltage | $V_{IK}$ | $V_{CC}$ or GND | -18 | Min | - | -1.2 | - | -1.2 | V |
| Short Circuit Output Current (Note 3) | $I_{OS}$ | $V_O$ = 0 $V_{CC}$ or GND | | Max | -60 | - | -60 | - | mA |
| Quiescent Supply Current, MSI | $I_{CC}$ | $V_{CC}$ or GND | 0 | Max | - | 8 | - | 80 | µA |
| Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load | $\Delta I_{CC}$ | 3.4V (Note 4) | | Max | - | 1.6 | - | 1.6 | mA |

NOTES:

3. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
4. Inputs that are not measured are at $V_{CC}$ or GND.
5. FCT Input Loading: All inputs are 1 unit load. Unit load is $\Delta I_{CC}$ limit specified in Electrical Specifications table, e.g., 1.6mA Max. at $70^oC$.

## Switching Specifications Over Operating Range FCT Series $t_r$, $t_f$ = 2.5ns, $C_L$ = 50pF, $R_L$ (Figure 4) (Note 6)

| PARAMETER | SYMBOL | $V_{CC}$ (V) | 25°C | 0°C TO 70°C | | UNITS |
|---|---|---|---|---|---|---|
| | | | TYP | MIN | MAX | |
| Propagation Delays | | | | | | |
| Data to Outputs | | | | | | |
| CD74FCT573 | $t_{PLH}$, $t_{PHL}$ | 5 | 5 | 1.5 | 8 | ns |
| CD74FCT573AT | $t_{PLH}$, $t_{PHL}$ | 5 | 3.9 | 1.5 | 5.7 | ns |
| $\overline{LE}$ to Outputs | | | | | | |
| CD74FCT573 | $t_{PLH}$, $t_{PHL}$ | 5 | 9 | 2 | 13 | ns |
| CD74FCT573AT | $t_{PLH}$, $t_{PHL}$ | 5 | 4.4 | 2 | 7 | ns |
| Output Enable Times | | | | | | |
| CD74FCT573 | $t_{PZL}$, $t_{PZH}$ | 5 | 7 | 1.5 | 12 | ns |
| CD74FCT573AT | $t_{PZL}$, $t_{PZH}$ | 5 | 6 | 1.5 | 8 | ns |
| Output Disable Times | | | | | | |
| CD74FCT573 | $t_{PLZ}$, $t_{PHZ}$ | 5 | 6 | 1.5 | 7.5 | ns |
| CD74FCT573AT | $t_{PLZ}$, $t_{PHZ}$ | 5 | 4 | 1.5 | 5.8 | ns |
| Power Dissipation Capacitance | $C_{PD}$ (Note 7) | - | 34 | - | - | pF |
| Minimum (Valley) $V_{OHV}$ During Switching of Other Outputs (Output Under Test Not Switching) | $V_{OHV}$ (Figure 1) | 5 | 0.5 | - | - | V |
| Maximum (Peak) $V_{OLP}$ During Switching of Other Outputs (Output Under Test Not Switching) | $V_{OLP}$ (Figure 1) | 5 | 1 | - | - | V |
| Input Capacitance | $C_I$ | - | - | - | 10 | pF |
| Three-State Output Capacitance | $C_O$ | - | - | - | 15 | pF |

NOTES:

6. 5V: Min is at 5.25V for 0°C to 70°C, Max is at 4.75V for 0°C to 70°C, Typ is at 5V.
7. $C_{PD}$, measured per flip-flop, is used to determine the dynamic power consumption.
   $P_D$ (per package) = $V_{CC}$ $I_{CC}$ + $\Sigma(V_{CC}^2$ $f_I$ $C_{PD}$ + $V_O^2$ $f_O$ $C_L$ + $V_{CC}$ $\Delta I_{CC}$ D) where:
   $V_{CC}$ = supply voltage
   $\Delta I_{CC}$ = flow through current x unit load
   $C_L$ = output load capacitance
   D = duty cycle of input high
   $f_O$ = output frequency
   $f_I$ = input frequency

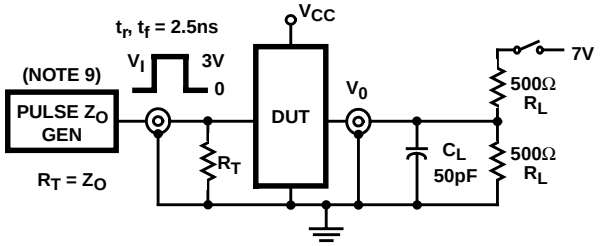
## Prerequisite for Switching

| PARAMETER | SYMBOL | $V_{CC}$ (V) | 25°C | 0°C TO 70°C | | UNITS |
|---|---|---|---|---|---|---|
| | | | TYP | MIN | MAX | |
| Data to Latch Enable Setup Time | $t_{SU}$ | 5 (Note 8) | - | 2 | - | ns |
| Data to Latch Enable Hold Time | $t_H$ | 5 | - | 1.5 | - | ns |
| Latch Enable Pulse Width | | | | | | |
| CD74FCT573 | $t_W$ | 5 | - | 6 | - | ns |
| CD74FCT573AT | $t_W$ | 5 | - | 5 | - | ns |

NOTE:

8. 5V: Minimum is at 4.75V for 0°C to 70°C, Typical is at 5V.

## Test Circuits and Waveforms




NOTE:

9. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_{OUT}$ ≤ 50Ω; $t_f$, $t_r$ ≤ 2.5ns.

**FIGURE 1. TEST CIRCUIT**

**SWITCH POSITION**

| TEST | SWITCH |
|---|---|
| $t_{PLZ}$, $t_{PZL}$, Open Drain | Closed |
| $t_{PHZ}$, $t_{PZH}$, $t_{PLH}$, $t_{PHL}$ | Open |

DEFINITIONS:

$C_L$ = Load capacitance, includes jig and probe capacitance.

$R_T$ = Termination resistance, should be equal to $Z_{OUT}$ of the Pulse Generator.

$V_{IN}$ = 0V to 3V.

Input: $t_r = t_f$ = 2.5ns (10% to 90%), unless otherwise specified

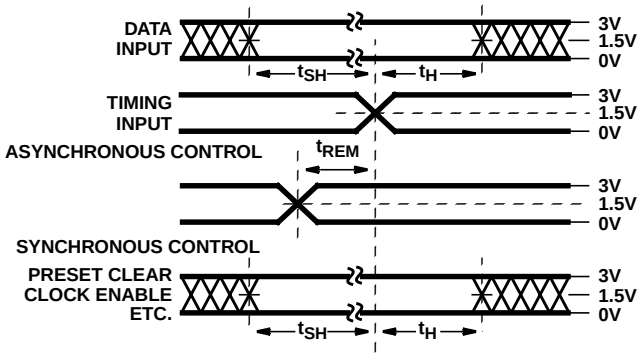



**FIGURE 2. SETUP, HOLD, AND RELEASE TIMING**

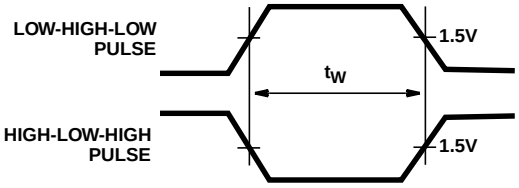



**FIGURE 3. PULSE WIDTH**

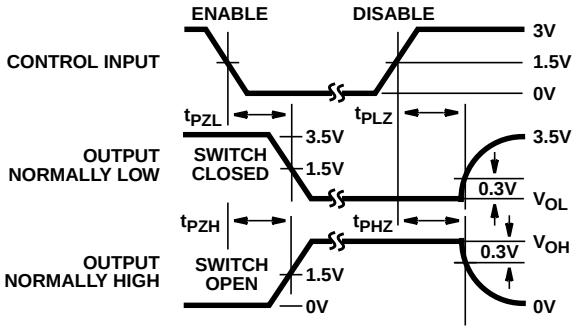



**FIGURE 4. ENABLE AND DISABLE TIMING**

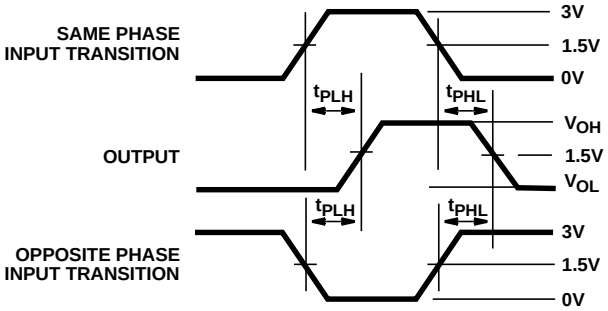
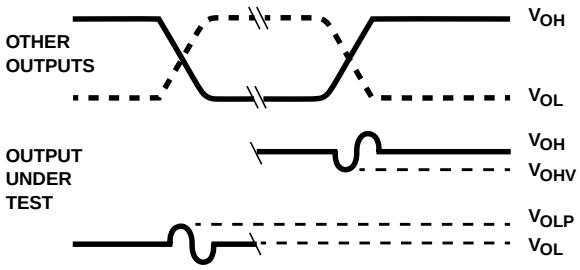



**FIGURE 5. PROPAGATION DELAY**

## *Test Circuits and Waveforms* (Continued)




NOTES:

10. $V_{OLP}$ is measured with respect to a ground reference near the output under test. $V_{OHV}$ is measured with respect to $V_{OH}$.
11. Input pulses have the following characteristics:
    $P_{RR} \leq 1MHz$, $t_r = 2.5ns$, $t_f = 2.5ns$, skew 1ns.
12. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700MHz bandwidth.

**FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS**

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