

# Fault Protected, Extended CMR, RS-485/RS-422 Transceivers with Cable Invert and $\pm 16.5\text{kV}$ ESD

## ISL32483E, ISL32485E

The ISL3248xE are fault protected, 5V powered differential transceivers that exceed the RS-485 and RS-422 standards for balanced communication. The RS-485 transceiver pins (driver outputs and receiver inputs) are fault protected up to  $\pm 60\text{V}$  and are protected against  $\pm 16.5\text{kV}$  ESD strikes without latch-up. Additionally, the extended common mode range allows these transceivers to operate in environments with common mode voltages up to  $\pm 25\text{V}$  ( $>2\times$  the RS-485 requirement), making this fault-protected RS-485 family one of the most robust on the market.

Transmitters (Tx) deliver an exceptional 2.5V (typical) differential output voltage into the RS-485 specified  $54\Omega$  load. This yields better noise immunity than standard RS-485 ICs or allows up to six  $120\Omega$  terminations in star network topologies.

Receiver (Rx) inputs feature a "Full Fail-Safe" design, which ensures a logic high Rx output if Rx inputs are floating, shorted, or on a terminated but undriven (idle) bus.

The ISL32483E and ISL32485E include cable invert functions that reverse the polarity of the Rx and/or Tx bus pins in case the cable is misconnected. Unlike competing devices, Rx full fail-safe operation is maintained even when the Rx input polarity is switched.

For fault protected RS-485 transceivers without the cable invert function, please see the [ISL32470E](#) and [ISL32490E](#) data sheets.

## Features

- Fault Protected RS-485 Bus Pins . . . . . Up to  $\pm 60\text{V}$
- Extended Common Mode Range . . . . .  $\pm 25\text{V}$   
More Than Twice the Range Required for RS-485
- $\pm 16.5\text{kV}$  HBM ESD Protection on RS-485 Bus Pins
- Cable Invert Pins  
Corrects for Reversed Cable Connections While Maintaining Rx Full Fail-Safe Functionality
- Full Fail-Safe (Open, Short, Terminated) RS-485 Receivers
- 1/4 Unit Load (UL) for Up to 128 Devices on the Bus
- High Rx  $I_{OL}$  for Opto-Couplers in Isolated Designs
- Hot Plug Circuitry: Tx and Rx Outputs Remain Three-State During Power-up/Power-down
- Slew Rate Limited RS-485 Data Rate . . . . . 1Mbps
- Low Quiescent Supply Current . . . . . 2.3mA
- Ultra Low Shutdown Supply Current . . . . .  $10\mu\text{A}$

## Applications

- Utility Meters/Automated Meter Reading Systems
- High Node Count RS-485 Systems
- PROFIBUS® and RS-485 Based Field Bus Networks, and Factory Automation
- Security Camera Networks
- Building Lighting and Environmental Control Systems
- Industrial/Process Control Networks

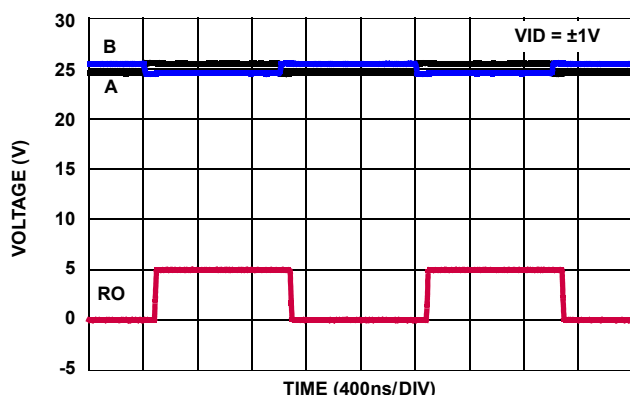


FIGURE 1. EXCEPTIONAL Rx OPERATES AT 1Mbps EVEN WITH  $\pm 25\text{V}$  COMMON MODE VOLTAGE

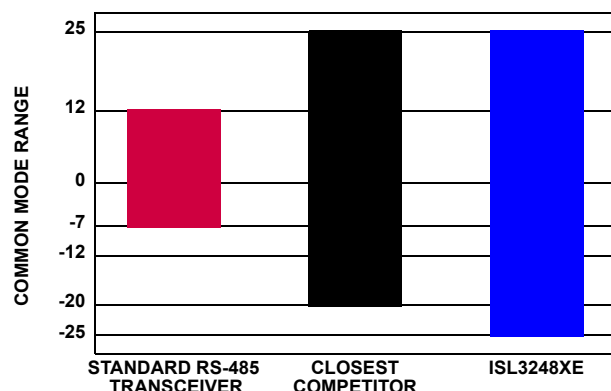


FIGURE 2. TRANSCEIVERS DELIVER SUPERIOR COMMON MODE RANGE vs STANDARD RS-485 DEVICES

# ISL32483E, ISL32485E

TABLE 1. SUMMARY OF FEATURES

| PART NUMBER | HALF/FULL DUPLEX | DATA RATE (Mbps) | SLEW-RATE LIMITED? | EN PINS? | HOT PLUG | POLARITY REVERSAL PINS? | QUIESCENT $I_{CC}$ (mA) | LOW POWER SHDN? | PIN COUNT |
|-------------|------------------|------------------|--------------------|----------|----------|-------------------------|-------------------------|-----------------|-----------|
| ISL32483E   | Full             | 1                | Yes                | Yes      | Yes      | Yes                     | 2.3                     | Yes             | 14        |
| ISL32485E   | Half             | 1                | Yes                | Tx Only  | Yes      | Yes                     | 2.3                     | No              | 8         |

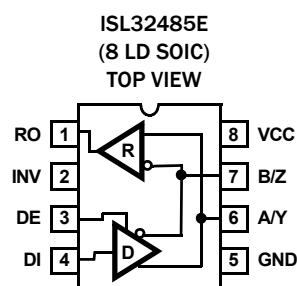
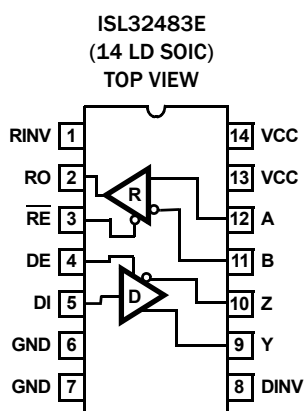
## Ordering Information

| PART NUMBER<br>(Notes 1, 2, 3) | PART MARKING  | TEMP. RANGE<br>(°C) | PACKAGE<br>(Pb-Free) | PKG.<br>DWG. # |
|--------------------------------|---------------|---------------------|----------------------|----------------|
| ISL32483EIBZ                   | ISL32483 EIBZ | -40 to +85          | 14 Ld SOIC           | M14.15         |
| ISL32485EIBZ                   | 32485 EIBZ    | -40 to +85          | 8 Ld SOIC            | M8.15          |

### NOTES:

1. Add "-T\*" suffix for tape and reel. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for [ISL32483E](#) and [ISL32485E](#). For more information on MSL please see techbrief [TB363](#).

## Pin Configurations



## Pin Descriptions

| PIN NAME               | ISL32483E PIN # | ISL32485E PIN # | FUNCTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------------------------|-----------------|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RO                     | 2               | 1               | Receiver output. If INV or RINV is low, then: If $A - B \geq -10\text{mV}$ , RO is high; if $A - B \leq -200\text{mV}$ , RO is low. If INV or RINV is high, then: If $B - A \geq -10\text{mV}$ , RO is high; if $B - A \leq -200\text{mV}$ , RO is low. In all cases, RO = High if A and B are unconnected (floating), or shorted together, or connected to an undriven, terminated bus (i.e., Rx is always failsafe open, shorted, and idle, even if polarity is inverted). |
| $\overline{\text{RE}}$ | 3               | N/A             | Receiver output enable. RO is enabled when $\overline{\text{RE}}$ is low; RO is high impedance when $\overline{\text{RE}}$ is high. Internally pulled low.                                                                                                                                                                                                                                                                                                                   |
| DE                     | 4               | 3               | Driver output enable. The driver outputs, Y and Z, are enabled by bringing DE high, and they are high impedance when DE is low. Internally pulled high to V <sub>CC</sub> .                                                                                                                                                                                                                                                                                                  |
| DI                     | 5               | 4               | Driver input. If INV or DINV is low, a low on DI forces output Y low and output Z high, while a high on DI forces output Y high and output Z low. The output states relative to DI invert if INV or DINV is high.                                                                                                                                                                                                                                                            |
| GND                    | 6, 7            | 5               | Ground connection.                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| A/Y                    | N/A             | 6               | $\pm 60\text{V}$ Fault and $\pm 16.5\text{kV}$ HBM ESD Protected RS-485/RS-422 level I/O pin. If INV is low, A/Y is the non-inverting receiver input and non-inverting driver output. If INV is high, A/Y is the inverting receiver input and the inverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1.                                                                                                                                            |
| B/Z                    | N/A             | 7               | $\pm 60\text{V}$ Fault and $\pm 16.5\text{kV}$ HBM ESD Protected RS-485/RS-422 level I/O pin. If INV is low, B/Z is the inverting receiver input and inverting driver output. If INV is high, B/Z is the non-inverting receiver input and the non-inverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1.                                                                                                                                            |
| A                      | 12              | N/A             | $\pm 60\text{V}$ Fault and $\pm 15\text{kV}$ HBM ESD Protected RS-485/RS-422 level input. If RINV is low, then A is the non-inverting receiver input. If RINV is high, then A is the inverting receiver input.                                                                                                                                                                                                                                                               |
| B                      | 11              | N/A             | $\pm 60\text{V}$ Fault and $\pm 15\text{kV}$ HBM ESD Protected RS-485/RS-422 level input. If RINV is low, then B is the inverting receiver input. If RINV is high, then B is the non-inverting receiver input.                                                                                                                                                                                                                                                               |
| Y                      | 9               | N/A             | $\pm 60\text{V}$ Fault and $\pm 15\text{kV}$ HBM ESD Protected RS-485/RS-422 level output. If DINV is low, then Y is the non-inverting driver output. If DINV is high, then Y is the inverting driver output                                                                                                                                                                                                                                                                 |
| Z                      | 10              | N/A             | $\pm 60\text{V}$ Fault and $\pm 15\text{kV}$ HBM ESD Protected RS-485/RS-422 level. If DINV is low, then Z is the inverting driver output. If DINV is high, then Z is the non-inverting driver output                                                                                                                                                                                                                                                                        |
| VCC                    | 13, 14          | 8               | System power supply input (4.5V to 5.5V).                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| INV                    | N/A             | 2               | Receiver and driver polarity selection input. When driven high, this pin swaps the polarity of the driver output and receiver input pins. If unconnected (floating) or connected low, normal RS-485 polarity conventions apply. Internally pulled low.                                                                                                                                                                                                                       |
| RINV                   | 1               | N/A             | Receiver polarity selection input. When driven high, this pin swaps the polarity of the receiver input pins. If unconnected (floating) or connected low, normal RS-485 polarity conventions apply. Internally pulled low.                                                                                                                                                                                                                                                    |
| DINV                   | 8               | N/A             | Driver polarity selection input. When driven high, this pin swaps the polarity of the driver output pins. If unconnected (floating) or connected low, normal RS-485 polarity conventions apply. Internally pulled low.                                                                                                                                                                                                                                                       |

## Truth Tables

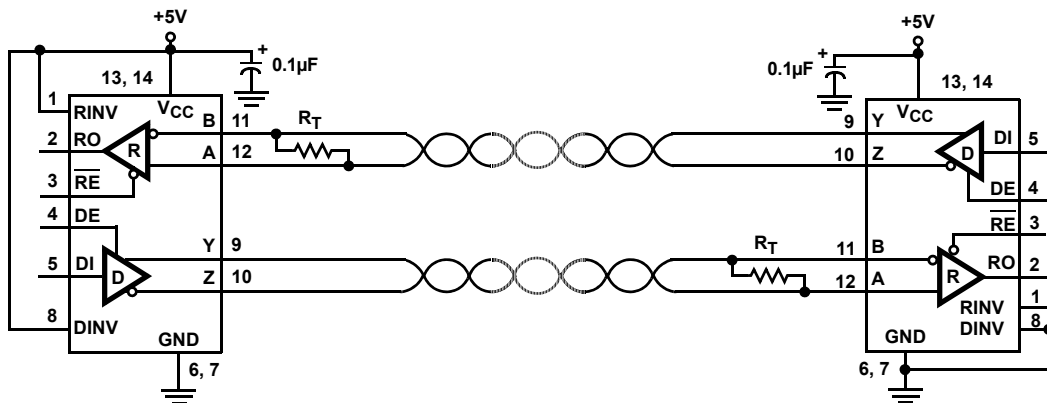
| TRANSMITTING    |    |    |             |                   |                   |
|-----------------|----|----|-------------|-------------------|-------------------|
| INPUTS          |    |    |             | OUTPUTS           |                   |
| $\overline{RE}$ | DE | DI | INV or DINV | Y                 | Z                 |
| X               | 1  | 1  | 0           | 1                 | 0                 |
| X               | 1  | 0  | 0           | 0                 | 1                 |
| X               | 1  | 1  | 1           | 0                 | 1                 |
| X               | 1  | 0  | 1           | 1                 | 0                 |
| 0               | 0  | X  | X           | High-Z            | High-Z            |
| 1               | 0  | X  | X           | High-Z (see Note) | High-Z (see Note) |

NOTE: Low Power Shutdown Mode (see Note 11 on page 7), except for ISL32485E.

| RECEIVING       |                  |                  |                        |             |                   |
|-----------------|------------------|------------------|------------------------|-------------|-------------------|
| INPUTS          |                  |                  |                        |             | OUTPUT            |
| $\overline{RE}$ | DE (Half Duplex) | DE (Full Duplex) | A-B                    | INV or RINV | RO                |
| 0               | 0                | X                | $\geq -0.01V$          | 0           | 1                 |
| 0               | 0                | X                | $\leq -0.2V$           | 0           | 0                 |
| 0               | 0                | X                | $\leq 0.01V$           | 1           | 1                 |
| 0               | 0                | X                | $\geq 0.2V$            | 1           | 0                 |
| 0               | 0                | X                | Inputs Open or Shorted | X           | 1                 |
| 1               | 0                | 0                | X                      | X           | High-Z (see Note) |
| 1               | 1                | 1                | X                      | X           | High-Z            |

NOTE: Low Power Shutdown Mode (see Note 11 on page 7), except for ISL32485E.

## Typical Operating Circuits



THE IC ON THE LEFT HAS THE CABLE CONNECTIONS SWAPPED, SO THE INV PINS (1, 8) ARE STRAPPED HIGH TO INVERT ITS RX AND TX POLARITY

ISL34183E FULL DUPLEX EXAMPLE

# ISL32483E, ISL32485E

## Absolute Maximum Ratings

|                                                |                                   |
|------------------------------------------------|-----------------------------------|
| V <sub>CC</sub> to Ground                      | 7V                                |
| Input Voltages                                 |                                   |
| DI, INV, RINV, DINV, DE, $\overline{RE}$       | -0.3V to (V <sub>CC</sub> + 0.3V) |
| Input/Output Voltages                          |                                   |
| A/Y, B/Z, A, B, Y, Z                           | ±60V                              |
| A/Y, B/Z, A, B, Y, Z                           |                                   |
| (Transient Pulse Through 100Ω, see Note 15)    | ±80V                              |
| RO                                             | -0.3V to (V <sub>CC</sub> + 0.3V) |
| Short Circuit Duration                         |                                   |
| Y, Z                                           | Indefinite                        |
| ESD Rating                                     | see "ESD PERFORMANCE" on page 6   |
| Latch-up (Tested per JESD78, Level 2, Class A) | +125°C                            |

## Thermal Information

|                                                |                                                                                                                 |                      |
|------------------------------------------------|-----------------------------------------------------------------------------------------------------------------|----------------------|
| Thermal Resistance (Typical)                   | $\theta_{JA}$ (°C/W)                                                                                            | $\theta_{JC}$ (°C/W) |
| 8 Ld SOIC Package (Notes 4, 5)                 | 108                                                                                                             | 47                   |
| 14 Ld SOIC Package (Notes 4, 5)                | 88                                                                                                              | 39                   |
| Maximum Junction Temperature (Plastic Package) | +150°C                                                                                                          |                      |
| Maximum Storage Temperature Range              | -65°C to +150°C                                                                                                 |                      |
| Pb-free Reflow Profile                         | see link below                                                                                                  |                      |
|                                                | <a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a> |                      |

## Recommended Operating Conditions

|                                   |                |
|-----------------------------------|----------------|
| Supply Voltage (V <sub>CC</sub> ) | 5V             |
| Temperature Range                 | -40°C to +85°C |
| Bus Pin Common Mode Voltage Range | -25V to +25V   |

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

### NOTES:

4.  $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief [TB379](#) for details.
5. For  $\theta_{JC}$ , the "case temp" location is taken at the package top center.

**Electrical Specifications** Test Conditions: V<sub>CC</sub> = 4.5V to 5.5V; Unless Otherwise Specified. Typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = +25°C (Note 6). **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

| PARAMETER                                                                                   | SYMBOL            | TEST CONDITIONS                                                                               | TEMP (°C) | MIN (Note 14) | TYP | MAX (Note 14)   | UNITS |
|---------------------------------------------------------------------------------------------|-------------------|-----------------------------------------------------------------------------------------------|-----------|---------------|-----|-----------------|-------|
| <b>DC CHARACTERISTICS</b>                                                                   |                   |                                                                                               |           |               |     |                 |       |
| Driver Differential V <sub>OUT</sub> (No load)                                              | V <sub>OD1</sub>  |                                                                                               | Full      | -             | -   | V <sub>CC</sub> | V     |
| Driver Differential V <sub>OUT</sub> (Loaded, Figure 3A)                                    | V <sub>OD2</sub>  | R <sub>L</sub> = 100Ω (RS-422)                                                                | Full      | <b>2.4</b>    | 3.2 | -               | V     |
|                                                                                             |                   | R <sub>L</sub> = 54Ω (RS-485)                                                                 | Full      | <b>1.5</b>    | 2.5 | V <sub>CC</sub> | V     |
|                                                                                             |                   | R <sub>L</sub> = 54Ω (PROFIBUS, V <sub>CC</sub> ≥ 5V)                                         | Full      | <b>2.0</b>    | 2.5 | -               | V     |
|                                                                                             |                   | R <sub>L</sub> = 21Ω (Six 120Ω terminations for Star Configurations, V <sub>CC</sub> ≥ 4.75V) | Full      | <b>0.8</b>    | 1.3 | -               | V     |
| Change in Magnitude of Driver Differential V <sub>OUT</sub> for Complementary Output States | ΔV <sub>OD</sub>  | R <sub>L</sub> = 54Ω or 100Ω (Figure 3A)                                                      | Full      | -             | -   | <b>0.2</b>      | V     |
| Driver Differential V <sub>OUT</sub> with Common Mode Load (Figure 3B)                      | V <sub>OD3</sub>  | R <sub>L</sub> = 60Ω, -7V ≤ V <sub>CM</sub> ≤ 12V                                             | Full      | <b>1.5</b>    | 2.1 | V <sub>CC</sub> | V     |
|                                                                                             |                   | R <sub>L</sub> = 60Ω, -25V ≤ V <sub>CM</sub> ≤ 25V (V <sub>CC</sub> ≥ 4.75V)                  | Full      | <b>1.7</b>    | 2.3 |                 | V     |
|                                                                                             |                   | R <sub>L</sub> = 21Ω, -15V ≤ V <sub>CM</sub> ≤ 15V (V <sub>CC</sub> ≥ 4.75V)                  | Full      | <b>0.8</b>    | 1.1 | -               | V     |
| Driver Common-Mode V <sub>OUT</sub> (Figure 3)                                              | V <sub>OC</sub>   | R <sub>L</sub> = 54Ω or 100Ω                                                                  | Full      | <b>-1</b>     | -   | <b>3</b>        | V     |
|                                                                                             |                   | R <sub>L</sub> = 60Ω or 100Ω, -20V ≤ V <sub>CM</sub> ≤ 20V                                    | Full      | <b>-2.5</b>   | -   | <b>5</b>        | V     |
| Change in Magnitude of Driver Common-Mode V <sub>OUT</sub> for Complementary Output States  | DV <sub>OC</sub>  | R <sub>L</sub> = 54Ω or 100Ω (Figure 3A)                                                      | Full      | -             | -   | <b>0.2</b>      | V     |
| Driver Short-Circuit Current                                                                | I <sub>OSD</sub>  | DE = V <sub>CC</sub> , -25V ≤ V <sub>O</sub> ≤ 25V (Note 8)                                   | Full      | <b>-250</b>   | -   | <b>250</b>      | mA    |
|                                                                                             | I <sub>OSD1</sub> | At First Fold-back, 22V ≤ V <sub>O</sub> ≤ -22V                                               | Full      | <b>-83</b>    |     | <b>83</b>       | mA    |
|                                                                                             | I <sub>OSD2</sub> | At Second Fold-back, 35V ≤ V <sub>O</sub> ≤ -35V                                              | Full      | <b>-13</b>    |     | <b>13</b>       | mA    |
| Logic Input High Voltage                                                                    | V <sub>IH</sub>   | DE, DI, $\overline{RE}$ , INV, RINV, DINV                                                     | Full      | <b>2.5</b>    | -   | -               | V     |
| Logic Input Low Voltage                                                                     | V <sub>IL</sub>   | DE, DI, $\overline{RE}$ , INV, RINV, DINV                                                     | Full      | -             | -   | <b>0.8</b>      | V     |
| Logic Input Current                                                                         | I <sub>IN1</sub>  | DI                                                                                            | Full      | <b>-1</b>     | -   | <b>1</b>        | μA    |
|                                                                                             |                   | DE, $\overline{RE}$ , INV, RINV, DINV                                                         | Full      | <b>-15</b>    | 6   | <b>15</b>       | μA    |

# ISL32483E, ISL32485E

**Electrical Specifications** Test Conditions:  $V_{CC} = 4.5V$  to  $5.5V$ ; Unless Otherwise Specified. Typicals are at  $V_{CC} = 5V$ ,  $T_A = +25^\circ C$  (Note 6).  
**Boldface limits apply over the operating temperature range,  $-40^\circ C$  to  $+85^\circ C$ . (Continued)**

| PARAMETER                                                    | SYMBOL                              | TEST CONDITIONS                                                                 |                                     | TEMP<br>(°C) | MIN<br>(Note 14)      | TYP   | MAX<br>(Note 14) | UNITS |
|--------------------------------------------------------------|-------------------------------------|---------------------------------------------------------------------------------|-------------------------------------|--------------|-----------------------|-------|------------------|-------|
| Input/Output Current (A/Y,<br>B/Z)                           | I <sub>IN2</sub>                    | DE = 0V,<br>V <sub>CC</sub> = 0V or 5.5V                                        | V <sub>IN</sub> = 12V               | Full         | -                     | 110   | 250              | μA    |
|                                                              |                                     |                                                                                 | V <sub>IN</sub> = -7V               | Full         | -200                  | -75   | -                | μA    |
|                                                              |                                     |                                                                                 | V <sub>IN</sub> = ±25V              | Full         | -800                  | ±240  | 800              | μA    |
|                                                              |                                     |                                                                                 | V <sub>IN</sub> = ±60V<br>(Note 17) | Full         | -6                    | ±0.7  | 6                | mA    |
| Input Current (A, B)<br>(Full Duplex Versions Only)          | I <sub>IN3</sub>                    | V <sub>CC</sub> = 0V or 5.5V                                                    | V <sub>IN</sub> = 12V               | Full         | -                     | 90    | 125              | μA    |
|                                                              |                                     |                                                                                 | V <sub>IN</sub> = -7V               | Full         | -100                  | -70   | -                | μA    |
|                                                              |                                     |                                                                                 | V <sub>IN</sub> = ±25V              | Full         | -500                  | ±200  | 500              | μA    |
|                                                              |                                     |                                                                                 | V <sub>IN</sub> = ±60V<br>(Note 17) | Full         | -3                    | ±0.5  | 3                | mA    |
| Output Leakage Current (Y, Z)<br>(Full Duplex Versions Only) | I <sub>OZD</sub>                    | RE = 0V, DE = 0V,<br>V <sub>CC</sub> = 0V or 5.5V                               | V <sub>IN</sub> = 12V               | Full         | -                     | 20    | 200              | μA    |
|                                                              |                                     |                                                                                 | V <sub>IN</sub> = -7V               | Full         | -100                  | -5    | -                | μA    |
|                                                              |                                     |                                                                                 | V <sub>IN</sub> = ±25V              | Full         | -500                  | ±40   | 500              | μA    |
|                                                              |                                     |                                                                                 | V <sub>IN</sub> = ±60V<br>(Note 17) | Full         | -3                    | ±0.15 | 3                | mA    |
| Receiver Differential<br>Threshold Voltage                   | V <sub>TH</sub>                     | A-B if INV or RINV = 0; B-A if INV or RINV = 1,<br>-25V ≤ V <sub>CM</sub> ≤ 25V |                                     | Full         | -200                  | -100  | -10              | mV    |
| Receiver Input Hysteresis                                    | DV <sub>TH</sub>                    | -25V ≤ V <sub>CM</sub> ≤ 25V                                                    |                                     | 25           | -                     | 25    | -                | mV    |
| Receiver Output High Voltage                                 | V <sub>OH</sub>                     | V <sub>ID</sub> = -10mV                                                         | I <sub>O</sub> = -2mA               | Full         | V <sub>CC</sub> - 0.5 | 4.75  | -                | V     |
|                                                              |                                     |                                                                                 | I <sub>O</sub> = -8mA               | Full         | 2.8                   | 4.2   | -                | V     |
| Receiver Output Low Voltage                                  | V <sub>OL</sub>                     | I <sub>O</sub> = 6mA, V <sub>ID</sub> = -200mV                                  |                                     | Full         | -                     | 0.27  | 0.4              | V     |
| Receiver Output Low Current                                  | I <sub>OL</sub>                     | V <sub>O</sub> = 1V, V <sub>ID</sub> = -200mV                                   |                                     | Full         | 15                    | 22    | -                | mA    |
| Three-State (High Impedance)<br>Receiver Output Current      | I <sub>OZR</sub>                    | 0V ≤ V <sub>O</sub> ≤ V <sub>CC</sub> (Note 16)                                 |                                     | Full         | -1                    | 0.01  | 1                | μA    |
| Receiver Short-Circuit Current                               | I <sub>OSR</sub>                    | 0V ≤ V <sub>O</sub> ≤ V <sub>CC</sub>                                           |                                     | Full         | ±12                   | -     | ±110             | mA    |
| SUPPLY CURRENT                                               |                                     |                                                                                 |                                     |              |                       |       |                  |       |
| No-Load Supply Current<br>(Note 7)                           | I <sub>CC</sub>                     | DE = V <sub>CC</sub> , RE = 0V or V <sub>CC</sub> , DI = 0V or V <sub>CC</sub>  |                                     | Full         | -                     | 2.3   | 4.5              | mA    |
| Shutdown Supply Current                                      | I <sub>SHDN</sub>                   | DE = 0V, RE = V <sub>CC</sub> , DI = 0V or V <sub>CC</sub> (Note 16)            |                                     | Full         | -                     | 10    | 50               | μA    |
| ESD PERFORMANCE                                              |                                     |                                                                                 |                                     |              |                       |       |                  |       |
| RS-485 Pins (A, Y, B, Z, A/Y,<br>B/Z)                        |                                     | Human Body Model,<br>From Bus Pins to<br>GND                                    | 1/2 Duplex                          | 25           | -                     | ±16.5 | -                | kV    |
|                                                              |                                     |                                                                                 | Full Duplex                         | 25           | -                     | ±15   | -                | kV    |
| All Pins                                                     |                                     | Human Body Model, per JEDEC                                                     |                                     | 25           | -                     | ±8    | -                | kV    |
|                                                              |                                     | Machine Model                                                                   |                                     | 25           | -                     | ±700  | -                | V     |
| DRIVER SWITCHING CHARACTERISTICS                             |                                     |                                                                                 |                                     |              |                       |       |                  |       |
| Driver Differential Output<br>Delay                          | t <sub>PLH</sub> , t <sub>PHL</sub> | R <sub>D</sub> = 54Ω, C <sub>D</sub> = 50pF<br>(Figure 4)                       | No CM Load                          | Full         | -                     | 70    | 125              | ns    |
|                                                              |                                     |                                                                                 | -25V ≤ V <sub>CM</sub> ≤ 25V        | Full         | -                     | -     | 350              | ns    |
| Driver Differential Output<br>Skew                           | t <sub>SKEW</sub>                   | R <sub>D</sub> = 54Ω, C <sub>D</sub> = 50pF<br>(Figure 4)                       | No CM Load                          | Full         | -                     | 4.5   | 15               | ns    |
|                                                              |                                     |                                                                                 | -25V ≤ V <sub>CM</sub> ≤ 25V        | Full         | -                     | -     | 25               | ns    |
| Driver Differential Rise or Fall<br>Time                     | t <sub>R</sub> , t <sub>F</sub>     | R <sub>D</sub> = 54Ω, C <sub>D</sub> = 50pF<br>(Figure 4)                       | No CM Load                          | Full         | 70                    | 170   | 300              | ns    |
|                                                              |                                     |                                                                                 | -25V ≤ V <sub>CM</sub> ≤ 25V        | Full         | 70                    | -     | 400              | ns    |
| Maximum Data Rate                                            | f <sub>MAX</sub>                    | C <sub>D</sub> = 820pF (Figure 6)                                               |                                     | Full         | 1                     | 4     | -                | Mbps  |
| Driver Enable to Output High                                 | t <sub>ZH</sub>                     | SW = GND (Figure 5), (Note 9)                                                   |                                     | Full         | -                     | -     | 350              | ns    |
| Driver Enable to Output Low                                  | t <sub>ZL</sub>                     | SW = V <sub>CC</sub> (Figure 5), (Note 9)                                       |                                     | Full         | -                     | -     | 300              | ns    |
| Driver Disable from Output<br>Low                            | t <sub>LZ</sub>                     | SW = V <sub>CC</sub> (Figure 5)                                                 |                                     | Full         | -                     | -     | 120              | ns    |

# ISL32483E, ISL32485E

**Electrical Specifications** Test Conditions:  $V_{CC} = 4.5V$  to  $5.5V$ ; Unless Otherwise Specified. Typical values are at  $V_{CC} = 5V$ ,  $T_A = +25^\circ C$  (Note 6). **Boldface limits apply over the operating temperature range,  $-40^\circ C$  to  $+85^\circ C$ . (Continued)**

| PARAMETER                                    | SYMBOL             | TEST CONDITIONS                                                                   | TEMP<br>( $^\circ C$ ) | MIN<br>(Note 14) | TYP | MAX<br>(Note 14) | UNITS |
|----------------------------------------------|--------------------|-----------------------------------------------------------------------------------|------------------------|------------------|-----|------------------|-------|
| Driver Disable from Output High              | $t_{HZ}$           | SW = GND (Figure 5)                                                               | Full                   | -                | -   | <b>120</b>       | ns    |
| Time to Shutdown                             | $t_{SHDN}$         | (Notes 11, 16)                                                                    | Full                   | <b>60</b>        | 160 | <b>600</b>       | ns    |
| Driver Enable from Shutdown to Output High   | $t_{ZH}(SHDN)$     | SW = GND (Figure 5),<br>(Notes 11, 12, 16)                                        | Full                   | -                | -   | <b>2000</b>      | ns    |
| Driver Enable from Shutdown to Output Low    | $t_{ZL}(SHDN)$     | SW = $V_{CC}$ (Figure 5),<br>(Notes 11, 12, 16)                                   | Full                   | -                | -   | <b>2000</b>      | ns    |
| <b>RECEIVER SWITCHING CHARACTERISTICS</b>    |                    |                                                                                   |                        |                  |     |                  |       |
| Maximum Data Rate                            | $f_{MAX}$          | $-25V \leq V_{CM} \leq 25V$ (Figure 7)                                            | Full                   | <b>1</b>         | 15  | -                | Mbps  |
| Receiver Input to Output Delay               | $t_{PLH}, t_{PHL}$ | $-25V \leq V_{CM} \leq 25V$ (Figure 7)                                            | Full                   | -                | 90  | <b>150</b>       | ns    |
| Receiver Skew   $t_{PLH} - t_{PHL}$          | $t_{SKD}$          | (Figure 7)                                                                        | Full                   | -                | 4   | <b>10</b>        | ns    |
| Receiver Enable to Output Low                | $t_{ZL}$           | $R_L = 1k\Omega$ , $C_L = 15pF$ , SW = $V_{CC}$ (Figure 8),<br>(Notes 10, 16)     | Full                   | -                | -   | <b>50</b>        | ns    |
| Receiver Enable to Output High               | $t_{ZH}$           | $R_L = 1k\Omega$ , $C_L = 15pF$ , SW = GND (Figure 8),<br>(Notes 10, 16)          | Full                   | -                | -   | <b>50</b>        | ns    |
| Receiver Disable from Output Low             | $t_{LZ}$           | $R_L = 1k\Omega$ , $C_L = 15pF$ , SW = $V_{CC}$ (Figure 8)<br>(Note 16)           | Full                   | -                | -   | <b>50</b>        | ns    |
| Receiver Disable from Output High            | $t_{HZ}$           | $R_L = 1k\Omega$ , $C_L = 15pF$ , SW = GND (Figure 8)<br>(Note 16)                | Full                   | -                | -   | <b>50</b>        | ns    |
| Time to Shutdown                             | $t_{SHDN}$         | (Notes 11, 16)                                                                    | Full                   | <b>60</b>        | 160 | <b>600</b>       | ns    |
| Receiver Enable from Shutdown to Output High | $t_{ZH}(SHDN)$     | $R_L = 1k\Omega$ , $C_L = 15pF$ , SW = GND (Figure 8),<br>(Notes 11, 13, 16)      | Full                   | -                | -   | <b>2000</b>      | ns    |
| Receiver Enable from Shutdown to Output Low  | $t_{ZL}(SHDN)$     | $R_L = 1k\Omega$ , $C_L = 15pF$ , SW = $V_{CC}$ (Figure 8),<br>(Notes 11, 13, 16) | Full                   | -                | -   | <b>2000</b>      | ns    |

**NOTES:**

- All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
- Supply current specification is valid for loaded drivers when  $DE = 0V$ .
- Applies to peak current. See "Typical Performance Curves" beginning on page 18 for more information
- Keep  $\overline{RE} = 0$  to prevent the device from entering SHDN.
- The  $\overline{RE}$  signal high time must be short enough (typically  $<100ns$ ) to prevent the device from entering SHDN.
- Transceivers (except on the ISL32485E) are put into shutdown by bringing  $\overline{RE}$  high and  $DE$  low. If the inputs are in this state for less than 60ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 600ns, the parts are guaranteed to have entered shutdown. See "Low Power Shutdown Mode" on page 12.
- Keep  $\overline{RE} = V_{CC}$ , and set the  $DE$  signal low time  $>600ns$  to ensure that the device enters SHDN.
- Set the  $\overline{RE}$  signal high time  $>600ns$  to ensure that the device enters SHDN.
- Compliance to data sheet limits is assured by one or more methods: production test, characterization and/or design.
- Tested according to TIA/EIA-485-A, Section 4.2.6 ( $\pm 80V$  for 15ms at a 1% duty cycle).
- Does not apply to the ISL32485E. The ISL32485E has no Rx enable function, and thus no SHDN function.
- See "Caution" statement in the "Recommended Operating Conditions" section on page 5.

## Test Circuits and Waveforms

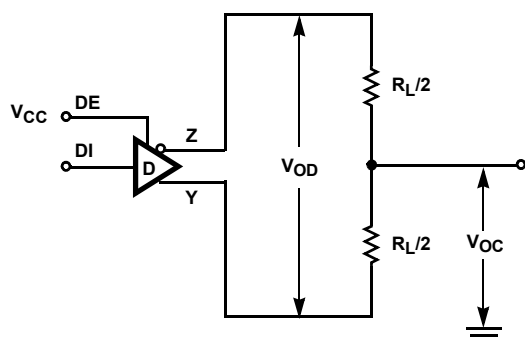


FIGURE 3A.  $V_{OD}$  AND  $V_{OC}$

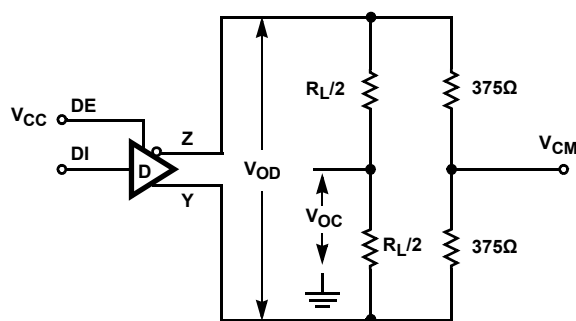


FIGURE 3B.  $V_{OD}$  AND  $V_{OC}$  WITH COMMON MODE LOAD

FIGURE 3. DC DRIVER TEST CIRCUITS

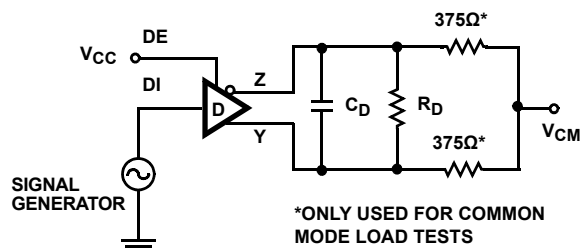


FIGURE 4A. TEST CIRCUIT

FIGURE 4. DRIVER PROPAGATION DELAY AND DIFFERENTIAL TRANSITION TIMES

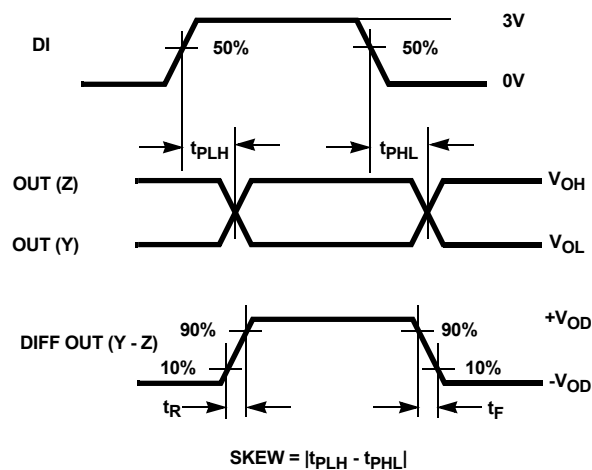


FIGURE 4B. MEASUREMENT POINTS

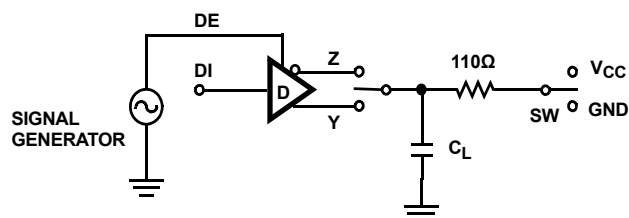


FIGURE 5A. TEST CIRCUIT

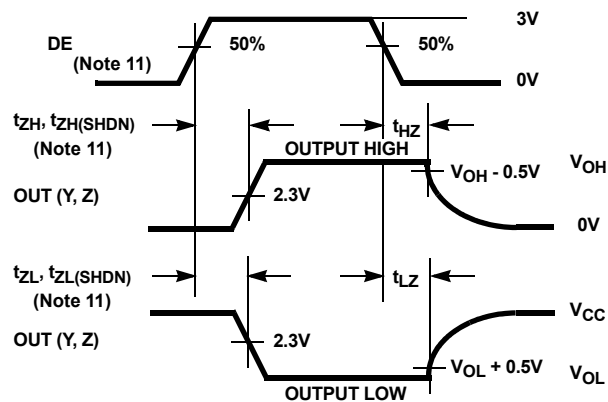


FIGURE 5B. MEASUREMENT POINTS

FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

| PARAMETER      | OUTPUT | $\overline{RE}$ | DI  | SW       | $C_L$ (pF) |
|----------------|--------|-----------------|-----|----------|------------|
| $t_{HZ}$       | Y/Z    | X               | 1/0 | GND      | 50         |
| $t_{LZ}$       | Y/Z    | X               | 0/1 | $V_{CC}$ | 50         |
| $t_{ZH}$       | Y/Z    | 0 (Note 9)      | 1/0 | GND      | 100        |
| $t_{ZL}$       | Y/Z    | 0 (Note 9)      | 0/1 | $V_{CC}$ | 100        |
| $t_{ZH(SHDN)}$ | Y/Z    | 1 (Note 12)     | 1/0 | GND      | 100        |
| $t_{ZL(SHDN)}$ | Y/Z    | 1 (Note 12)     | 0/1 | $V_{CC}$ | 100        |

## Test Circuits and Waveforms (Continued)

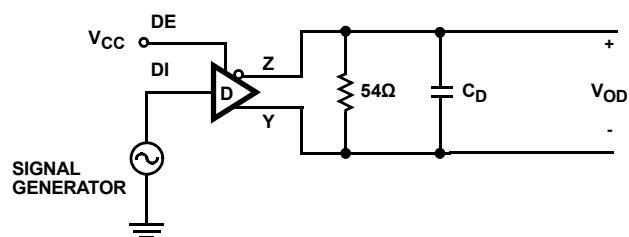


FIGURE 6A. TEST CIRCUIT

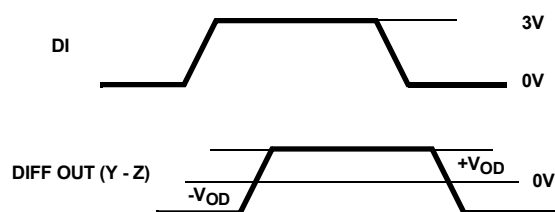


FIGURE 6B. MEASUREMENT POINTS

FIGURE 6. DRIVER DATA RATE

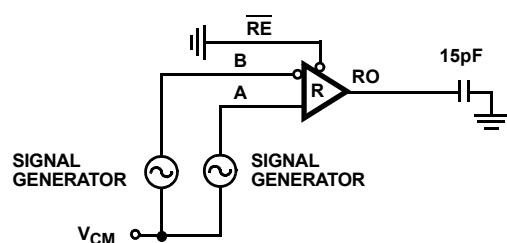


FIGURE 7A. TEST CIRCUIT

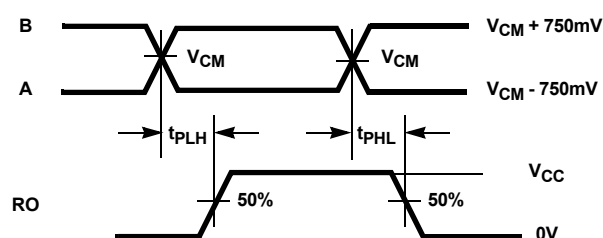
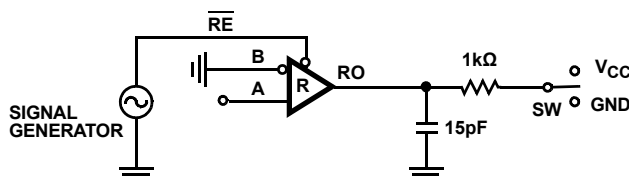


FIGURE 7B. MEASUREMENT POINTS

FIGURE 7. RECEIVER PROPAGATION DELAY AND DATA RATE



| PARAMETER                | DE | A     | SW       |
|--------------------------|----|-------|----------|
| $t_{HZ}$                 | 0  | +1.5V | GND      |
| $t_{LZ}$                 | 0  | -1.5V | $V_{CC}$ |
| $t_{ZH}$ (Note 10)       | 0  | +1.5V | GND      |
| $t_{ZL}$ (Note 10)       | 0  | -1.5V | $V_{CC}$ |
| $t_{ZH}(SHDN)$ (Note 13) | 0  | +1.5V | GND      |
| $t_{ZL}(SHDN)$ (Note 13) | 0  | -1.5V | $V_{CC}$ |

FIGURE 8A. TEST CIRCUIT

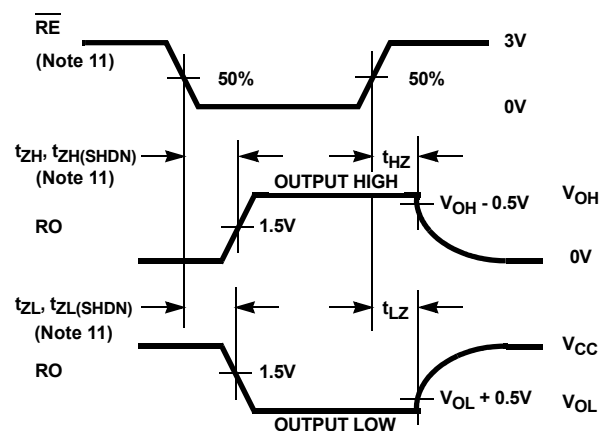


FIGURE 8B. MEASUREMENT POINTS

FIGURE 8. RECEIVER ENABLE AND DISABLE TIMES

## Application Information

RS-485 and RS-422 are differential (balanced) data transmission standards used for long haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a point-to-multipoint (multidrop) standard, which allows only one driver and up to 10 (assuming one-unit load devices) receivers on each bus. RS-485 is a true multipoint standard, which allows up to 32 one-unit load devices (any combination of drivers and receivers) on each bus. To allow for multipoint operation, the RS-485 specification requires that drivers must handle bus contention without sustaining any damage.

Another important advantage of RS-485 is the extended common mode range (CMR), which specifies that the driver outputs and receiver inputs withstand signals that range from +12V to -7V. RS-422 and RS-485 are intended for runs as long as 4000 feet, so the wide CMR is necessary to handle ground potential differences, as well as voltages induced in the cable by external fields.

The ISL3248xE is a family of ruggedized RS-485 transceivers that improves on the RS-485 basic requirements and therefore increases system reliability. The CMR increases to  $\pm 25\text{V}$ , while the RS-485 bus pins (receiver inputs and driver outputs) include fault protection against voltages and transients up to  $\pm 60\text{V}$ . Additionally, larger-than-required differential output voltages ( $V_{OD}$ ) increase noise immunity, while the  $\pm 16.5\text{kV}$  built-in ESD protection complements the fault protection.

## Receiver (Rx) Features

These devices utilize a differential input receiver for maximum noise immunity and common mode rejection. Input sensitivity is better than  $\pm 200\text{mV}$ , as required by the RS-422 and RS-485 specifications.

Receiver input (load) current surpasses the RS-422 specification of 3mA and is four times lower than the RS-485 "Unit Load (UL)" requirement of 1mA maximum. Thus, these products are known as "one-quarter UL" transceivers, and there can be up to 128 of these devices on a network while still complying with the RS-485 loading specification.

The Rx functions with common mode voltages as great as  $\pm 25\text{V}$ , making them ideal for industrial or long networks where induced voltages are a realistic concern.

All the receivers include a "full fail-safe" function that guarantees a high-level receiver output if the receiver inputs are unconnected (floating), shorted together, or connected to a terminated bus with all the transmitters disabled (i.e., an idle bus).

Rx outputs feature high drive levels (typically  $22\text{mA}$  @  $V_{OL} = 1\text{V}$ ) to ease the design of optically coupled isolated interfaces. Except for the ISL32485E, Rx outputs are three-statable via the active low  $\overline{\text{RE}}$  input.

The Rx includes noise filtering circuitry to reject high-frequency signals, and typically rejects pulses narrower than 50ns (equivalent to 20Mbps).

## Driver (Tx) Features

The RS-485/RS-422 driver is a differential output device that delivers at least 1.5V across a  $54\Omega$  load (RS-485) and at least 2.4V across a  $100\Omega$  load (RS-422). The drivers feature low propagation delay skew to maximize bit width and to minimize EMI, and all drivers are three-statable via the active high DE input.

The driver outputs are slew rate limited to minimize EMI and to minimize reflections in unterminated or improperly terminated networks.

## High Overvoltage (Fault) Protection Increases Ruggedness

The  $\pm 60\text{V}$  (referenced to the IC GND) fault protection on the RS-485 pins makes these transceivers some of the most rugged on the market. This level of protection makes the ISL3248xE perfect for applications where power (e.g., 24V and 48V supplies) must be routed in the conduit with the data lines, or for outdoor applications where large transients are likely to occur. When power is routed with the data lines, even a momentary short between the supply and data lines will destroy an unprotected device. The  $\pm 60\text{V}$  fault levels of this family are at least *five times higher* than the levels specified for standard RS-485 ICs. The ISL3248xE protection is active whether the Tx is enabled or disabled, and even if the IC is powered down.

If transients or voltages (including overshoots and ringing) greater than  $\pm 60\text{V}$  are possible, then additional external protection is required.

## Widest Common Mode Voltage (CMV) Tolerance Improves Operating Range

RS-485 networks operating in industrial complexes or over long distances are susceptible to large CMV variations. Either of these operating environments may suffer from large node-to-node ground potential differences or CMV pickup from external electromagnetic sources, and devices with only the minimum required +12V to -7V CMR may malfunction. The ISL3248xE's extended  $\pm 25\text{V}$  CMR is the widest available, allowing operation in environments that would overwhelm lesser transceivers. Additionally, the Rx will not phase invert (erroneously change state), even with CMVs of  $\pm 40\text{V}$  or differential voltages as large as 40V.

## Cable Invert (Polarity Reversal) Function

With large node count RS-485 networks, it is common for some cable data lines to be wired backwards during installation. When this happens, the node is unable to communicate over the network. Once a technician finds the miswired node, he must then rewire the connector, which is time consuming.

The ISL32483E and ISL32485E simplify this task by including cable invert pins (INV, DINV, RINV) that allow the technician to invert the polarity of the Rx input and/or the Tx output pins simply by moving a jumper to change the state of the invert pins. When the invert pin is low, the IC operates like any standard RS-485 transceiver, and the bus pins have their normal polarity definition of A and Y being noninverting and B and Z being inverting. With the invert pin high, the corresponding bus pins reverse their polarity, so B and Z are now noninverting, and A and Y become inverting.

Intersil's unique cable invert function is superior to that found on competing devices, because the Rx full fail-safe function is maintained, even when the Rx polarity is reversed. Competitor devices implement the Rx invert function simply by inverting the Rx output. This means that with the Rx inputs floating or shorted together, the Rx appropriately delivers a logic 1 in normal polarity, but outputs a logic low when the IC is operated in the inverted mode. Intersil's innovative Rx design guarantees that, with the Rx inputs floating or shorted together ( $V_{ID}=0V$ ), the Rx output remains high, regardless of the state of the invert pins.

The full duplex ISL32483E includes two invert pins that allow for separate control of the Rx and Tx polarities. If only the Rx cable is miswired, then only the RINV pin need be driven to a logic 1. If the Tx cable is miswired, then DINV must be connected to a logic high. The half-duplex version has only one logic pin (INV) that, when high, switches the polarity of both the Tx and the Rx blocks.

## High $V_{OD}$ Improves Noise Immunity and Flexibility

The ISL3248xE driver design delivers larger differential output voltages ( $V_{OD}$ ) than the RS-485 standard requires or than most RS-485 transmitters can deliver. The typical  $\pm 2.5V$   $V_{OD}$  provides more noise immunity than networks built using many other transceivers.

Another advantage of the large  $V_{OD}$  is the ability to drive more than two bus terminations, which allows for utilizing the ISL3248xE in "star" and other multi-terminated, nonstandard network topologies.

Figure 10 details the transmitter's  $V_{OD}$  versus  $I_{OUT}$  characteristic, and includes load lines for four ( $30\Omega$ ) and six ( $20\Omega$ )  $120\Omega$  terminations. The figure shows that the driver typically delivers  $\pm 1.3V$  into six terminations, and the "Electrical Specifications" on page 5 guarantee a  $V_{OD}$  of  $\pm 0.8V$  at  $21\Omega$  over the full temperature range. The RS-485 standard requires a minimum  $1.5V$   $V_{OD}$  into two terminations, but the ISL3248xE delivers RS-485 voltage levels with 2x to 3x the number of terminations.

## Hot Plug Function

When a piece of equipment powers up, there is a period of time in which the processor or ASIC driving the RS-485 control lines (DE,  $\overline{RE}$ ) is unable to ensure that the RS-485 Tx and Rx outputs are kept disabled. If the equipment is connected to a bus, a driver activating prematurely during power-up may crash the bus. To avoid this scenario, the ISL3248xE devices incorporate a "Hot Plug" function. Circuitry monitoring  $V_{CC}$  ensures that, during power-up and power-down, the Tx and Rx outputs remain disabled, regardless of the state of DE and  $\overline{RE}$ , if  $V_{CC}$  is less than  $\approx 3.5V$ . This gives the processor or ASIC a chance to stabilize and drive the RS-485 control lines to the proper states. Figure 9 illustrates the power-up and power-down performance of the ISL3248xE compared to an RS-485 IC without the Hot Plug feature.

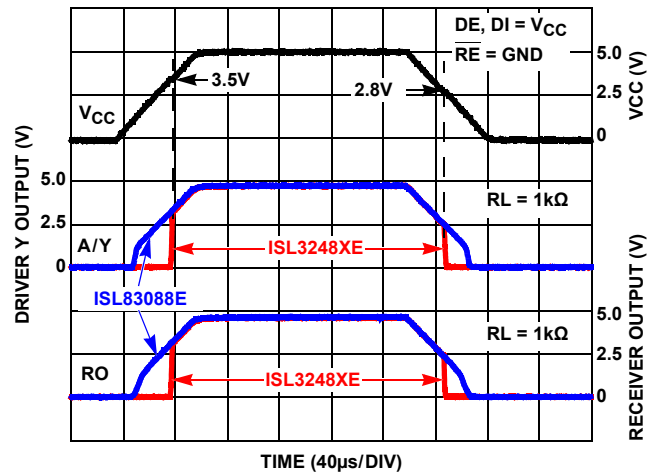


FIGURE 9. HOT PLUG PERFORMANCE (ISL3248xE) vs ISL83088E WITHOUT HOT PLUG CIRCUITRY

## ESD Protection

All pins on the ISL3248xE devices include Class 3 ( $>8kV$ ) Human Body Model (HBM) ESD protection structures that are good enough to survive ESD events commonly seen during manufacturing. Even so, the RS-485 pins (driver outputs and receiver inputs) incorporate more advanced structures that allow them to survive ESD events in excess of  $\pm 16.5kV$  HBM ( $\pm 15kV$  for full-duplex version). The RS-485 pins are particularly vulnerable to ESD strikes, because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins or connecting a cable can cause an ESD event that might destroy unprotected ICs. The new ESD structures protect the device whether or not it is powered up, and without interfering with the exceptional  $\pm 25V$  CMR. This built-in ESD protection minimizes the need for board-level protection structures (e.g., transient suppression diodes) and the associated, undesirable capacitive load they present.

## Data Rate, Cables, and Terminations

RS-485/RS-422 are intended for network lengths up to 4000 feet, but the maximum system data rate decreases as the transmission length increases. These 1Mbps versions can operate at full data rates with lengths up to 800 feet (244m). Jitter is the limiting parameter at this data rate, so employing encoded data streams (e.g., Manchester coded or Return-to-Zero) may allow increased transmission distances.

Twisted pair is the cable of choice for RS-485/RS-422 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common mode signals, which are effectively rejected by the differential receivers in these ICs.

Proper termination is imperative to minimize reflections, and terminations are recommended unless power dissipation is an overriding concern. In point-to-point, or point-to-multipoint (single driver on bus like RS-422) networks, the main cable should be terminated in its characteristic impedance (typically 120Ω) at the end farthest from the driver. In multi-receiver applications, stubs connecting receivers to the main cable should be kept as short as possible. Multipoint (multi-driver) systems require that the main cable be terminated in its characteristic impedance at both ends. Stubs connecting a transceiver to the main cable should be kept as short as possible.

## Built-In Driver Overload Protection

As stated previously, the RS-485 specification requires that drivers survive worst-case bus contentions undamaged. These transceivers meet this requirement via driver output short circuit current limits and on-chip thermal shutdown circuitry.

The driver output stages incorporate a double foldback, short circuit current limiting scheme, which ensures that the output current never exceeds the RS-485 specification, even at the common mode and fault condition voltage range extremes. The first foldback current level ( $\approx 70\text{mA}$ ) is set to ensure that the driver never folds back when driving loads with common mode voltages up to  $\pm 25\text{V}$ . The very low second foldback current

setting ( $\approx 9\text{mA}$ ) minimizes power dissipation if the Tx is enabled when a fault occurs.

In the event of a major short circuit condition, devices also include a thermal shutdown feature that disables the drivers whenever the die temperature becomes excessive. This eliminates the power dissipation, allowing the die to cool. The drivers automatically re-enable after the die temperature drops about  $15^\circ\text{C}$ . If the contention persists, the thermal shutdown/re-enable cycle repeats until the fault is cleared. Receivers stay operational during thermal shutdown.

## Low Power Shutdown Mode

These BiCMOS transceivers all use a fraction of the power required by competitive devices, but they also include a shutdown feature (except the ISL32485E) that reduces the already low quiescent  $I_{CC}$  to a  $10\mu\text{A}$  trickle. These devices enter shutdown whenever the receiver and driver are *simultaneously* disabled ( $\overline{RE} = V_{CC}$  and  $DE = \text{GND}$ ) for a period of at least 600ns. Disabling both the driver and the receiver for less than 60ns guarantees that the transceiver will not enter shutdown.

Note that receiver and driver enable times increase when the transceiver enables from shutdown. Refer to Notes 9, 10, 11, 12 and 13, at the end of "Electrical Specifications" on page 5, for more information.

## Typical Performance Curves $V_{CC} = 5\text{V}$ , $T_A = +25^\circ\text{C}$ ; Unless Otherwise Specified.

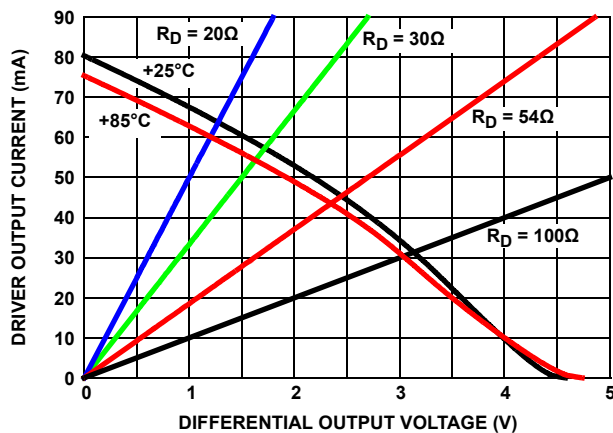


FIGURE 10. DRIVER OUTPUT CURRENT vs DIFFERENTIAL OUTPUT VOLTAGE

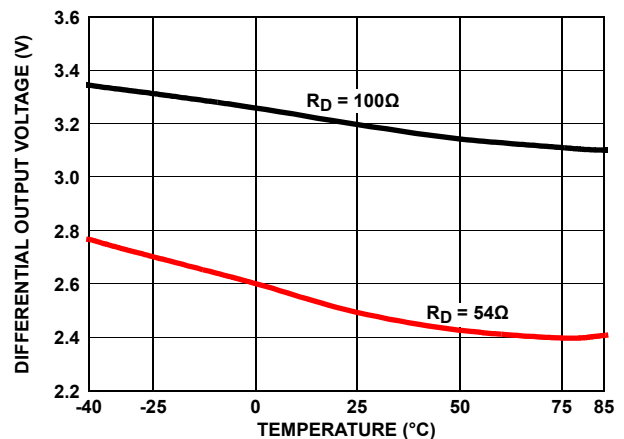


FIGURE 11. DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs TEMPERATURE

## Typical Performance Curves $V_{CC} = 5V$ , $T_A = +25^\circ C$ ; Unless Otherwise Specified. (Continued)

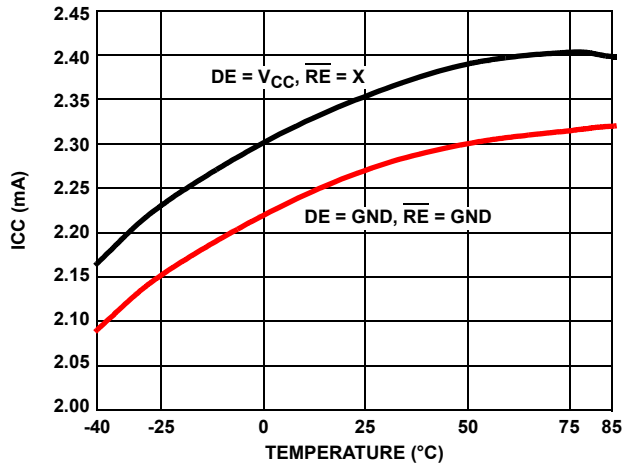


FIGURE 12. SUPPLY CURRENT vs TEMPERATURE

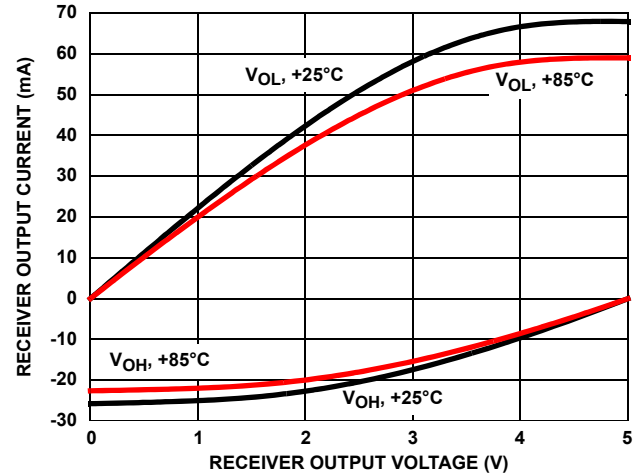


FIGURE 13. RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

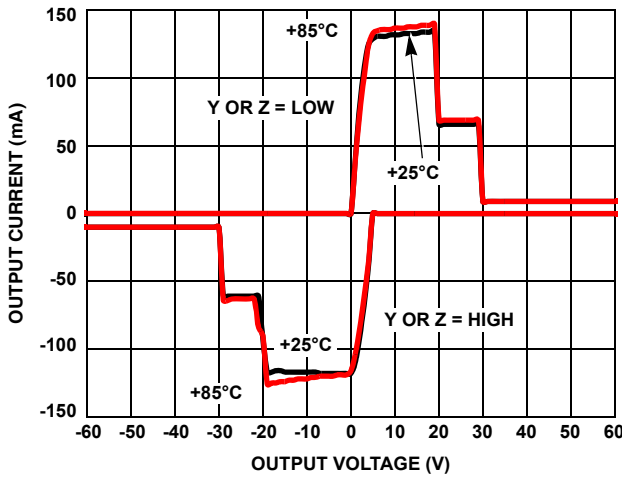


FIGURE 14. DRIVER OUTPUT CURRENT vs SHORT CIRCUIT VOLTAGE

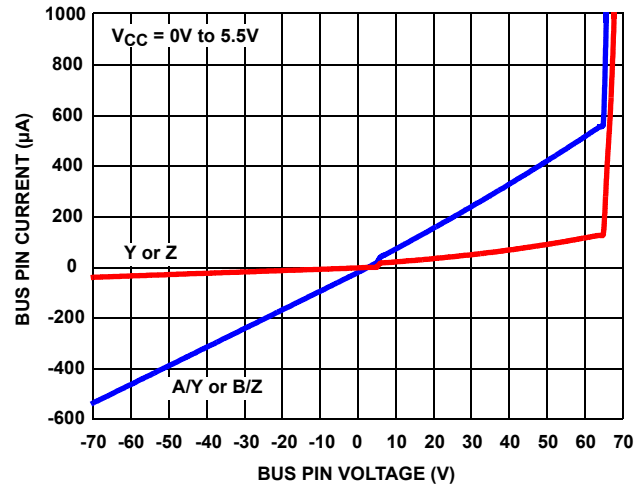


FIGURE 15. BUS PIN CURRENT vs BUS PIN VOLTAGE

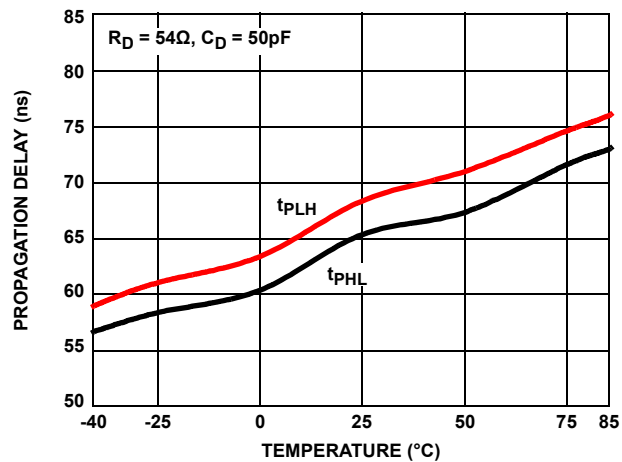


FIGURE 16. DRIVER DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE

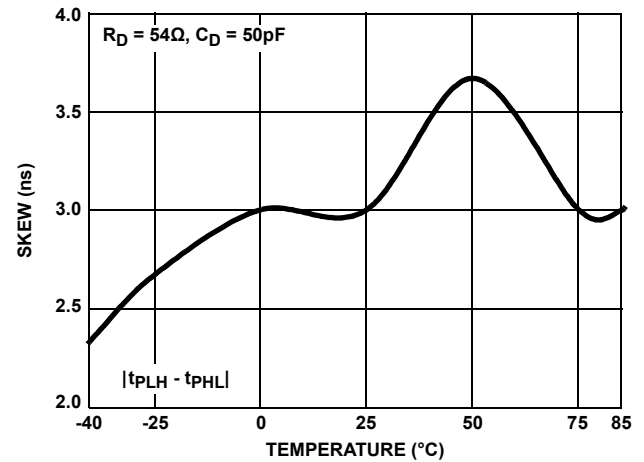


FIGURE 17. DRIVER DIFFERENTIAL SKEW vs TEMPERATURE

## Typical Performance Curves $V_{CC} = 5V$ , $T_A = +25^\circ C$ ; Unless Otherwise Specified. (Continued)

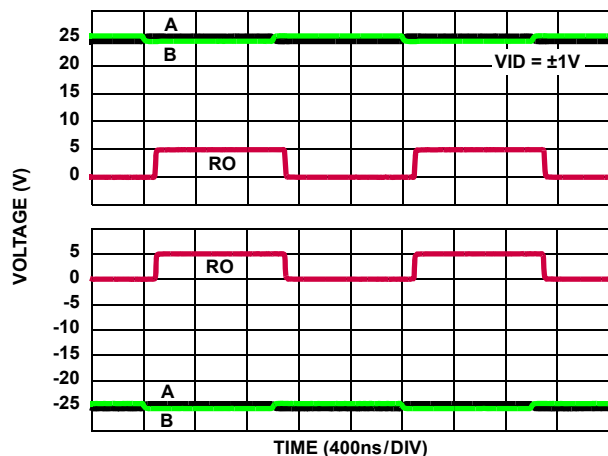


FIGURE 18. RECEIVER PERFORMANCE WITH  $\pm 25V$  CMV

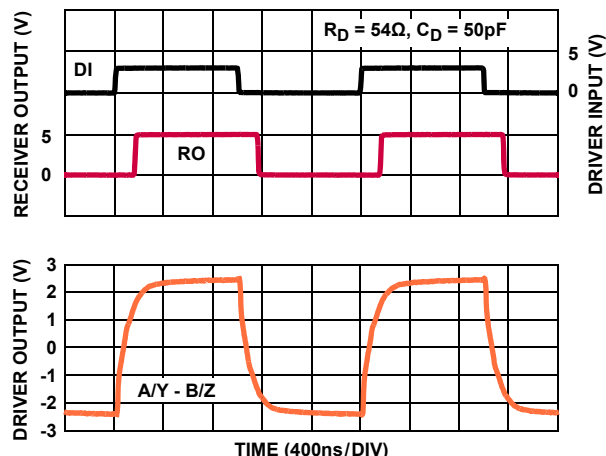


FIGURE 19. DRIVER AND RECEIVER WAVEFORMS

## Die Characteristics

### SUBSTRATE POTENTIAL (Powered Up):

GND

### PROCESS:

Si Gate BiCMOS

# ISL32483E, ISL32485E

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

| DATE             | REVISION | CHANGE                                                                                                                                                     |
|------------------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| March 8, 2012    | FN7785.1 | Page 5 - Thermal Resistance - 8 Ld SOIC package Theta JA changed from 116 to 108<br>Page 13 - Updated Figure 15 to show Pos breakdown between 60V and 70V. |
| January 18, 2011 | FN7785.0 | Initial Release                                                                                                                                            |

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\*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: [ISL32483E, ISL32485E](http://www.intersil.com/products)

To report errors or suggestions for this data sheet, please go to [www.intersil.com/ask our staff](http://www.intersil.com/ask_our_staff)

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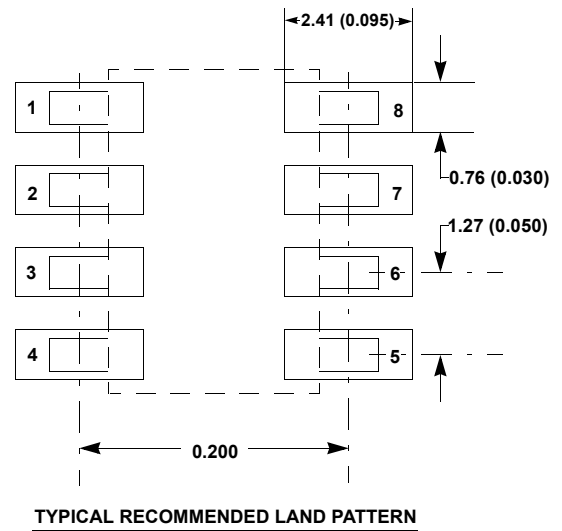
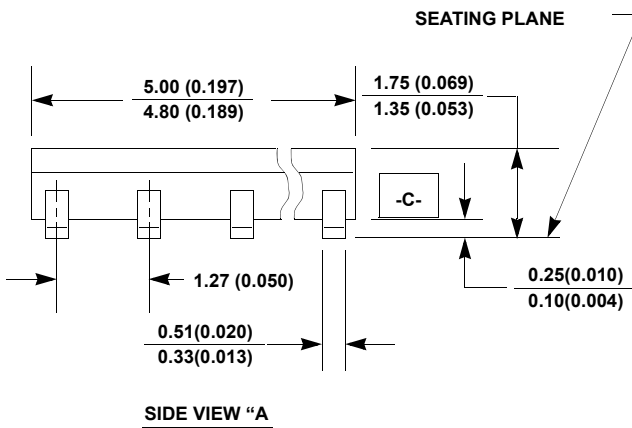
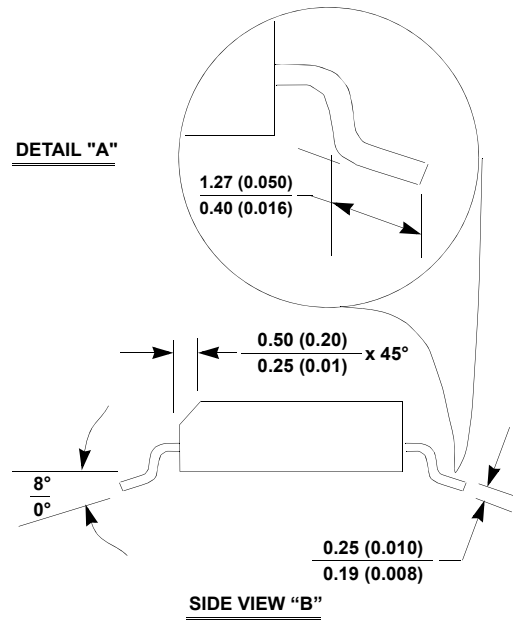
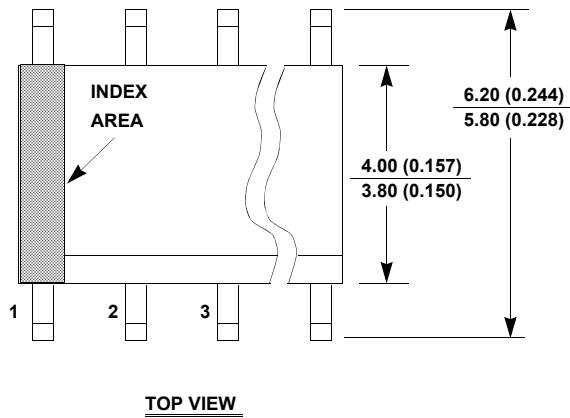


## Package Outline Drawing

### M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

Rev 2, 11/10



#### NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.