

## Advanced Lighting Management Unit

Check for Samples: [LP3954](#)

### FEATURES

- Audio Synchronization for Color/RGB LEDs
- Command Based PWM Controlled RGB LED Drivers
- High Current Driver for Flash LED With Built-in Timing
- 4+2 or 6 Low Voltage Constant Current White LED Drivers With Orogrammable 8-Bit Adjustment (0...25mA/LED)
- High Efficiency Boost DC-DC Converter
- SPI / I<sup>2</sup>C Compatible Interface
- Possibility for External PWM Dimming Control
- Possibility for Clock Synchronization for RGB Timing
- Ambient Light and Temperature Sensing Possibility
- Small Package – DSBGA, 3.0 x 3.0 x 0.6mm

### DESCRIPTION

LP3954 is an advanced lighting management unit for handheld devices. It drives any phone lights including display backlights, RGB, keypad and camera flash LEDs. The boost DC-DC converter drives high current loads with high efficiency. White LED backlight drivers are high efficiency low voltage structures with excellent matching and automatic fade in/ fade out function. The new stand-alone command based RGB controller is feature rich and easy to configure. Built-in audio synchronization feature allows user to synchronize the color LEDs to audio input. Integrated high current driver can drive camera flash LED or motor/vibra. Internal ADC can be used for ambient light or temperature sensing. The flexible SPI/I<sup>2</sup>C interface allows easy control of LP3954. Small DSBGA package together with minimum number of external components is a best fit for handheld devices.

### APPLICATIONS

- Cellular Phones
- PDAs, MP3 players



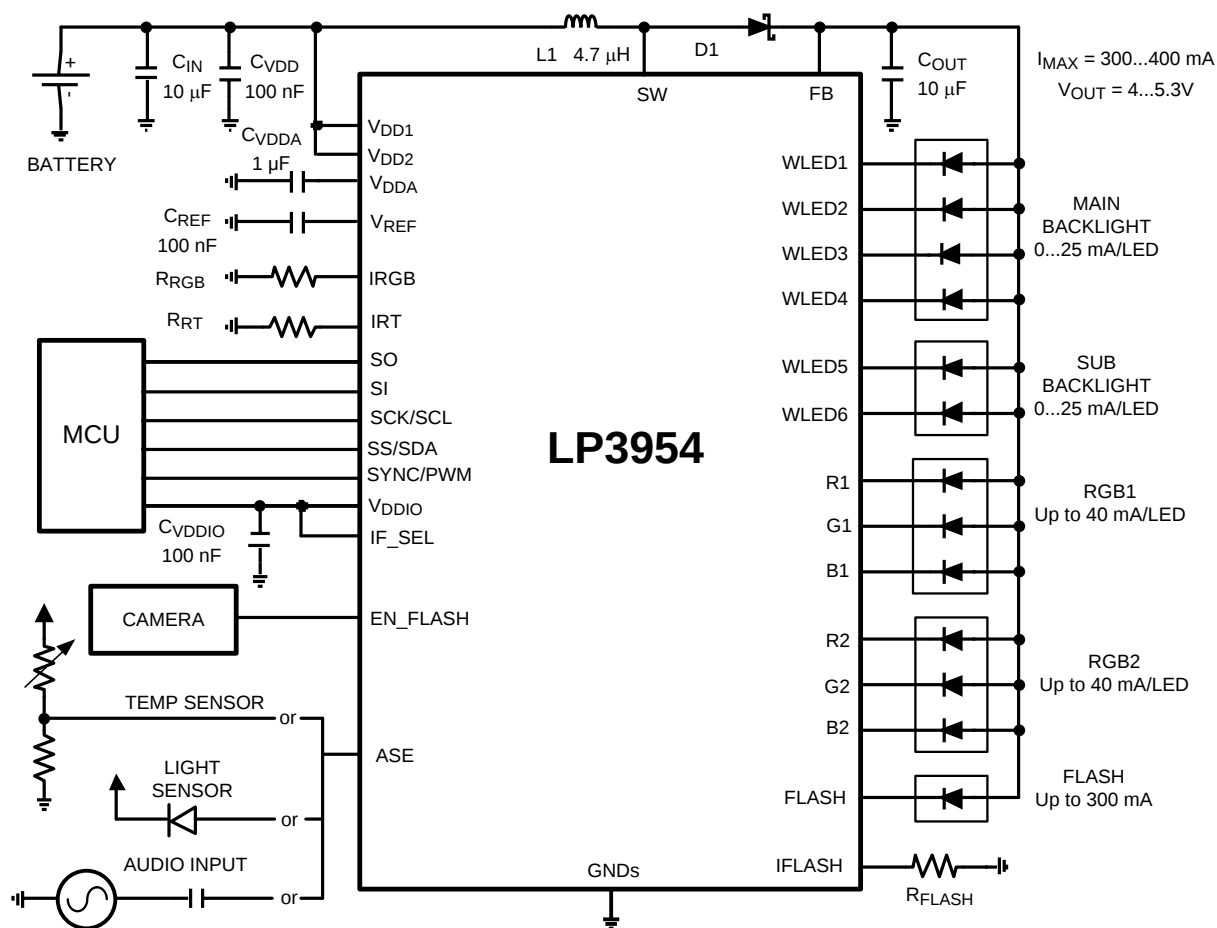
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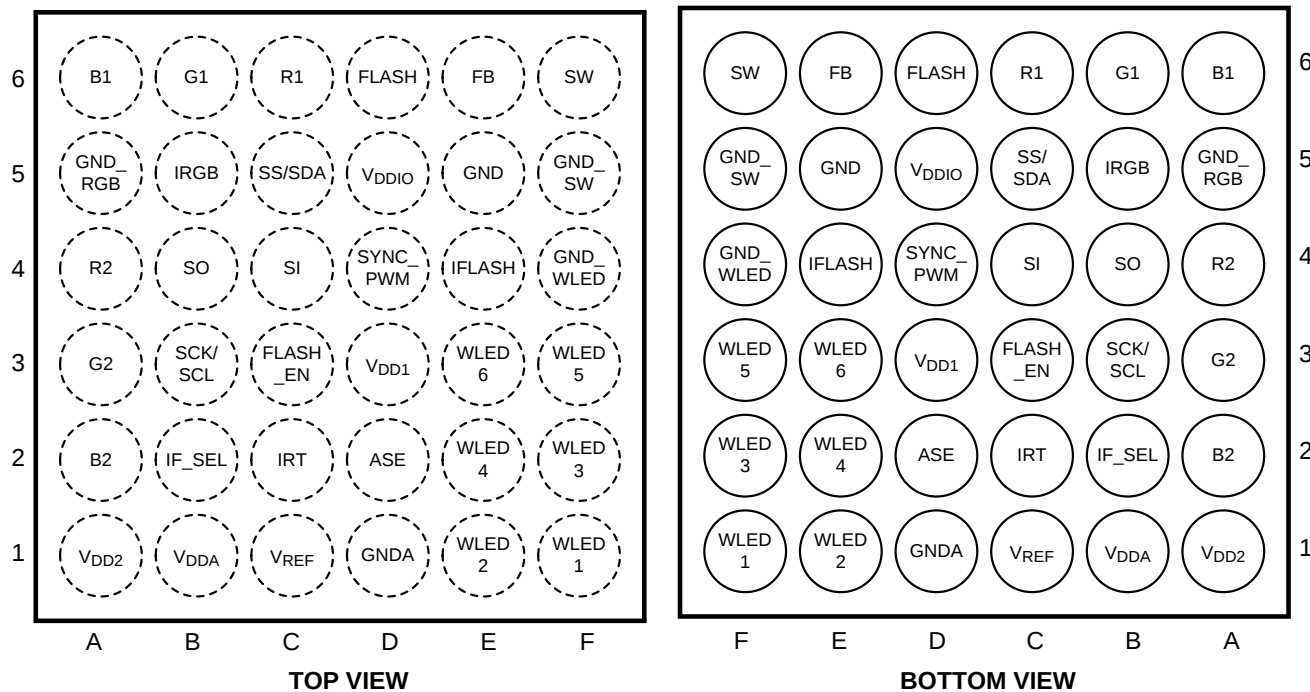
## Typical Application



## Connection Diagrams

**DSBGA Package, 3.0 x 3.0 x 0.6mm, 0.5mm pitch Package Number YZR0036AAA or**

**DSBGA Package, 3.0 x 3.0 x 0.65mm, 0.5mm pitch Package Number YPG0036AAA**



**Table 1. Pin Descriptions**

| Pin No. | Name     | Type               | Description                                                                   |
|---------|----------|--------------------|-------------------------------------------------------------------------------|
| 6F      | SW       | Output             | Boost Converter Power Switch                                                  |
| 6E      | FB       | Input              | Boost Converter Feedback                                                      |
| 6D      | FLASH    | Output             | High Current Flash Output                                                     |
| 6C      | R1       | Output             | Red LED 1 Output                                                              |
| 6B      | G1       | Output             | Green LED 1 Output                                                            |
| 6A      | B1       | Output             | Blue LED 1 Output                                                             |
| 5F      | GND_SW   | Ground             | Power Switch Ground                                                           |
| 5E      | GND      | Ground             | Ground                                                                        |
| 5D      | VDDIO    | Power              | Supply Voltage for Input/output Buffers and Drivers                           |
| 5C      | SS/SDA   | Logic Input/Output | Slave Select (SPI), Serial Data In/Out (I <sup>2</sup> C)                     |
| 5B      | IRGB     | Input              | Bias Current Set Resistor for RGB Drivers                                     |
| 5A      | GND_RGB  | Ground             | Ground for RGB Currents                                                       |
| 4F      | GND_WLED | Ground             | Ground for WLED Currents                                                      |
| 4E      | IFLASH   | Input              | High Current Flash Current Set Resistor                                       |
| 4D      | SYNC_PWM | Logic Input        | External PWM Control for LEDs or External Clock for RGB Sync                  |
| 4C      | SI       | Logic Input        | Serial Input (SPI), Address Select (I <sup>2</sup> C)                         |
| 4B      | SO       | Logic Output       | Serial Data Out (SPI)                                                         |
| 4A      | R2       | Output             | Red LED 2 output                                                              |
| 3F      | WLED5    | Output             | White LED 5 output                                                            |
| 3E      | WLED6    | Output             | White LED 6 output                                                            |
| 3D      | VDD1     | Power              | Supply voltage                                                                |
| 3C      | EN_FLASH | Logic Input        | Enable for High Current Flash                                                 |
| 3B      | SCK/SCL  | Logic Input        | Clock (SPI/I <sup>2</sup> C)                                                  |
| 3A      | G2       | Output             | Green LED 2 Output                                                            |
| 2F      | WLED3    | Output             | White LED 3 output                                                            |
| 2E      | WLED4    | Output             | White LED 4 output                                                            |
| 2D      | ASE      | Input              | Audio Synchronization Input                                                   |
| 2C      | IRT      | Input              | Oscillator Frequency Resistor                                                 |
| 2B      | IF_SEL   | Logic Input        | Interface (SPI or I <sup>2</sup> C compatible) Selection (IF_SEL = 1 for SPI) |
| 2A      | B2       | Output             | Blue LED 2 Output                                                             |
| 1F      | WLED1    | Output             | White LED 1 Output                                                            |
| 1E      | WLED2    | Output             | White LED 2 Output                                                            |
| 1D      | GNDA     | Ground             | Ground for Analog Circuitry                                                   |
| 1C      | VREF     | Output             | Reference Voltage                                                             |
| 1B      | VDDA     | Power              | Internal LDO Output                                                           |
| 1A      | VDD2     | Power              | Supply Voltage                                                                |



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings<sup>(1) (2)(3)</sup>

|                                                                             |                                                 |
|-----------------------------------------------------------------------------|-------------------------------------------------|
| V (SW, FB, R1-2, G1-2, B1-2, FLASH, WLED1-6) <sup>(4) (5)</sup>             | -0.3V to +7.2V                                  |
| V <sub>DD1</sub> , V <sub>DD2</sub> , V <sub>DD_IO</sub> , V <sub>DDA</sub> | -0.3V to +6.0V                                  |
| Voltage on ASE, IRT, IFLASH, IRGB, VREF                                     | -0.3V to V <sub>DD1</sub> +0.3V with 6.0V max   |
| Voltage on Logic Pins                                                       | -0.3V to V <sub>DD_IO</sub> +0.3V with 6.0V max |
| V(all other pins): Voltage to GND                                           | -0.3V to 6.0V                                   |
| I (V <sub>REF</sub> )                                                       | 10μA                                            |
| I(R1, G1, B1, R2, G2, B2)                                                   | 100mA                                           |
| I(FLASH) <sup>(6)</sup>                                                     | 400mA                                           |
| Continuous Power Dissipation <sup>(7)</sup>                                 | Internally Limited                              |
| Junction Temperature (T <sub>J-MAX</sub> )                                  | 150°C                                           |
| Storage Temperature Range                                                   | -65°C to +150°C                                 |
| Maximum Lead Temperature (Soldering) <sup>(8)</sup>                         | 260°C                                           |
| ESD Rating, Human Body Model <sup>(9)</sup>                                 | 2kV                                             |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
- (2) All voltages are with respect to the potential at the GND pins.
- (3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (4) Battery/Charger voltage should be above 6V no more than 10% of the operational lifetime.
- (5) Voltage tolerance of LP3954 above 6.0V relies on fact that V<sub>DD1</sub> and V<sub>DD2</sub> (2.8V) are available (ON) at all conditions. If V<sub>DD1</sub> and V<sub>DD2</sub> are not available (ON) at all conditions, TI does not ensure any parameters or reliability for this device.
- (6) The total load current of the boost converter in worst-case conditions should be limited to 300mA (min. input and max. output voltage).
- (7) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T<sub>J</sub>=160°C (typ.) and disengages at T<sub>J</sub>=140°C (typ.).
- (8) For detailed soldering specifications and information, please refer to Application Note AN1112 : Micro SMD Wafer Level Chip Scale Package [SNVA009](#) or Application Note AN1412 : Micro SMDxt Wafer Level Chip Scale Package [SNVA131](#).
- (9) The Human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin. MIL-STD-883 3015.7

## Operating Ratings<sup>(1) (2)</sup>

|                                                            |                                |
|------------------------------------------------------------|--------------------------------|
| V (SW, FB, WLED1-6, R1-2, G1-2, B1-2, FLASH)               | 0 to 6.0V                      |
| V <sub>DD1,2</sub> with external LDO                       | 2.7 to 5.5V                    |
| V <sub>DD1,2</sub> with internal LDO                       | 3.0 to 5.5V                    |
| V <sub>DDA</sub>                                           | 2.7 to 2.9V                    |
| V <sub>DD_IO</sub>                                         | 1.65V to V <sub>DD1</sub>      |
| Voltage on ASE                                             | 0.1V to V <sub>DDA</sub> -0.1V |
| Recommended Load Current                                   | 0mA to 300mA                   |
| Junction Temperature (T <sub>J</sub> ) Range               | -30°C to +125°C                |
| Ambient Temperature (T <sub>A</sub> ) Range <sup>(3)</sup> | -30°C to +85°C                 |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
- (2) All voltages are with respect to the potential at the GND pins.
- (3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T<sub>A-MAX</sub>) is dependent on the maximum operating junction temperature (T<sub>J-MAX-OP</sub> = 125°C), the maximum power dissipation of the device in the application (P<sub>D-MAX</sub>), and the junction-to ambient thermal resistance of the part/package in the application (θ<sub>JA</sub>), as given by the following equation: T<sub>A-MAX</sub> = T<sub>J-MAX-OP</sub> - (θ<sub>JA</sub> × P<sub>D-MAX</sub>).

## Thermal Properties

|                                                                                                           |        |
|-----------------------------------------------------------------------------------------------------------|--------|
| Junction-to-Ambient Thermal Resistance(θ <sub>JA</sub> ), YZR0036AAA or YPG0036AAA Package <sup>(1)</sup> | 60°C/W |
|-----------------------------------------------------------------------------------------------------------|--------|

- (1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

## Electrical Characteristics<sup>(1) (2)</sup>

Limits in standard typeface are for  $T_j = 25^\circ\text{C}$ . Limits in **boldface** type apply over the operating ambient temperature range ( $-30^\circ\text{C} < T_A < +85^\circ\text{C}$ ). Unless otherwise noted, specifications apply to the LP3954 Block Diagram with:  $V_{DD1} = V_{DD2} = 3.6\text{V}$ ,  $V_{DDIO} = 2.8\text{V}$ ,  $C_{VDD} = C_{VDDIO} = 100\text{nF}$ ,  $C_{OUT} = C_{IN} = 10\mu\text{F}$ ,  $C_{VDDA} = 1\mu\text{F}$ ,  $C_{REF} = 100\text{nF}$ ,  $L_1 = 4.7\mu\text{H}$ ,  $R_{FLASH} = 1.2\text{k}$ ,  $R_{RGB} = 5.6\text{k}$  and  $R_{RT} = 82\text{k}$  <sup>(3)</sup>.

| Parameter      |                                                                   | Test Conditions                                                                      | Min         | Typ      | Max         | Unit          |
|----------------|-------------------------------------------------------------------|--------------------------------------------------------------------------------------|-------------|----------|-------------|---------------|
| $I_{VDD}$      | Standby supply current ( $V_{DD1}$ , $V_{DD2}$ )                  | NSTBY = L<br>SCK, SS, SI                                                             |             | <b>1</b> | <b>8</b>    | $\mu\text{A}$ |
|                | No-boost supply current ( $V_{DD1}$ , $V_{DD2}$ )                 | NSTBY = H,<br>EN_BOOST = L<br>SCK, SS, SI<br>Audio sync and LEDs OFF                 |             |          | <b>400</b>  | $\mu\text{A}$ |
|                | No-load supply current ( $V_{DD1}$ , $V_{DD2}$ )                  | NSTBY = H,<br>EN_BOOST = H<br>SCK, SS, SI<br>Audio sync and LEDs OFF<br>Autoload OFF |             |          | <b>1</b>    | mA            |
|                | RGB drivers ( $V_{DD1}$ , $V_{DD2}$ )                             | CC mode at R1, G1, B1 and R2, G2, B2 set to 15mA                                     |             | 150      |             | $\mu\text{A}$ |
|                |                                                                   | SW mode                                                                              |             | 150      |             |               |
|                | WLED drivers ( $V_{DD1}$ , $V_{DD2}$ )                            | 4+2 banks $I_{OUT}/\text{LED}$ 25mA                                                  |             | 500      |             | $\mu\text{A}$ |
|                | Audio synchronization ( $V_{DD1}$ , $V_{DD2}$ )                   | Audio sync ON                                                                        |             |          |             | $\mu\text{A}$ |
|                |                                                                   | $V_{DD1,2} = 2.8\text{V}$                                                            |             | 390      |             |               |
|                |                                                                   | $V_{DD1,2} = 3.6\text{V}$                                                            |             | 700      |             |               |
|                | Flash ( $V_{DD1}$ , $V_{DD2}$ )                                   | $I(R_{FLASH}) = 1\text{mA}$<br>Peak current during flash                             |             | 2        |             | mA            |
| $I_{VDDIO}$    | $V_{DDIO}$ Standby Supply current                                 | NSTBY = L<br>SCK, SS, SI = H                                                         |             |          | <b>1</b>    | $\mu\text{A}$ |
|                | $V_{DDIO}$ supply current                                         | 1MHz SCK frequency in SPI mode,<br>$C_L = 50\text{pF}$ at SO pin                     |             | 20       |             | $\mu\text{A}$ |
| $I_{EXT\_LDO}$ | External LDO output current ( $V_{DD1}$ , $V_{DD2}$ , $V_{DDA}$ ) | 7V tolerant application only<br>$I_{BOOST} = 300\text{mA}$                           |             |          | <b>6.5</b>  | mA            |
| $V_{DDA}$      | Output voltage of internal LDO for analog parts                   | <sup>(4)</sup>                                                                       | <b>2.72</b> | 2.80     | <b>2.88</b> | V             |
|                |                                                                   |                                                                                      | <b>-3</b>   |          | <b>+3</b>   | %             |

(1) All voltages are with respect to the potential at the GND pins.

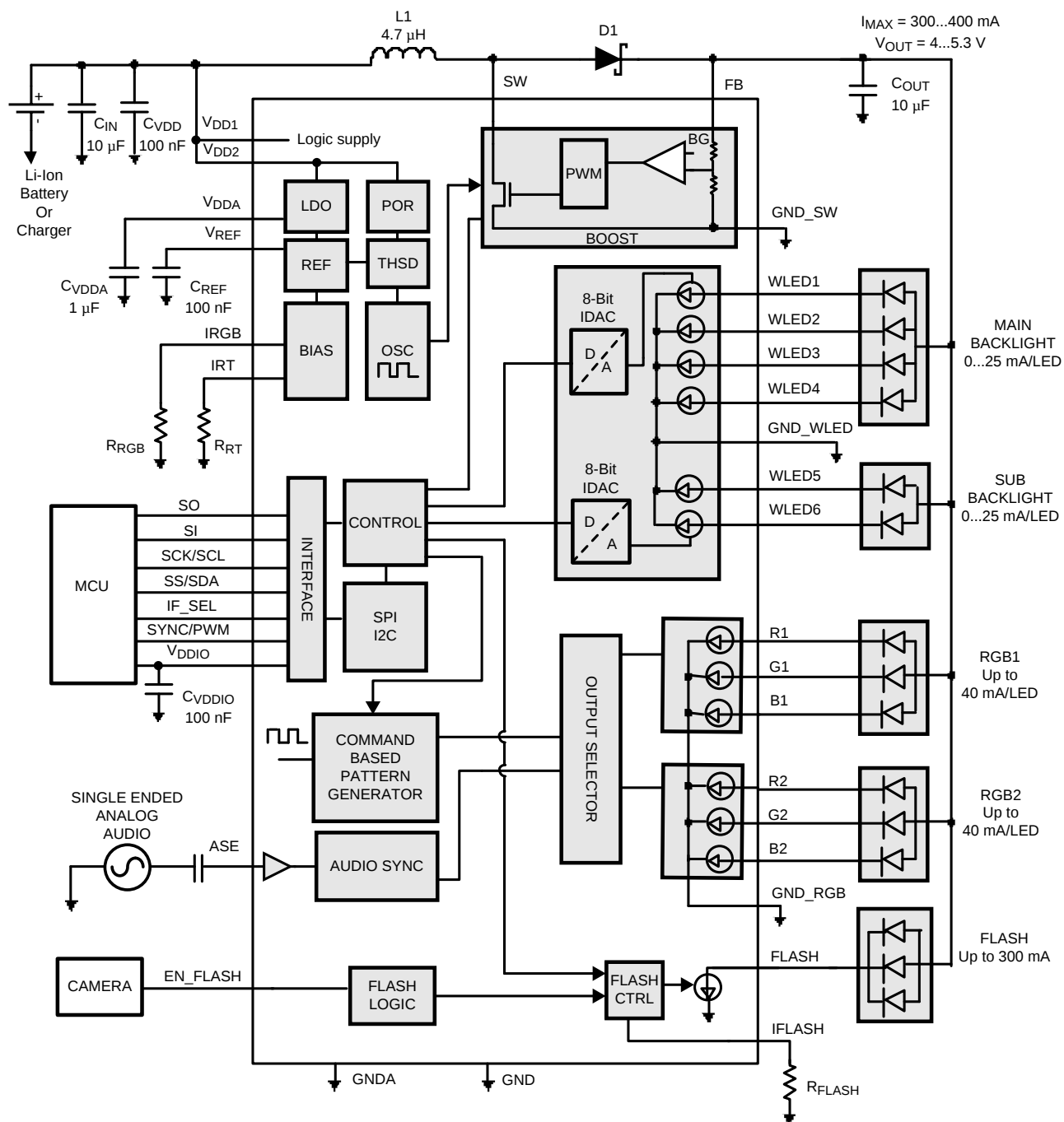
(2) Min and Max limits are ensured by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.

(3) Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.

(4)  $V_{DDA}$  output is not recommended for external use.

## DETAILED DESCRIPTION

### Block Diagram



## Modes of Operation

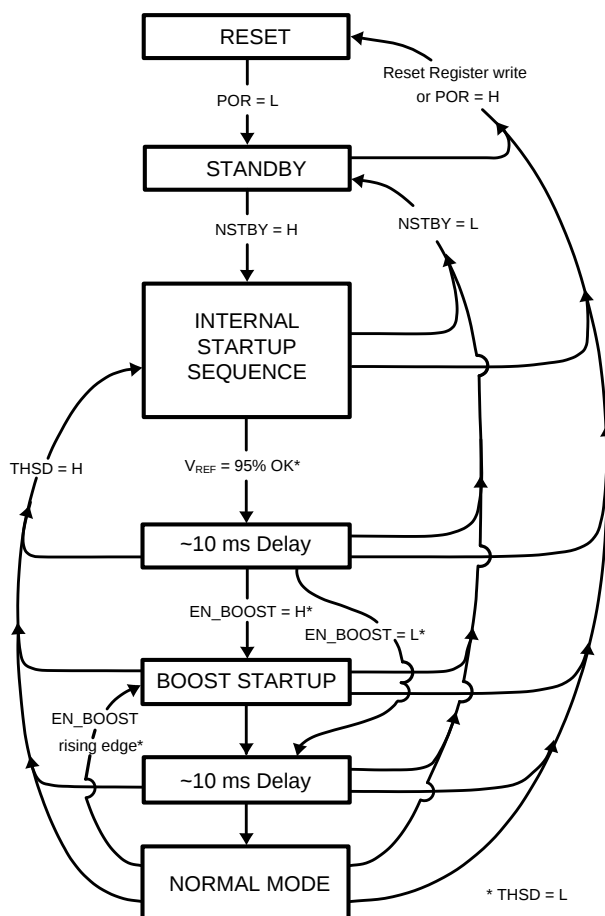
**RESET:** In the RESET mode all the internal registers are reset to the default values and the chip goes to STANDBY mode after reset. NSTBY control bit is low after reset by default. Reset is entered always if Reset Register is written or internal Power On Reset is active. There is no dedicated Reset pin available. LP3954 can be reset by writing any data to Reset Register in address 60H. Power On Reset (POR) will activate during the chip startup or when the supply voltage VDD2 falls below 1.5V. Once VDD2 rises above 1.5V, POR will inactivate and the chip will continue to the STANDBY mode.

**STANDBY:** The STANDBY mode is entered if the register bit NSTBY is LOW. This is the low power consumption mode, when all circuit functions are disabled. Registers can be written in this mode and the control bits are effective immediately after power up.

**STARTUP:** When NSTBY bit is written high, the INTERNAL STARTUP SEQUENCE powers up all the needed internal blocks (Vref, Bias, Oscillator etc.). To ensure the correct oscillator initialization, a 10ms delay is generated by the internal state-machine. If the chip temperature rises too high, the Thermal Shutdown (THSD) disables the chip operation and STARTUP mode is entered until no thermal shutdown event is present.

**BOOST STARTUP:** Soft start for boost output is generated in the BOOST STARTUP mode. The boost output is raised in PFM mode during the 10ms delay generated by the state-machine. The Boost startup is entered from Internal Startup Sequence if EN\_BOOST is HIGH or from Normal mode when EN\_BOOST is written HIGH. During the 10ms Boost Startup time all LED outputs are switched off to ensure smooth start-up.

**NORMAL:** During NORMAL mode the user controls the chip using the Control Registers. The registers can be written in any sequence and any number of bits can be altered in a register in one write



**Figure 1. Modes of Operation**

## Magnetic Boost DC/DC Converter

The LP3954 Boost DC/DC Converter generates a 4.0 – 5.3V voltage for the LEDs from single Li-Ion battery (3V...4.5V). The output voltage is controlled with an 8-bit register in 9 steps. The converter is a magnetic switching PWM mode DC/DC converter with a current limit. The converter has three options for switching frequency, 1MHz, 1.67MHz and 2MHz (default), when timing resistor  $R_T$  is 82k $\Omega$ m. Timing resistor defines the internal oscillator frequency and thus directly affects boost frequency and all circuit's internally generated timing (RGB, Flash, WLED fading).

The LP3954 Boost Converter uses pulse-skipping elimination to stabilize the noise spectrum. Even with light load or no load a minimum length current pulse is fed to the inductor. An active load is used to remove the excess charge from the output capacitor at very light loads. At very light load and when input and output voltages are very close to each other, the pulse skipping is not completely eliminated. Output voltage should be at least 0.5V higher than input voltage to avoid pulse skipping. Reducing the switching frequency will also reduce the required voltage difference.

Active load can be disabled with the `en_autoload` bit. Disabling will increase the efficiency at light loads, but the downside is that pulse skipping will occur. The Boost Converter should be stopped when there is no load to minimise the current consumption.

The topology of the magnetic boost converter is called CPM control, current programmed mode, where the inductor current is measured and controlled with the feedback. The user can program the output voltage of the boost converter. The output voltage control changes the resistor divider in the feedback loop.

The following figure shows the boost topology with the protection circuitry. Four different protection schemes are implemented:

1. Over voltage protection, limits the maximum output voltage
  - Keeps the output below breakdown voltage.
  - Prevents boost operation if battery voltage is much higher than desired output.
2. Over current protection, limits the maximum inductor current
  - Voltage over switching NMOS is monitored; too high voltages turn the switch off.
3. Feedback break protection. Prevents uncontrolled operation if FB pin gets disconnected.
4. Duty cycle limiting, done with digital control.

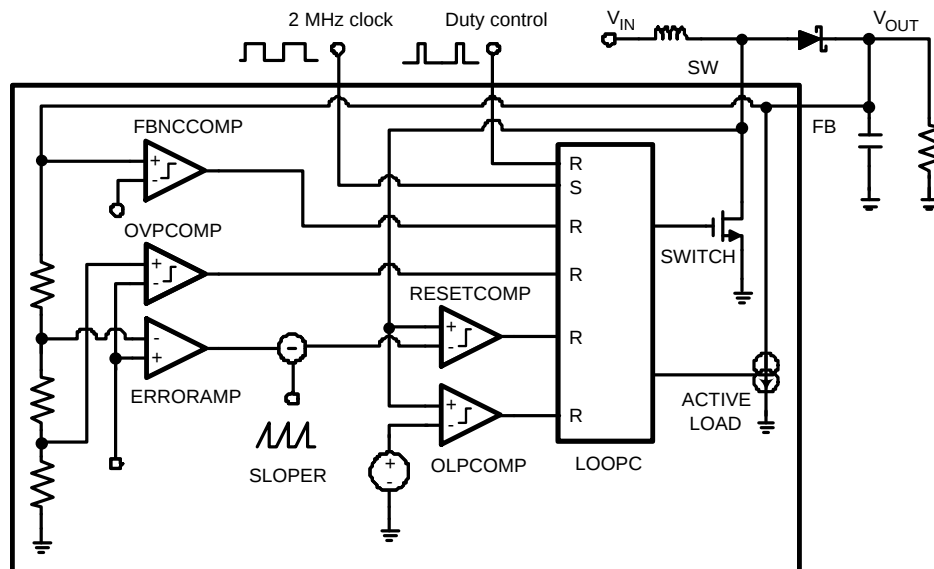


Figure 2. Boost Converter Topology

**MAGNETIC BOOST DC/DC CONVERTER ELECTRICAL CHARACTERISTICS**

| Parameter     |                                  | Test Conditions                                                                  | Min        | Typ                       | Max        | Unit     |
|---------------|----------------------------------|----------------------------------------------------------------------------------|------------|---------------------------|------------|----------|
| $I_{LOAD}$    | Load Current                     | $3.0V \leq V_{IN}$<br>$V_{OUT} = 5V$                                             | 0          |                           | 300        | mA       |
|               |                                  | $3.0V \leq V_{IN}$<br>$V_{OUT} = 4V$                                             | 0          |                           | 400        |          |
| $V_{OUT}$     | Output Voltage Accuracy (FB Pin) | $3.0V \leq V_{IN} \leq V_{OUT} - 0.5$<br>$V_{OUT} = 5.0V$                        | <b>-5</b>  |                           | <b>+5</b>  | %        |
|               | Output Voltage (FB Pin)          | $1\text{ mA} \leq I_{LOAD} \leq 300\text{ mA}$<br>$V_{IN} > 5V + V_{(SCHOTTKY)}$ |            | $V_{IN} - V_{(SCHOTTKY)}$ |            | V        |
| $R_{DS_{ON}}$ | Switch ON Resistance             | $V_{DD1,2} = 2.8V$ , $I_{SW} = 0.5A$                                             |            | 0.4                       | <b>0.8</b> | $\Omega$ |
| $f_{PWF}$     | PWM Mode Switching Frequency     | $RT = 82\text{ k}\Omega$<br>$freq\_sel[2:0] = 1XX$                               |            | 2                         |            | MHz      |
|               | Frequency Accuracy               | $2.7 \leq V_{DDA} \leq 2.9$                                                      | -6         | $\pm 3$                   | +6         | %        |
|               |                                  | $RT = 82\text{ k}\Omega$                                                         | <b>-9</b>  |                           | <b>+9</b>  |          |
| $t_{PULSE}$   | Switch Pulse Minimum Width       | no load                                                                          |            | 25                        |            | ns       |
| $t_{STARTUP}$ | Startup Time                     | Boost startup from STANDBY                                                       |            | 10                        |            | ms       |
| $I_{SW\_MAX}$ | SW Pin Current Limit             |                                                                                  | 700        | 800                       | 900        | mA       |
|               |                                  |                                                                                  | <b>550</b> |                           | <b>950</b> |          |

**BOOST STANDBY MODE**

User can stop the Boost Converter operation by writing the Enables register bit EN\_BOOST low. When EN\_BOOST is written high, the converter starts for 10ms in PFM mode and then goes to PWM mode.

**BOOST OUTPUT VOLTAGE CONTROL**

User can control the boost output voltage by boost output 8-bit register.

| Boost Output [7:0]<br>Register 0DH |           | Boost Output<br>Voltage (typical) |
|------------------------------------|-----------|-----------------------------------|
| Bin                                | Hex       |                                   |
| 0000 0000                          | 00        | 4.00                              |
| 0000 0001                          | 01        | 4.25                              |
| 0000 0011                          | 03        | 4.40                              |
| 0000 0111                          | 07        | 4.55                              |
| 0000 1111                          | 0F        | 4.70                              |
| 0001 1111                          | 1F        | 4.85                              |
| <b>0011 1111</b>                   | <b>3F</b> | <b>5.00 Default</b>               |
| 0111 1111                          | 7F        | 5.15                              |
| 1111 1111                          | FF        | 5.30                              |

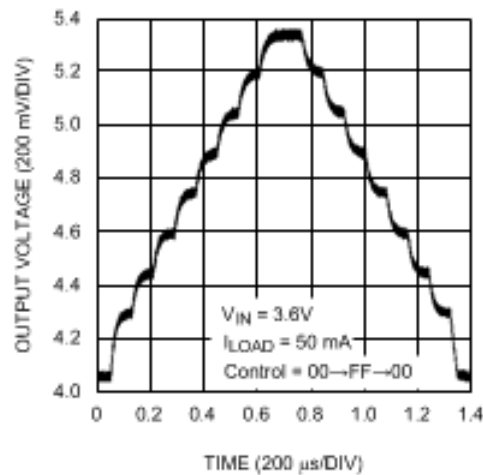


Figure 3. Boost Output Voltage Control

## BOOST FREQUENCY CONTROL

| freq_sel[2:0] <sup>(1)</sup> | frequency |
|------------------------------|-----------|
| 1XX                          | 2.00 MHz  |
| 01X                          | 1.67 MHz  |
| 001                          | 1.00 MHz  |

(1) Register 'boost freq' (address 0EH). Register default value after reset is 07H.

## Boost Converter Typical Performance Characteristics

$V_{IN} = 3.6V$ ,  $V_{OUT} = 5.0V$  if not otherwise stated

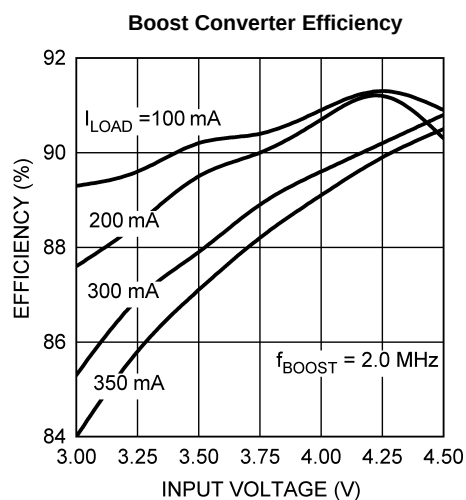


Figure 4.

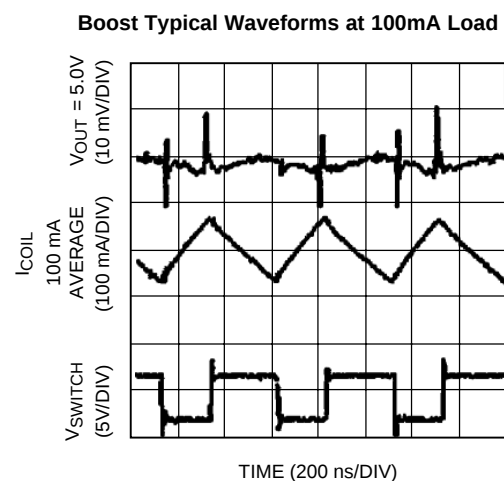


Figure 5.

$V_{in} = 3.6V$ ,  $V_{out} = 5.0V$  if not otherwise stated

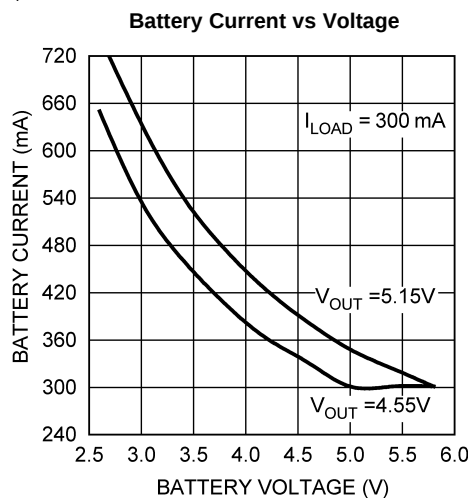


Figure 6.

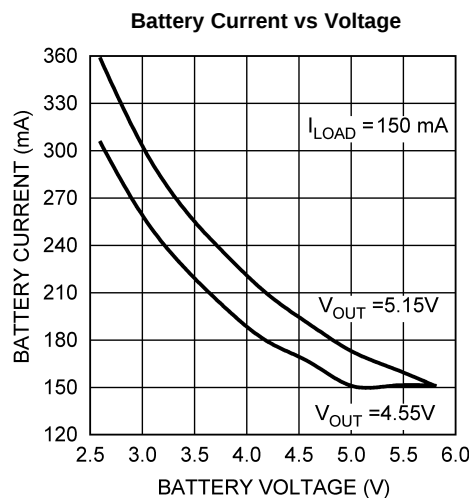


Figure 7.

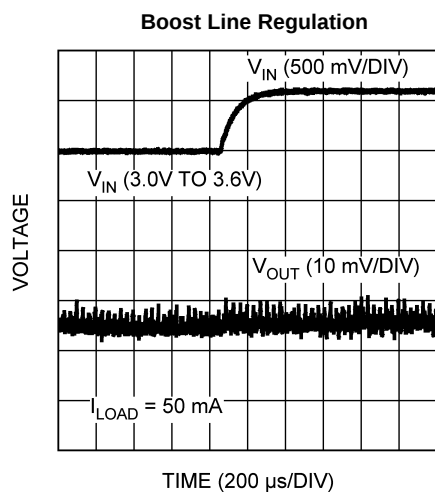


Figure 8.

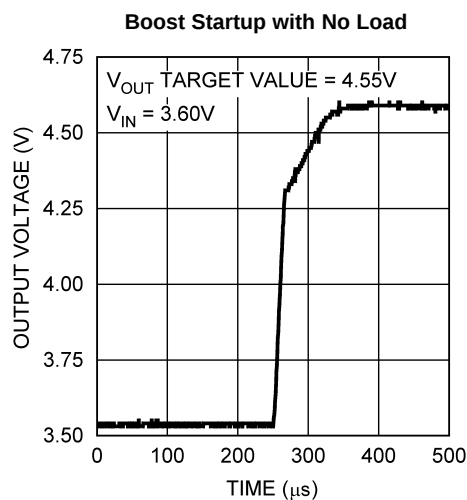


Figure 9.

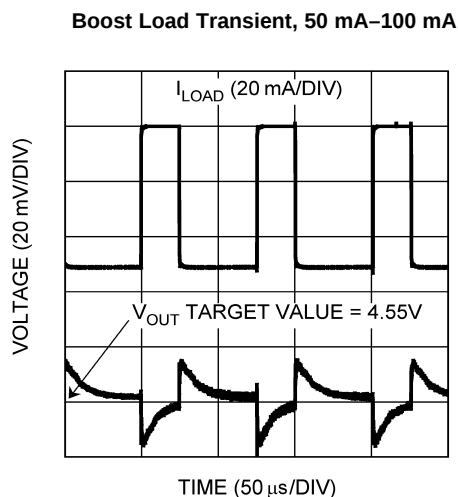


Figure 10.

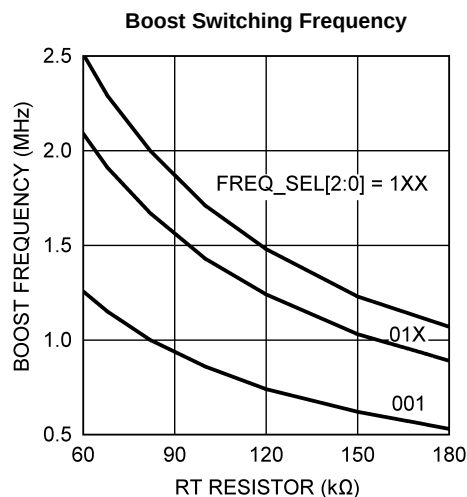
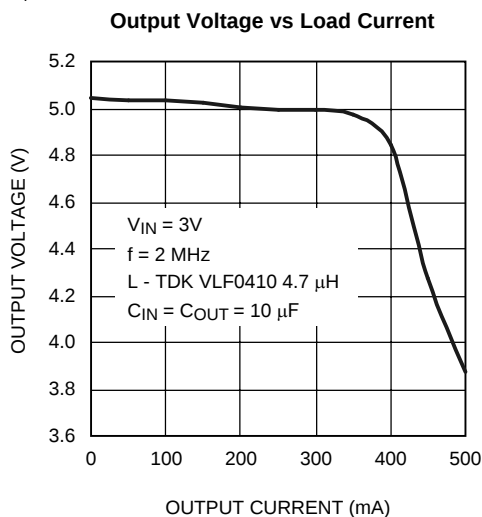
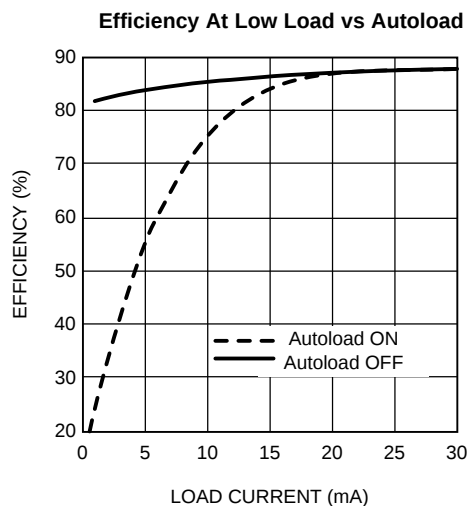


Figure 11.

V<sub>IN</sub> = 3.6V, V<sub>OUT</sub> = 5.0V if not otherwise stated



**Figure 12.**



**Figure 13.**

## Functionality of Color LED Outputs (R1, G1, B1; R2, G2, B2)

LP3954 has 2 sets of RGB/color LED outputs. Both sets have 3 outputs and the sets can be controlled in 4 different ways:

1. Command based pattern generator control (internal PWM)
2. Audio synchronization control
3. Direct ON/OFF control
4. External PWM control

By using **command based pattern generator** user can program any kind of color effect patterns. LED intensity, blinking cycles and slopes are independently controlled with 8 16-bit commands. Also real time commands are possible as well as loops and step by step control. If analog audio is available on system, the user can use **audio synchronization** for synchronizing LED blinking to the music. The different modes together with the various sub modes generate very colorful and interesting lighting effects. **Direct ON/OFF** control is mainly for switching on and off LEDs. **External PWM control** is for applications where external PWM signal is available and required to control the color LEDs. PWM signal can be connected to any color LED separately as shown later.

## COLOR LED CONTROL MODE SELECTION

The RGB\_SEL[1:0] bits in the Enables register (08H) control the output modes for RGB1 (R1, G1, B1) and RGB2 (R2, G2, B2) outputs. The following table shows the RGB\_SEL functionality.

| RGB_SEL[1:0] | Audio Sync Connected To | Command Based Pattern Generator Connected To |
|--------------|-------------------------|----------------------------------------------|
| 00           | none                    | RGB1 & RGB2                                  |
| 01           | RGB1                    | RGB2                                         |
| 10           | RGB2                    | RGB1                                         |
| 11           | RGB1 & RGB2             | none                                         |

**RGB Control register** (00H) has control bits for direct on/off control of all color LEDs. Note that the LEDs have to be turned on in order to control them with audio synchronization or pattern generator.

The external PWM signal controls any LED depending on the control register setup. The controls are in the Ext. PWM Control register (address 07H) except the FLASH control in HC\_Flash (10H) register as follows:

| Ext. PWM Control <sup>(1)</sup> |       |                                 |
|---------------------------------|-------|---------------------------------|
| wled1-4_pwm                     | bit 7 | PWM controls WLED 1-4           |
| wled5-6_pwm                     | bit 6 | PWM controls WLED 5-6           |
| r1_pwm                          | bit 5 | PWM controls R1 output          |
| g1_pwm                          | bit 4 | PWM controls G1 output          |
| b1_pwm                          | bit 3 | PWM controls B1 output          |
| r2_pwm                          | bit 2 | PWM controls R2 output          |
| g2_pwm                          | bit 1 | PWM controls G2 output          |
| b2_pwm                          | bit 0 | PWM controls B2 output          |
| HC_Flash                        |       |                                 |
| hc_pwm                          | bit 5 | PWM controls high current flash |

- (1) **Note:** If DISPL=1, wled1-4pwm controls WLED1-6  
**Note:** Maximum external PWM frequency is 1kHz. If during the external PWM control the internal PWM is on the result will be product of both functions.

### CURRENT CONTROL OF COLOR LED OUTPUTS (R1, R2, G1, G2, B1, B2)

Both RGB output sets can be separately controlled as constant current sinks or as switches. This is done using cc\_rgb1/2 bits in the RGB control register. In constant current mode one or both RGB output sets are controlled with constant current sinks (no external ballast resistors required). The maximum output current for both drivers is set by one external resistor  $R_{RGB}$ . User can decrease the maximum current for an individual LED driver by programming as shown later.

The maximum current for all RGB drivers is set with  $R_{RGB}$ . The equation for calculating the maximum current is

$$I_{MAX} = 100 \times 1.23V / (R_{RGB} + 50\Omega) \quad (1)$$

where

$I_{MAX}$  - maximum RGB current in any RGB output in constant current mode

1.23V - reference voltage

100 - internal current mirror multiplier

$R_{RGB}$  - resistor value in Ohms

50Ω - internal resistor in the  $I_{RGB}$  input

For example if 22mA is required for maximum RGB current  $R_{RGB}$  equals to

$$R_{RGB} = 100 \times 1.23V / I_{MAX} - 50\Omega = 123V / 0.022A - 50\Omega = 5.54k\Omega \quad (2)$$

Each individual RGB output has a separate maximum current programming. The control bits are in registers **RGB1 max current** and **RGB2 max current** (12H and 13H) and programming is shown in table below. The default value after reset is 00.

| IR1[1:0], IG1[1:0],<br>IB1[1:0], IR2[1:0],<br>IG2[1:0], IB2[1:0] | Maximum<br>Current/Output |
|------------------------------------------------------------------|---------------------------|
| 00                                                               | $0.25 \times I_{MAX}$     |
| 01                                                               | $0.50 \times I_{MAX}$     |
| 10                                                               | $0.75 \times I_{MAX}$     |
| 11                                                               | $1.00 \times I_{MAX}$     |

### SWITCH MODE

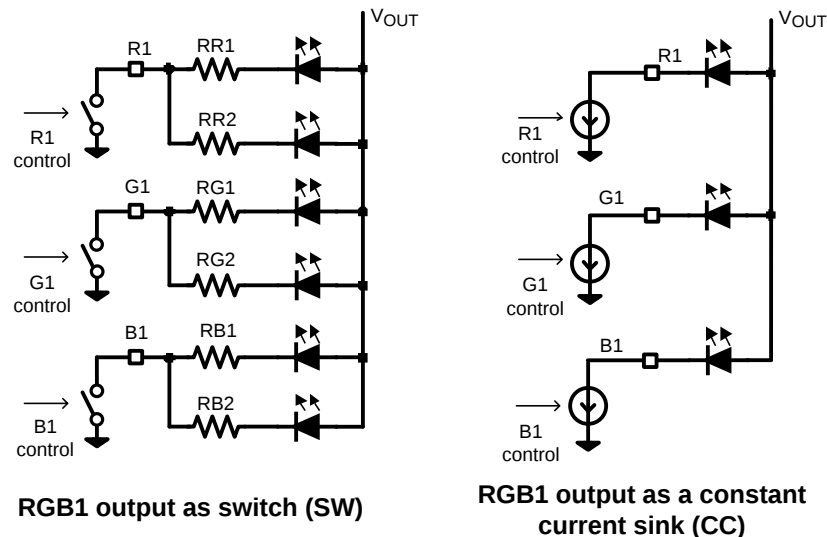
The switch mode is used if there is a need to connect parallel LEDs to output or if the RGB output current needs to be increased.

Please note that the switch mode **requires an external ballast resistors** at each output to limit the LED current.

The switch/current mode and on/off controls for RGB are in the RGB\_ctrl register (00H) as follows:

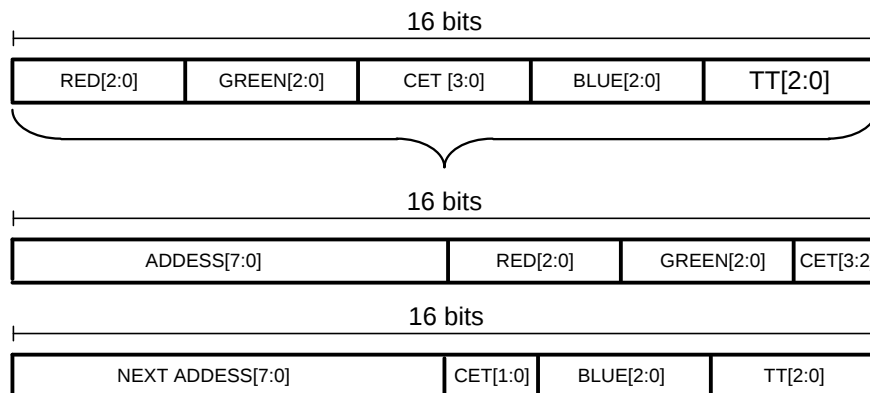
**Table 2. RGB\_ctrl Register (00H)**

|                |      |   |                                                                      |
|----------------|------|---|----------------------------------------------------------------------|
| <b>CC_RGB1</b> | bit7 | 1 | R1, G1 and B1 are switches → limit current with ballast resistor     |
|                |      | 0 | R1, G1 and B1 are constant current sinks, current limited internally |
| <b>CC_RGB2</b> | bit6 | 1 | R2, G2 and B2 are switches → limit current with ballast resistor     |
|                |      | 0 | R2, G2 and B2 are constant current sinks, current limited internally |
| <b>r1sw</b>    | bit5 | 1 | R1 is on                                                             |
|                |      | 0 | R1 is off                                                            |
| <b>g1sw</b>    | bit4 | 1 | G1 is on                                                             |
|                |      | 0 | G1 is off                                                            |
| <b>b1sw</b>    | bit3 | 1 | B1 is on                                                             |
|                |      | 0 | B1 is off                                                            |
| <b>r2sw</b>    | bit2 | 1 | R2 is on                                                             |
|                |      | 0 | R2 is off                                                            |
| <b>g2sw</b>    | bit1 | 1 | G2 is on                                                             |
|                |      | 0 | G2 is off                                                            |
| <b>b2sw</b>    | bit0 | 1 | B2 is on                                                             |
|                |      | 0 | B2 is off                                                            |



## Command Based Pattern Generator for Color LEDs

The LP3954 has a unique stand-alone command based pattern generator with 8 user controllable 16-bit wide commands. Since write registers are 8-bit long one command requires 2 write cycles. Each command has intensity level for each LED, command execution time (CET) and transition time (TT). The command structure is shown in following two figures.



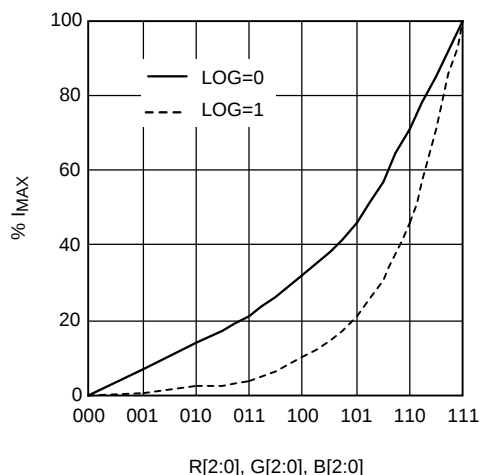
### COMMAND REGISTER WITH 8 COMMANDS

|           |             |      |      |    |    |    |     |      |      |
|-----------|-------------|------|------|----|----|----|-----|------|------|
| COMMAND 1 | ADDRESS 50H | R2   | R1   | R0 | G2 | G1 | G0  | CET3 | CET2 |
|           | ADDRESS 51H | CET1 | CET0 | B2 | B1 | B0 | TT2 | TT1  | TT0  |
| COMMAND 2 | ADDRESS 52H | R2   | R1   | R0 | G2 | G1 | G0  | CET3 | CET2 |
|           | ADDRESS 53H | CET1 | CET0 | B2 | B1 | B0 | TT2 | TT1  | TT0  |
| COMMAND 3 | ADDRESS 54H | R2   | R1   | R0 | G2 | G1 | G0  | CET3 | CET2 |
|           | ADDRESS 55H | CET1 | CET0 | B2 | B1 | B0 | TT2 | TT1  | TT0  |
| COMMAND 4 | ADDRESS 56H | R2   | R1   | R0 | G2 | G1 | G0  | CET3 | CET2 |
|           | ADDRESS 57H | CET1 | CET0 | B2 | B1 | B0 | TT2 | TT1  | TT0  |
| COMMAND 5 | ADDRESS 58H | R2   | R1   | R0 | G2 | G1 | G0  | CET3 | CET2 |
|           | ADDRESS 59H | CET1 | CET0 | B2 | B1 | B0 | TT2 | TT1  | TT0  |
| COMMAND 6 | ADDRESS 5AH | R2   | R1   | R0 | G2 | G1 | G0  | CET3 | CET2 |
|           | ADDRESS 5BH | CET1 | CET0 | B2 | B1 | B0 | TT2 | TT1  | TT0  |
| COMMAND 7 | ADDRESS 5CH | R2   | R1   | R0 | G2 | G1 | G0  | CET3 | CET2 |
|           | ADDRESS 5DH | CET1 | CET0 | B2 | B1 | B0 | TT2 | TT1  | TT0  |
| COMMAND 8 | ADDRESS 5EH | R2   | R1   | R0 | G2 | G1 | G0  | CET3 | CET2 |
|           | ADDRESS 5FH | CET1 | CET0 | B2 | B1 | B0 | TT2 | TT1  | TT0  |

### COLOR INTENSITY CONTROL

Each color, Red, Green and Blue, has 3-bit intensity levels. The level control is logarithmic. 2 logarithmic curves are available. The LOG bit in Pattern\_gen\_ctrl register (11H) defines the curve used. The values for both logarithmic curves are shown in following table.

| R[2:0], G[2:0],<br>B[2:0] | CURRENT<br>[% × I <sub>MAX(COLOR)</sub> ] |       |
|---------------------------|-------------------------------------------|-------|
|                           | LOG=0                                     | LOG=1 |
| 000                       | 0                                         | 0     |
| 001                       | 7                                         | 1     |
| 010                       | 14                                        | 2     |
| 011                       | 21                                        | 4     |
| 100                       | 32                                        | 10    |
| 101                       | 46                                        | 21    |
| 110                       | 71                                        | 46    |
| 111                       | 100                                       | 100   |



### COMMAND EXECUTION TIME (CET) AND TRANSITION TIME (TT)

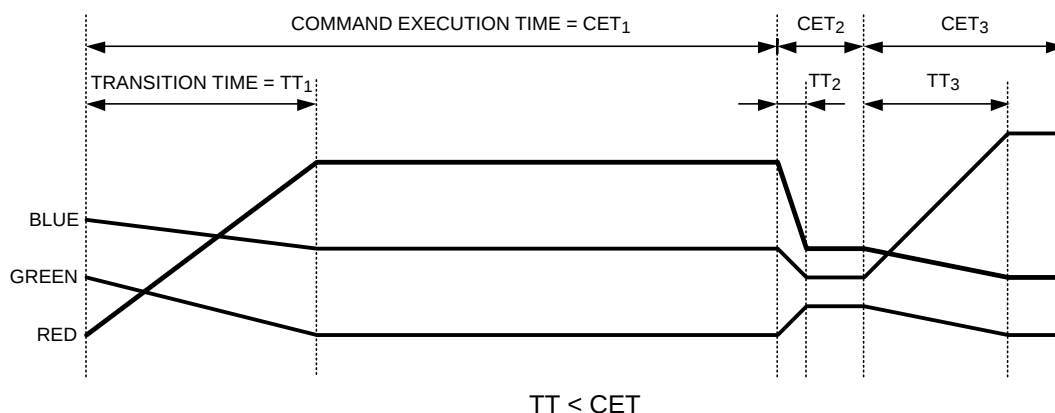
The command execution CET time is the duration of one single command. Command execution times CET are defined as follows, when  $R_T=82k$ :

| CET [3:0] | CET duration, ms |
|-----------|------------------|
| 0000      | 197              |
| 0001      | 393              |
| 0010      | 590              |
| 0011      | 786              |
| 0100      | 983              |
| 0101      | 1180             |
| 0110      | 1376             |
| 0111      | 1573             |
| 1000      | 1769             |
| 1001      | 1966             |
| 1010      | 2163             |
| 1011      | 2359             |
| 1100      | 2556             |
| 1101      | 2753             |
| 1110      | 2949             |
| 1111      | 3146             |

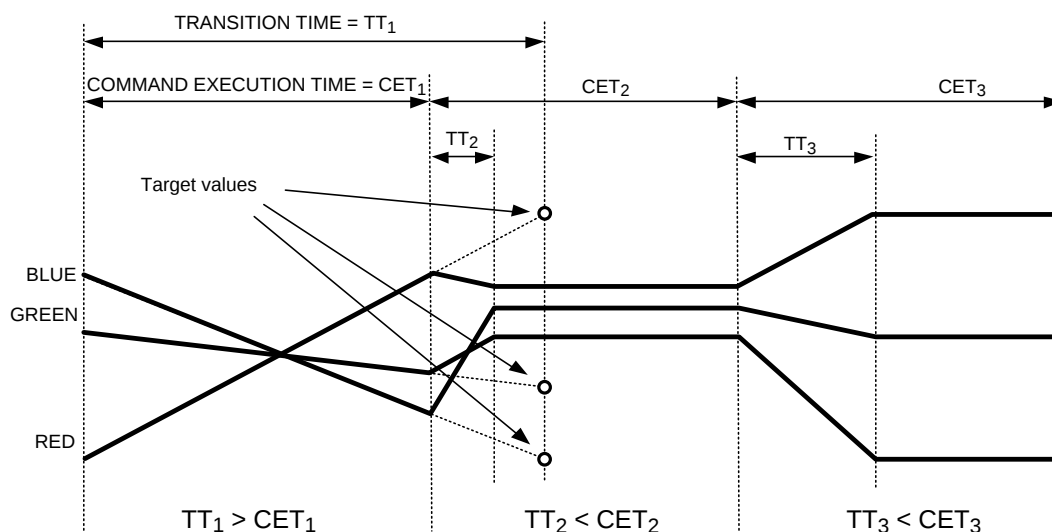
Transition time TT is duration of transition from the previous RGB value to programmed new value. Transition times TT are defined as follows:

| TT [2:0] | Transition time, ms |
|----------|---------------------|
| 000      | 0                   |
| 001      | 55                  |
| 010      | 110                 |
| 011      | 221                 |
| 100      | 442                 |
| 101      | 885                 |
| 110      | 1770                |
| 111      | 3539                |

The figure below shows an example of RGB CET and TT times.

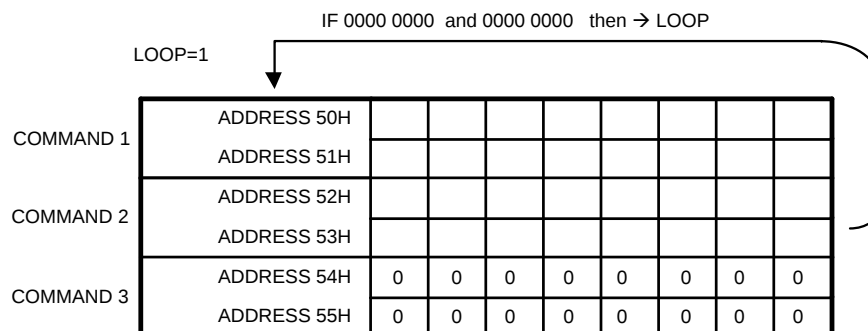


The command execution time also may be less than the transition time – the figure below illuminates this case.



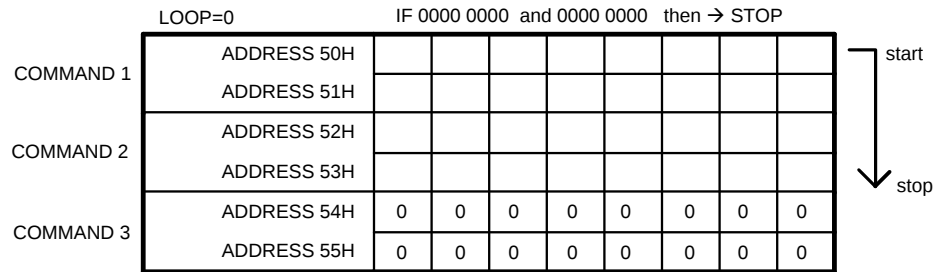
## LOOP CONTROL

Pattern generator commands can be looped using the LOOP bit (D1) in Pattern gen ctrl register (11H). If LOOP=1 the program will be looped from the command 8 register or if there is 0000 0000 and 0000 0000 in one command register. The loop will start from command 1 and continue until stopped by writing rgb\_start=0 or loop=0. The example of loop is shown in following figure:



## SINGLE PROGRAM

If control bit LOOP=0 the program will start from Command 1 and run to either last command or to empty “0000 0000 / 0000 0000” command.



The LEDs maintain the brightness of the last command when the single program stops. Changes in command register will not be effective in this phase. The RGB\_START bit has to be toggled off and on to make changes effective.

## START BIT

Pattern\_gen\_ctrl register's RGB\_START bit will enable command execution starting from Command 1.

| Pattern gen ctrl register (11H) |       |                                                                                                                    |
|---------------------------------|-------|--------------------------------------------------------------------------------------------------------------------|
| rgb_start                       | Bit 2 | 0 – Pattern generator disabled<br>1 – execution pattern starting from command 1                                    |
| loop                            | Bit 1 | 0 – pattern generator loop disabled (single pattern)<br>1 – pattern generator loop enabled (execute until stopped) |
| log                             | Bit 0 | 0 – color intensity mode 0<br>1 – color intensity mode 1                                                           |

## HARDWARE ON/OFF CONTROL AND DIMMING

PWM\_LED input can be used as direct ON/OFF control or PWM dimming control for selected RGB outputs or the WLED groups. PWM\_LED control can be enabled with the control bits in the **Ext. PWM Control** register.

## Audio Synchronization

The color LEDs connected to RGB outputs can be synchronized to incoming audio with Audio Synchronization feature. Audio Sync has 2 modes. **Amplitude mode** synchronizes color LEDs based on input signal's peak amplitude. In the amplitude mode the user can select between 3 different amplitude mapping modes and 4 different speed configurations. The **frequency mode** synchronizes the color LEDs based on bass, middle and treble amplitudes (= low pass, band pass and high pass filters). User can select between 2 different frequency responses and 4 different speed configurations for best audio-visual user experience. Programmable gain and AGC function are also available for adjustment of input signal amplitude to light response. The Audio Sync functionality is described more closely below.

## USING A DIGITAL PWM AUDIO SIGNAL AS AN AUDIO SYNCHRONIZATION SOURCE

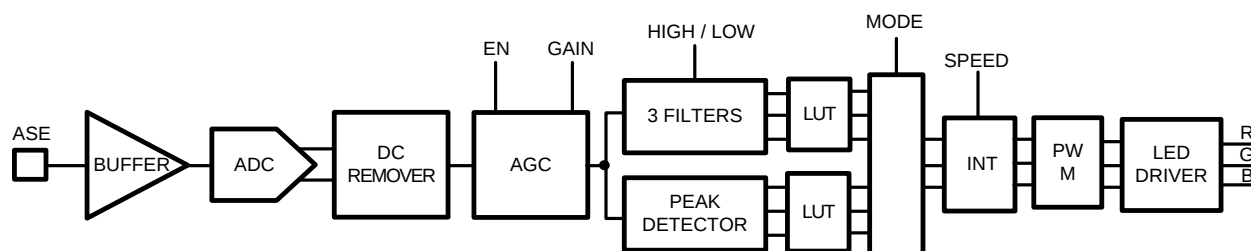
If the input signal is a PWM signal, use a first or second order low pass filter to convert the digital PWM audio signal into an analog waveform. There are two parameters that need to be known to get the filter to work successfully: frequency of the PWM signal and the voltage level of the PWM signal. Suggested cut-off frequency (-3dB) should be around 2 kHz to 4 kHz and the stop-band attenuation at sampling frequency should be around -48dB or better. Use a resistor divider to reduce the digital signal amplitude to meet the specification of the analog audio input. Because a low-order low-pass filter attenuates the high-frequency components from audio signal, MODE\_CONTROL=[01] selection is recommended when frequency synchronization mode is enabled. Application example 5 shows an example of a second order RC-filter for 29 kHz PWM signal with 3.3V amplitude. Active filters, such as a Sallen-Key filter, may also be applied. An active filter gives better stop-band attenuation and cut-off frequency can be higher than for a RC-filter.

To make sure that the filter rolls off sufficiently quickly, connect your filter circuit to the audio input(s), turn on the audio synchronization feature, set manual gain to maximum, apply the PWM signal to the filter input and keep an eye on LEDs. If they are blinking without an audio signal (modulation), a sharper roll-off after the cut-off frequency, more stop-band attenuation, or smaller amplitude of the PWM signal is required.

## AUDIO SYNCHRONIZATION SIGNAL PATH

LP3954 audio synchronization is mainly done digitally and it consists of the following signal path blocks:

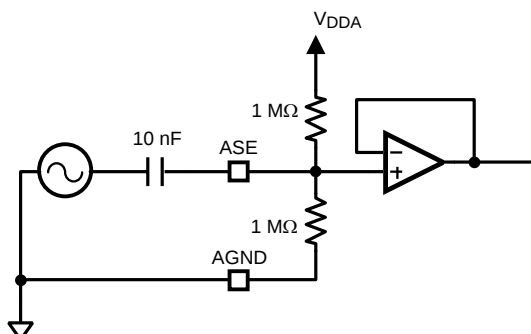
- Input Buffers
- AD Converter
- DC Remover
- Automatic Gain Control (AGC)
- Programmable Gain
- 3 Band Digital Filter
- Peak Detector
- Look-up Tables (LUT)
- Mode Selector
- Integrators
- PWM Generator
- Output Drivers



The digitized input signal has DC component that is removed by digital **DC REMOVER** (-3dB at 400Hz). Since the light response of input audio signal is very much amplitude dependent the AGC adjusts the input signal to suitable range automatically. User can disable **AGC** and the gain can be set manually with **PROGRAMMABLE GAIN**. LP3954 has 2 audio synchronization modes: amplitude and frequency. For amplitude based synchronization the **PEAK DETECTION** method is used. For frequency based synchronization **3 BAND FILTER** separates high pass, low pass and band pass signals. For both modes the predefined LUT is used to optimize the audio visual effect. **MODE SELECTOR** selects the synchronization mode. Different response times to music beat can be selected using **INTEGRATOR** speed variables. Finally **PWM GENERATOR** sets the driver FET duty cycles.

## INPUT SIGNAL TYPE AND BUFFERING

LP3954 supports single ended audio input as shown in the figure below. The electric parameters of the buffer are described in the Audio Synch table. The buffer is rail-to-rail input operational amplifier connected as a voltage follower. DC level of the input signal is set by a simple resistor divider



## AUDIO SYNC ELECTRICAL PARAMETERS

| Symbol    | Parameter                              | Test Conditions | Min        | Typ         | Max             | Unit |
|-----------|----------------------------------------|-----------------|------------|-------------|-----------------|------|
| $Z_{IN}$  | Input Impedance of ASE                 |                 | <b>250</b> | 500         |                 | kOhm |
| $A_{IN}$  | Audio Input Level Range (peak-to-peak) | Gain = 21dB     | <b>0.1</b> |             | $V_{DDA} - 0.1$ | V    |
|           |                                        | Gain = 0 dB     |            |             |                 |      |
| $f_{3dB}$ | Crossover Frequencies (-3 dB)          |                 |            |             |                 | kHz  |
|           | Narrow Frequency Response              | Low Pass        |            | 0.5         |                 |      |
|           |                                        | Band Pass       |            | 1.0 and 1.5 |                 |      |
|           |                                        | High Pass       |            | 2.0         |                 |      |
|           | Wide Frequency Response                | Low Pass        |            | 1.0         |                 |      |
|           |                                        | Band Pass       |            | 2.0 and 3.0 |                 |      |
|           |                                        | High Pass       |            | 4.0         |                 |      |

## CONTROL OF AUDIO SYNCHRONIZATION

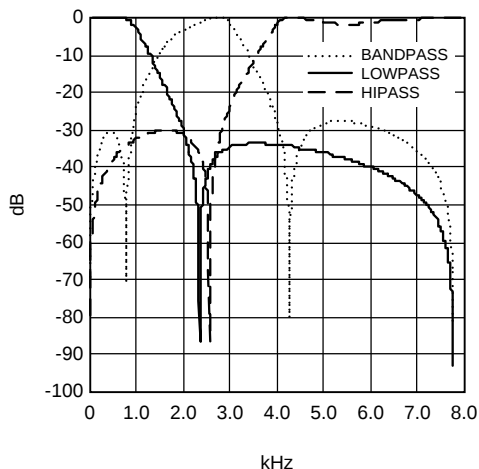
The following table describes the controls required for audio synchronization.

| Audio_sync_CTRL1 (2AH) |          |                                                                                                                                                                                                                                         |               |  |               |
|------------------------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|--|---------------|
| GAIN_SEL[2:0]          | Bits 7-5 | Input signal gain control. Range 0...21 dB, step 3 dB:                                                                                                                                                                                  |               |  |               |
|                        |          | [000] = 0 dB (default)                                                                                                                                                                                                                  | [011] = 9 dB  |  | [110] = 18 dB |
|                        |          | [001] = 3 dB                                                                                                                                                                                                                            | [100] = 12 dB |  | [111] = 21 dB |
|                        |          | [010] = 6 dB                                                                                                                                                                                                                            | [101] = 15 dB |  |               |
| SYNC_MODE              | Bit 4    | Synchronization mode selector.<br>SYNCMODE = 0 → Amplitude Mode (default)<br>SYNCMODE = 1 → Frequency Mode                                                                                                                              |               |  |               |
| EN_AGC                 | Bit 3    | Automatic Gain Control enable<br>1 = enabled<br>0 = disabled (Gain Select enabled) (default)                                                                                                                                            |               |  |               |
| EN_SYNC                | Bit 2    | Audio synchronization enable<br>1 = Enabled<br>Note : If AGC is enabled, AGC gain starts from current GAIN_SEL gain value.<br>0 = Disabled (default)                                                                                    |               |  |               |
| INPUT_SEL[1:0]         | Bits 1-0 | [00] = Single ended input signal, ASE.<br>[01] = Temperature measurement<br>[10] = Ambient light measurement<br>[11] = No input (default)                                                                                               |               |  |               |
| Audio_sync_CTRL2 (2BH) |          |                                                                                                                                                                                                                                         |               |  |               |
| EN_AVG                 | Bit 4    | 0 – average disabled (not applicable in audio synchronization mode)<br>1 – average enabled (not applicable in audio synchronization mode)                                                                                               |               |  |               |
| MODE_CTRL[1:0]         | Bits 3-2 | See below: Mode control                                                                                                                                                                                                                 |               |  |               |
| SPEED_CTRL[1:0]        | Bits 1-0 | Sets the LEDs light response time to audio input.<br>[00] = FASTEST (default)<br>[01] = FAST<br>[10] = MEDIUM<br>[11] = SLOW<br>(For SLOW setting in amplitude mode f <sub>MAX</sub> =3.8Hz,<br>Frequency mode f <sub>MAX</sub> =7.6Hz) |               |  |               |

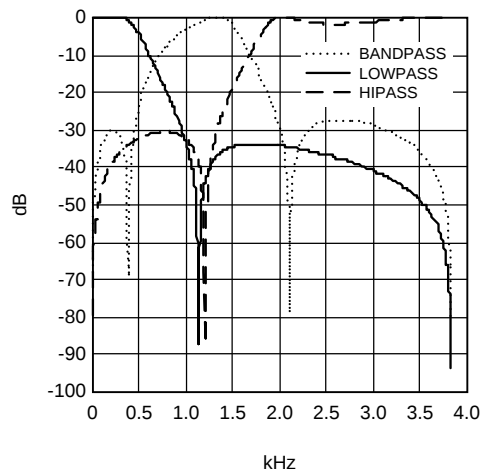
## MODE CONTROL IN FREQUENCY MODE

Mode control has two setups based on audio synchronization mode select: the frequency mode and the amplitude mode. During the **frequency mode** user can select two filter options by MODE\_CTRL as shown below. User can select the filters based on the music type and light effect requirements. In the first mode the frequency range extends to 8 kHz in the second to 4 kHz.

The lowpass filter is used for the red, the bandpass filter for the blue and the hipass filter for the green LED.



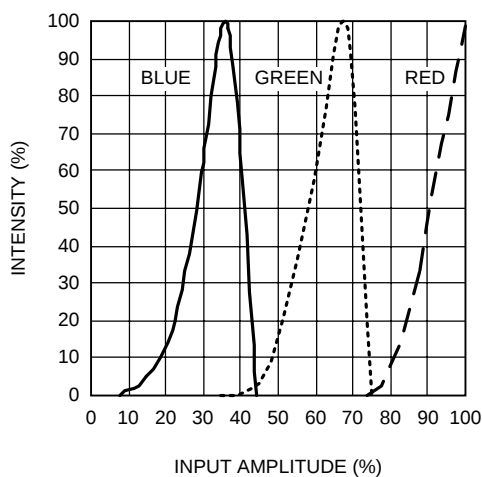
**Figure 14. Higher frequency mode**  
**MODE\_CTRL = 00 and SYNC\_MODE = 1**



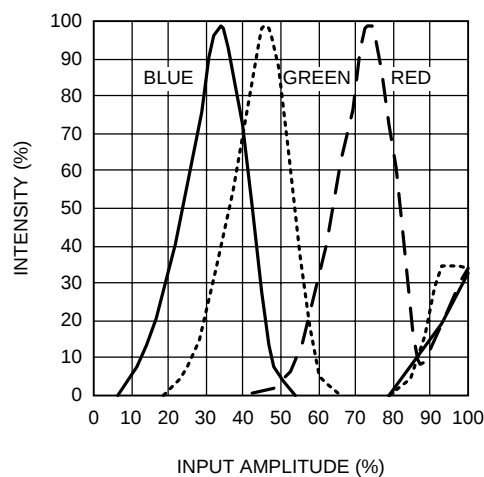
**Figure 15. Lower frequency mode**  
**MODE\_CTRL = 01 and SYNC\_MODE = 1**

### MODE CONTROL IN AMPLITUDE MODE

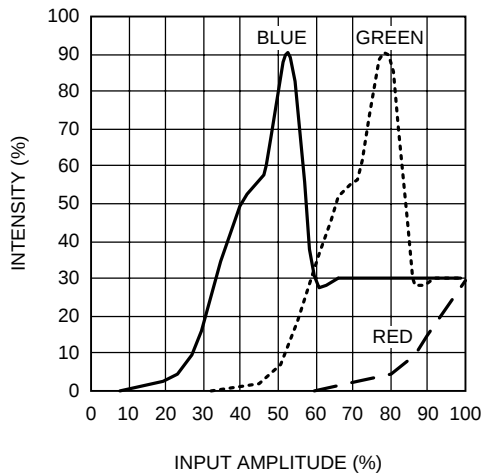
During the **amplitude synchronization mode** user can select between three different amplitude mappings by using MODE\_CTRL select. These three mapping option gives different light response. The modes are shown in the tables below.



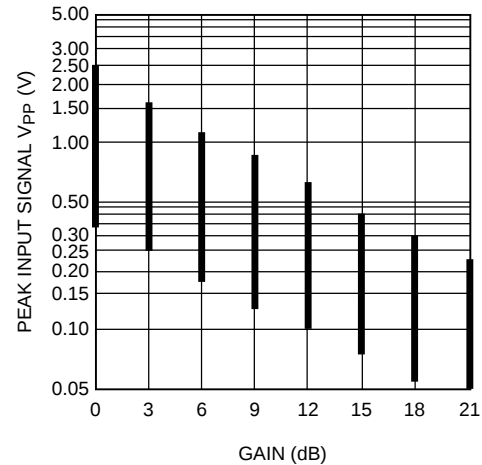
**Figure 16. Non-overlapping mode**  
**MODE\_CTRL[1:0] = [01]**



**Figure 17. Partly overlapping mode**  
**MODE\_CTRL[1:0] = [00]**



**Figure 18. Overlapping mode MODE\_CTRL[1:0] = [10]**



**Figure 19. Peak Input Signal Level Range vs Gain Setting**

### RGB OUTPUT SYNCHRONIZATION TO EXTERNAL CLOCK

The RGB pattern generator and high current flash driver timing can be synchronized to external clock with following configuration.

1. Set PWM\_SYNC bit in Enables register to 1
2. Feed PWM\_SYNC pin with 5 MHz clock

By this the internal 5 MHz clock is disabled from pattern generator and flash timing circuitry.

The external clock signal frequency will fully determine the timings related to RGB and Flash.

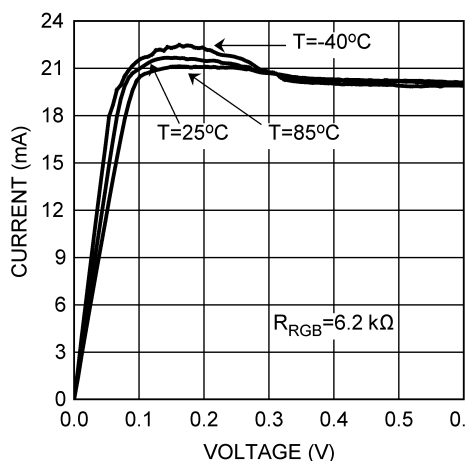
Note: The boost converter will use internal 5 MHz clock even if the external clock is available.

### RGB Driver Typical Performance Characteristics

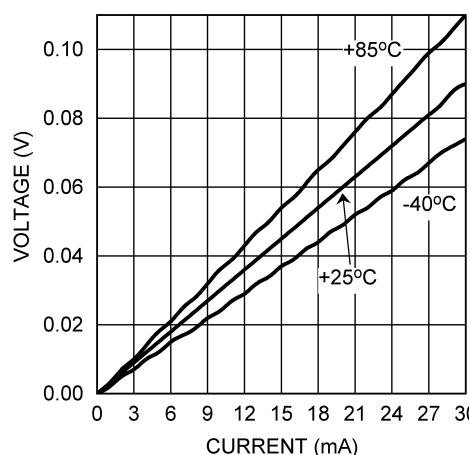
#### RGB DRIVER ELECTRICAL CHARACTERISTICS (R1, G1, B1, R2, G2, B2 OUTPUTS)

| Parameter      | Test Conditions                                 | Min                                            | Typ         | Max       | Unit            |
|----------------|-------------------------------------------------|------------------------------------------------|-------------|-----------|-----------------|
| $I_{LEAKAGE}$  | R1, G1, B1, R2, G2, B2 pin leakage current      |                                                | 0.1         | <b>1</b>  | $\mu A$         |
| $I_{MAX(RGB)}$ | Maximum recommended sink current <sup>(1)</sup> | CC mode                                        |             | <b>40</b> | mA              |
|                |                                                 | SW mode                                        |             | <b>50</b> | mA              |
|                | Accuracy at 37mA                                | $R_{RGB}=3.3\text{ k}\Omega \pm 1\%$ , CC mode | $\pm 5$     |           | %               |
|                | Current mirror ratio                            | CC mode                                        | 1:100       |           |                 |
|                | RGB1 and RGB2 current mismatch                  | $I_{RGB}=37\text{mA}$ , CC mode                | $\pm 5$     |           | %               |
| $R_{SW}$       | Switch resistance                               | SW mode                                        | 2.5         | <b>4</b>  | $\Omega$        |
| $f_{RGB}$      | RGB switching frequency                         | Accuracy proportional to internal clock freq.  | <b>18.2</b> | 20        | <b>21.8</b> kHz |
|                |                                                 | If external SYNC 5MHz is in use                |             | 20        | kHz             |

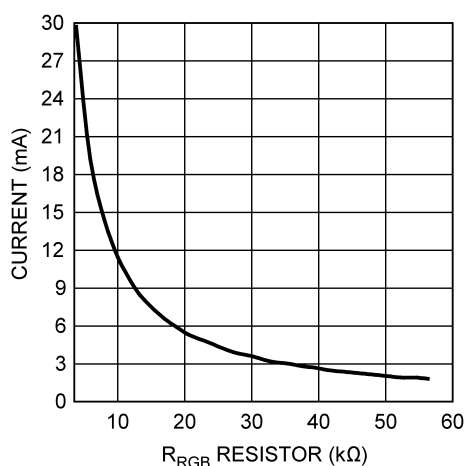
- (1) **Note:** RGB current should be limited as follows:  
**constant current mode** – limit by external  $R_{RGB}$  resistor;  
**switch mode** – limit by external ballast resistors



**Figure 20. Output Current vs Pin Voltage (Current Sink Mode)**



**Figure 21. Pin Voltage vs Output Current (Switch Mode)**



**Figure 22. Output Current vs  $R_{RGB}$  (Current Sink Mode)**

### Single High Current Driver

LP3954 has internal constant current driver that is capable for driving high current mainly targeted for FLASH LED in camera phone applications.

### MAXIMUM CURRENT SETUP FOR FLASH

The user sets the maximum current of FLASH with  $R_{FLASH}$  resistor based on following equation:

$$I_{MAX} = 300 \times 1.23V / (R_{FLASH} + 50\Omega), \quad (3)$$

where

$I_{max}$  = maximum flash current in Amps (ie. 0.3A)

1.23V = reference voltage

300 = internal current mirror multiplier

$R_{FLASH}$  = Resistor value in Ohms

50Ω = Internal resistor in the  $I_{FLASH}$  input

For example if 300mA is required for maximum flash current  $R_{FLASH}$  equals to

$$R_{FLASH} = 300 \times 1.23V / I_{MAX} - 50\Omega = 369V / 0.3A - 50\Omega = 1.18k\Omega \quad (4)$$

## CURRENT CONTROL FOR FLASH

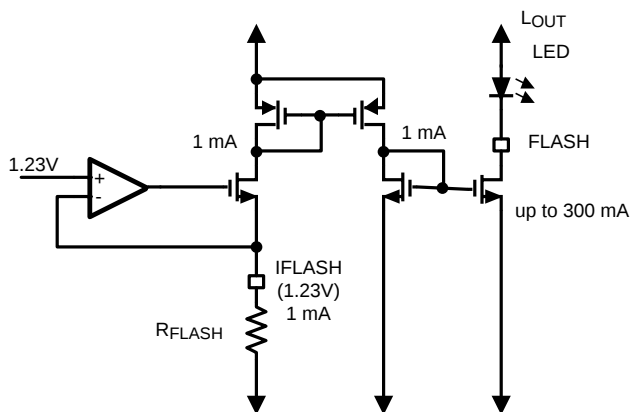
To minimize the internal current consumption, the flash function has an enable bit EN\_HCFLASH in the HC Flash register.

| EN_HCFLASH |                                                                         |
|------------|-------------------------------------------------------------------------|
| 0          | FLASH disabled, no extra current consumption through R <sub>FLASH</sub> |
| 1          | FLASH enabled, IFLASH set by HC_SW[1:0] (see below)                     |

HC[1:0] bits in the HC Flash register control the FLASH current as show in following table.

| HC[1:0] | I(FLASH)                            |
|---------|-------------------------------------|
| 00      | $0.25 \times I_{\text{MAX(FLASH)}}$ |
| 01      | $0.50 \times I_{\text{MAX(FLASH)}}$ |
| 10      | $0.75 \times I_{\text{MAX(FLASH)}}$ |
| 11      | $1.00 \times I_{\text{MAX(FLASH)}}$ |

Figure 23 shows the internal structure for the FLASH driver.



**Figure 23. Internal Structure of Flash Driver**

## FLASH TIMING

Flash output is turned on in lower current **View finder** mode when the EN\_HCFFLASH bit is written high. The actual Flash at maximum current starts when the EN\_FLASH i/o-pin goes high. The Flash length can be selected from 3 pre-defined values or EN\_FLASH pin pulse length can determine the length. The pulse length is controlled by the FT\_T[1:0] bits as show in the table below.

| FL_T[1:0] | Flash Duration Typ   | Current During View Finder/Focusing | Current During FLASH             |
|-----------|----------------------|-------------------------------------|----------------------------------|
| 00        | 200ms                | Set by HC[1:0]                      | HC[11] = I <sub>MAX(FLASH)</sub> |
| 01        | 400ms                | Set by HC[1:0]                      | HC[11] = I <sub>MAX(FLASH)</sub> |
| 10        | 600ms                | Set by HC[1:0]                      | HC[11] = I <sub>MAX(FLASH)</sub> |
| 11        | EN_FLASH on duration | Set by HC[1:0]                      | HC[11] = I <sub>MAX(FLASH)</sub> |

Figure 24 shows the functionality of the built-in flash.

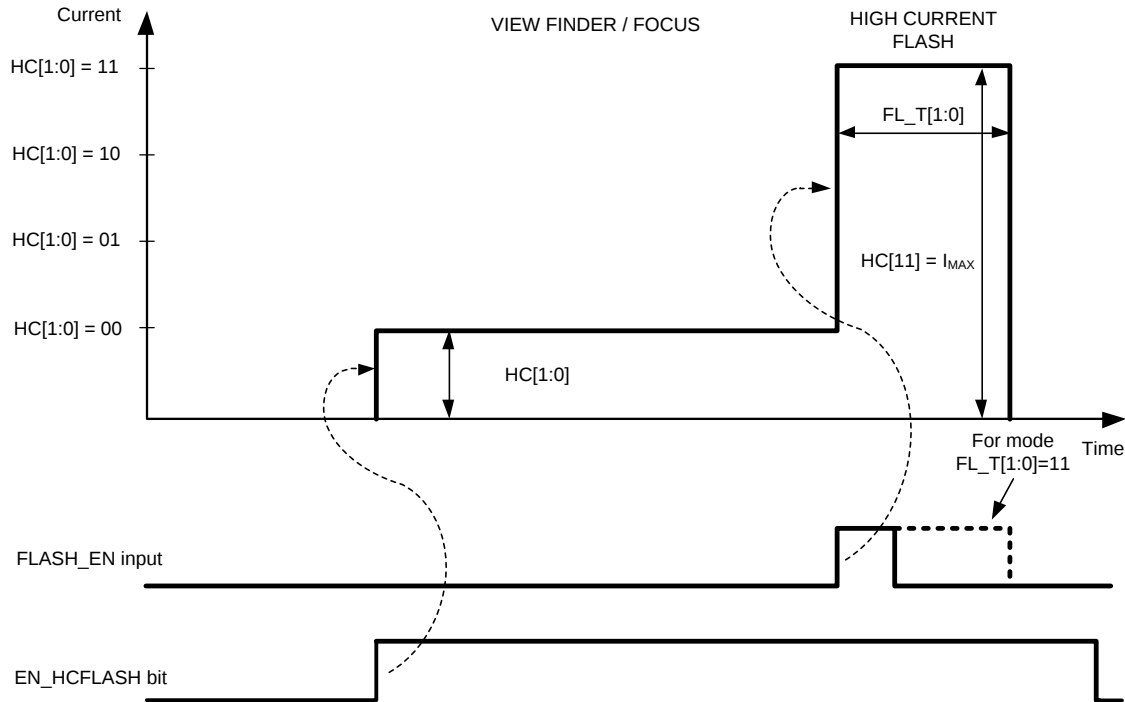


Figure 24. Built-In Flash

**HIGH CURRENT DRIVER ELECTRICAL CHARACTERISTICS**

| Parameter               |                           | Test Conditions                 | Min | Typ   | Max | Unit |
|-------------------------|---------------------------|---------------------------------|-----|-------|-----|------|
| I <sub>LEAKAGE</sub>    | FLASH pin leakage current |                                 |     | 0.1   | 2   | μA   |
| I <sub>MAX(FLASH)</sub> | Maximum Sink Current      |                                 |     |       | 400 | mA   |
|                         | Accuracy at 300 mA        | R <sub>FLASH</sub> =1.18 kΩ ±1% |     | ±5    | ±10 | %    |
|                         | Current mirror ratio      |                                 |     | 1:300 |     |      |

**Backlight Drivers**

LP3954 has 2 independent backlight drivers. Both drivers are regulated constant current sinks. LED current for both LED banks (WLED1...4 and WLED5...6) are controlled by 8-bit current mode DACs with 0.1 mA step.

WLED1...4 and WLED5...6 can be also controlled with one DAC for better matching allowing the use of larger displays having up to 6 white LEDs in parallel.

Display configuration is controlled with DISPL bit as shown below.

| DISPL | Configuration              | Matching            |
|-------|----------------------------|---------------------|
| 0     | Main display up to 4 LEDs  | Good btw WLED1...4  |
|       | Sub display up to 2 LEDs   | Good btw WLED5...6  |
| 1     | Large display up to 6 LEDs | Good btw WLED 1...6 |

| Display backlight enables |   |                  |
|---------------------------|---|------------------|
| EN_W1-4                   | 1 | WLED1-4 enabled  |
|                           | 0 | WLED1-4 disabled |
| EN_W5-6                   | 1 | WLED5-6 enabled  |
|                           | 0 | WLED5-6 disabled |

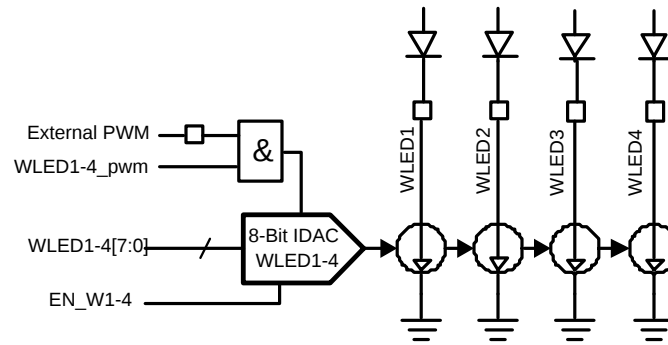


Figure 25. Main Display up to 4 LEDs (WLED1...4)

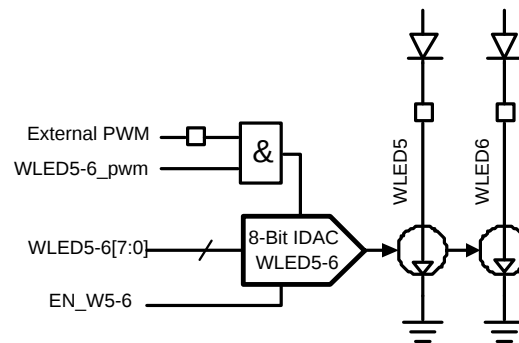


Figure 26. Sub Display Driver up to 2 LEDs (WLED5...6)

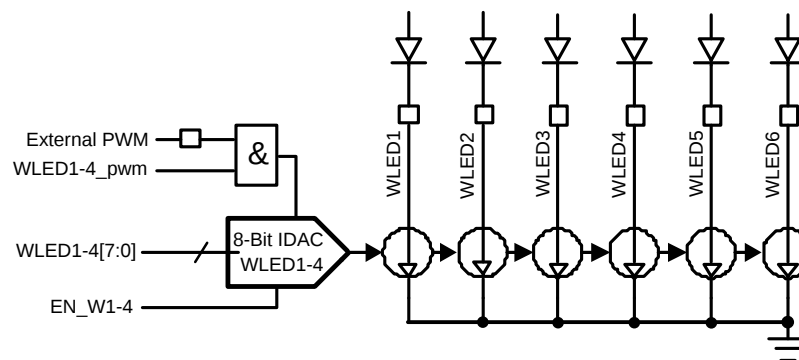


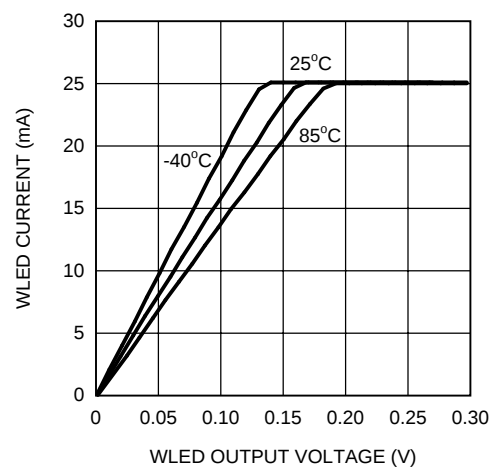
Figure 27. Main Display up to 6 LEDs (WLED1...6) (DISPL=1)

## BACKLIGHT DRIVER ELECTRICAL CHARACTERISTICS

| Parameter      | Test Conditions         | Min                                 | Typical | Max   | Unit    |
|----------------|-------------------------|-------------------------------------|---------|-------|---------|
| $I_{MAX}$      | Maximum Sink Current    | 21.3                                | 25.5    | 29.4  | mA      |
| $I_{Leakage}$  | Leakage Current         |                                     | 0.03    | 1     | $\mu$ A |
| $I_{WLED1}$    | WLED1 Current tolerance | $I_{WLED1}$ set to 12.8mA (80H)     |         |       |         |
|                |                         | 10.52                               | 12.8    | 14.78 | mA      |
|                |                         | -18                                 |         | +16   | %       |
| $I_{Match1-4}$ | Sink Current Matching   | $I_{SINK}=13$ mA, Between WLED1...4 |         | 0.2   | %       |
| $I_{Match5-6}$ | Sink Current Matching   | $I_{SINK}=13$ mA, Between WLED5...6 |         | 0.2   | %       |
| $I_{Match1-6}$ | Sink Current Matching   | $I_{SINK}=13$ mA, Between WLED1...6 |         | 0.3   | %       |

## ADJUSTMENT

| WLED1-4[7:0]<br>WLED5-6[7:0] | Driver Current,<br>mA (typical) |
|------------------------------|---------------------------------|
| 0000 0000                    | 0                               |
| 0000 0001                    | 0.1                             |
| 0000 0010                    | 0.2                             |
| 0000 0011                    | 0.3                             |
| ...                          | ...                             |
| ...                          | ...                             |
| 1111 1101                    | 25.3                            |
| 1111 1110                    | 25.4                            |
| 1111 1111                    | 25.5                            |



**Figure 28. WLED Output Current vs. Voltage**

## FADE IN / FADE OUT

LP3954 has an automatic fade in and out for main and sub backlight. The fade function is enabled with EN\_FADE bit. The slope of the fade curve is set by the SLOPE bit. Fade control for main and sub display is set by FADE\_SEL bit.

|          |   |                           |
|----------|---|---------------------------|
| EN_FADE  | 0 | Automatic fade disabled   |
|          | 1 | Automatic fade enabled    |
| SLOPE    | 0 | Fade execution time 1.3s  |
|          | 1 | Fade execution time 0.65s |
| FADE_SEL | 0 | Fade controls WLED1-4     |
|          | 1 | Fade controls WLED5-6     |

Recommended fading sequence:

1. ASSUMPTION: Current WLED value in register
2. Set SLOPE
3. Set FADE\_SEL
4. Set EN\_FADE = 1
5. Set target WLED value
6. Fading will be done either within 0.5s or 1s based on Slope selection

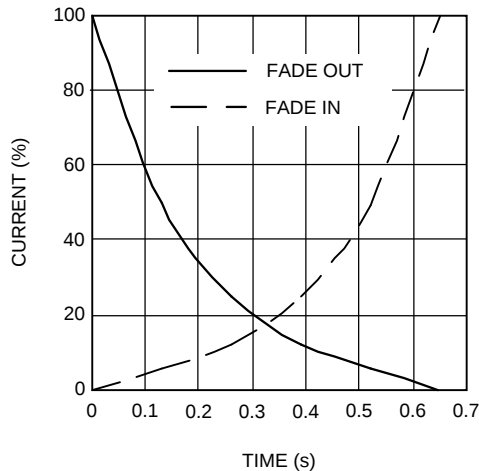


Figure 29. WLED Dimming, SLOPE=0

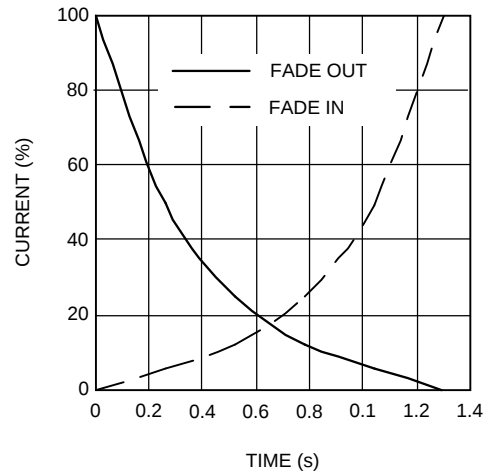


Figure 30. WLED Dimming, SLOPE=1

### Ambient Light and Temperature Measurement with LP3954

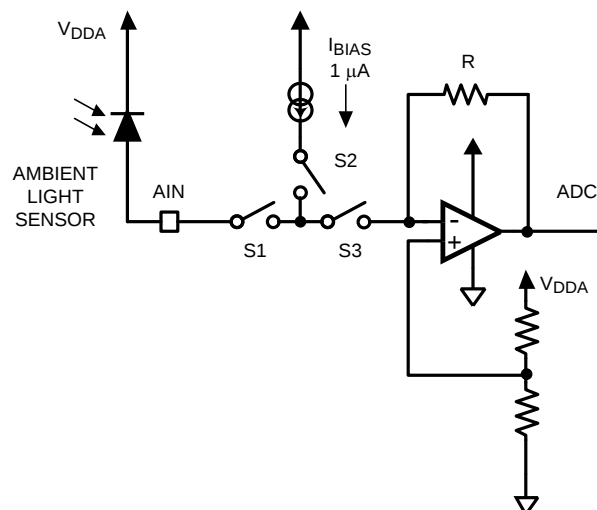
The Analog-to-Digital converter (ADC) in the Audio Synchronization block can be also used for ambient light measurement or temperature measurement.

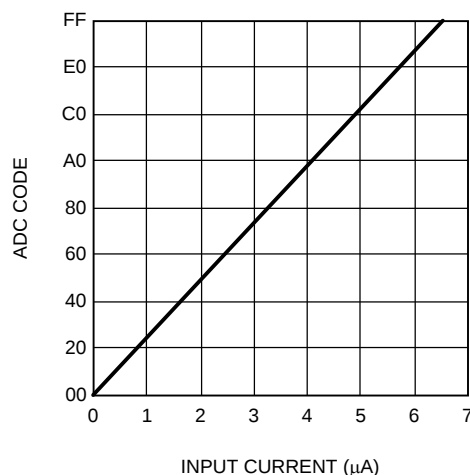
The selection between these modes is controlled with input selector bits INPUT\_SEL[1:0] as follows

| INPUT_SEL[1:0] | Mode                                      |
|----------------|-------------------------------------------|
| 00             | Audio synchronization                     |
| 01             | Temperature measurement (voltage input)   |
| 10             | Ambient light measurement (current input) |
| 11             | No input                                  |

### AMBIENT LIGHT MEASUREMENT

The ambient light measurement requires only one external component: Ambient light sensor (photo transistor or diode). The ADC reads the current level at ASE pin and converts the result in digital word. User can read the ADC output from the ADC output register. The known ambient light condition allows user to set the backlight current to optimal level thus saving power especially in low light and bright sunlight condition.

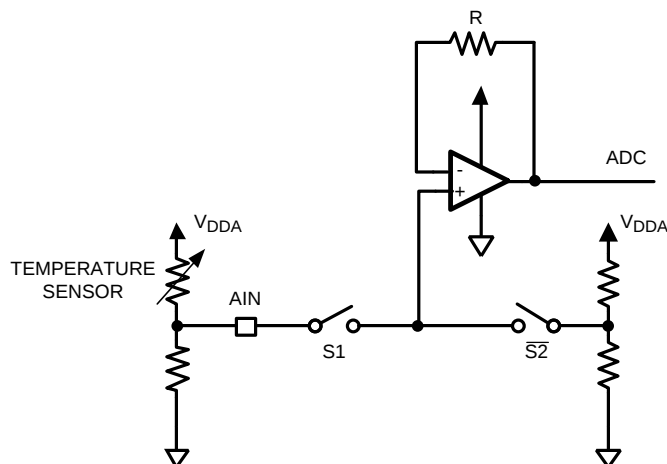




**Figure 31. ADC Code vs Input Current in Light Measurement Mode**

### TEMPERATURE MEASUREMENT

The temperature measurement requires two external components: resistor and thermistor (resistor that has known temperature vs resistance curve). The ADC reads the voltage level at ASE pin and converts the result in digital word. User can read the ADC output from register. The known temperature allows for example to monitor the temperature inside the display module and decrease the current level of the LEDs if temperature raises too high. This function may increase lifetime of LEDs in some applications.



**Figure 32. Temperature Sensor Connection Example**

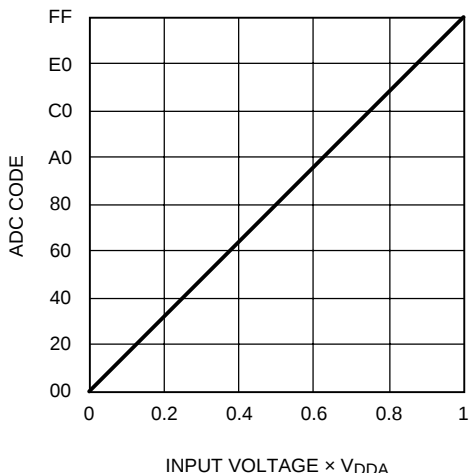


Figure 33. ADC Code vs Input Voltage in Temperature Measurement Mode

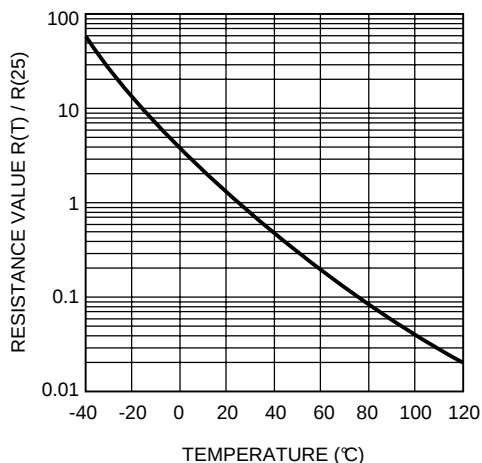


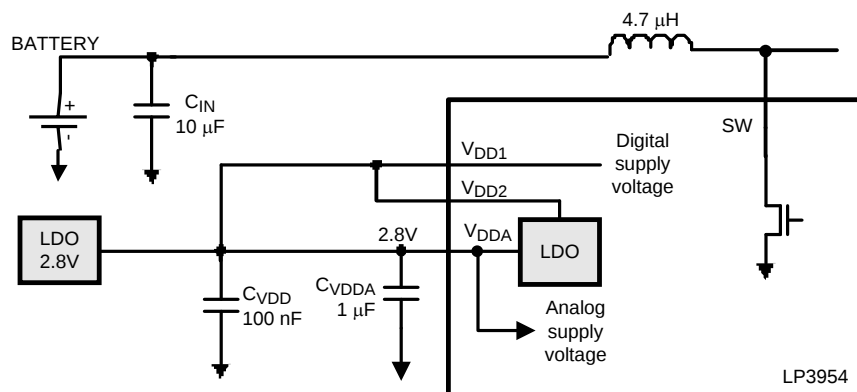
Figure 34. Example Curve for Thermistor

#### EXAMPLE TEMP SENSOR READING AT DIFFERENT TEMPERATURES ( $R(25^{\circ}\text{C})=1\text{M}\Omega$ )

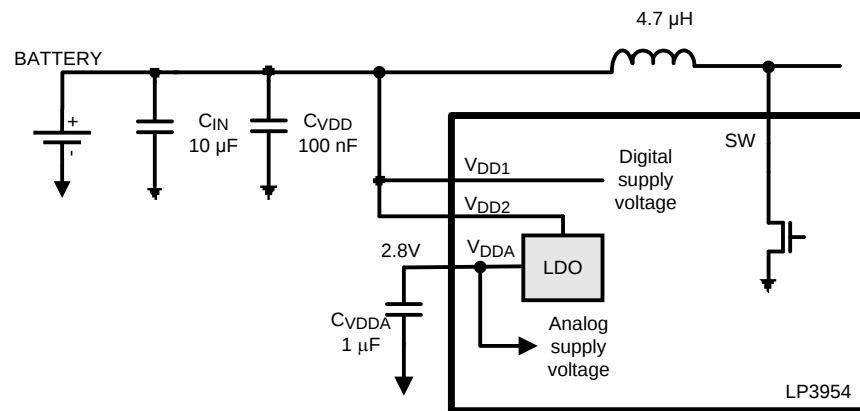
| T°C | R(M $\Omega$ ) | Rt(M $\Omega$ ) | V(ASE)    |
|-----|----------------|-----------------|-----------|
| -40 | 1              | 60              | 2.7540984 |
| 0   | 1              | 4               | 2.24      |
| 25  | 1              | 1               | 1.4       |
| 60  | 1              | 0.2             | 0.4666667 |
| 100 | 1              | 0.04            | 0.1076923 |

#### 7V Shielding

To shield LP3954 from high input voltages 6...7.2V the use of external 2.8V LDO is required. This 2.8V voltage protects internally the device against high voltage condition. The recommended connection is as shown in the picture below. Internally both logic and analog circuitry works at 2.8V supply voltage. Both supply voltage pins should have separate filtering capacitors.



In cases where high voltage is not an issue the connection is as shown below.



## Logic Interface Characteristics

( $1.65\text{V} \leq V_{\text{DDIO}} \leq V_{\text{DD1,2}}\text{V}$ ) (Unless otherwise noted)

| Parameter                                                |                        | Test Conditions                                             | Min                     | Typ                     | Max                     | Unit |
|----------------------------------------------------------|------------------------|-------------------------------------------------------------|-------------------------|-------------------------|-------------------------|------|
| LOGIC INPUTS SS, SI, SCK/SCL, SYNC/PWM, IF_SEL, EN_FLASH |                        |                                                             |                         |                         |                         |      |
| V <sub>IL</sub>                                          | Input Low Level        |                                                             |                         |                         | 0.2 × V <sub>DDIO</sub> | V    |
| V <sub>IH</sub>                                          | Input High Level       |                                                             | 0.8 × V <sub>DDIO</sub> |                         |                         | V    |
| I <sub>I</sub>                                           | Logic Input Current    |                                                             | −1.0                    |                         | 1.0                     | μA   |
| f <sub>SCL</sub>                                         | Clock Frequency        | I <sup>2</sup> C Mode                                       |                         |                         | 400                     | kHz  |
|                                                          |                        | SPI Mode, V <sub>DDIO</sub> > 1.8V                          |                         |                         | 13                      | MHz  |
|                                                          |                        | SPI Mode, 1.65V ≤ V <sub>DDIO</sub> < 1.8V                  |                         |                         | 5                       | MHz  |
| LOGIC OUTPUT SO                                          |                        |                                                             |                         |                         |                         |      |
| V <sub>OL</sub>                                          | Output Low Level       | I <sub>SO</sub> = 3 mA<br>V <sub>DDIO</sub> > 1.8V          |                         | 0.3                     | 0.5                     | V    |
|                                                          |                        | I <sub>SO</sub> = 2 mA<br>1.65V ≤ V <sub>DDIO</sub> < 1.8V  |                         | 0.3                     | 0.5                     |      |
| V <sub>OH</sub>                                          | Output High Level      | I <sub>SO</sub> = −3 mA<br>V <sub>DDIO</sub> > 1.8V         | V <sub>DDIO</sub> − 0.5 | V <sub>DDIO</sub> − 0.3 |                         | V    |
|                                                          |                        | I <sub>SO</sub> = −2 mA<br>1.65V ≤ V <sub>DDIO</sub> < 1.8V | V <sub>DDIO</sub> − 0.5 | V <sub>DDIO</sub> − 0.3 |                         |      |
| I <sub>L</sub>                                           | Output Leakage Current | V <sub>SO</sub> = 2.8V                                      |                         |                         | 1.0                     | μA   |
| LOGIC OUTPUT SDA                                         |                        |                                                             |                         |                         |                         |      |
| V <sub>OL</sub>                                          | Output Low Level       | I <sub>SDA</sub> = 3 mA                                     |                         | 0.3                     | 0.5                     | V    |

## Control Interface

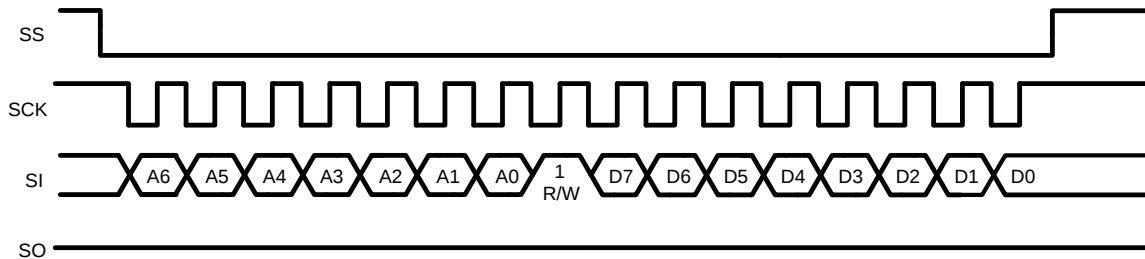
The LP3954 supports two different interface modes:

- SPI interface (4 wire, serial)
- I<sup>2</sup>C compatible interface (2 wire, serial)

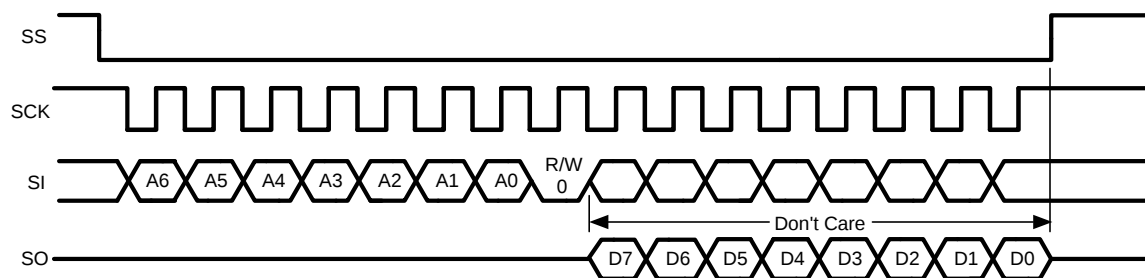
User can define the serial interface by IF\_SEL pin. IF\_SEL=0 selects the I<sup>2</sup>C mode.

## SPI INTERFACE

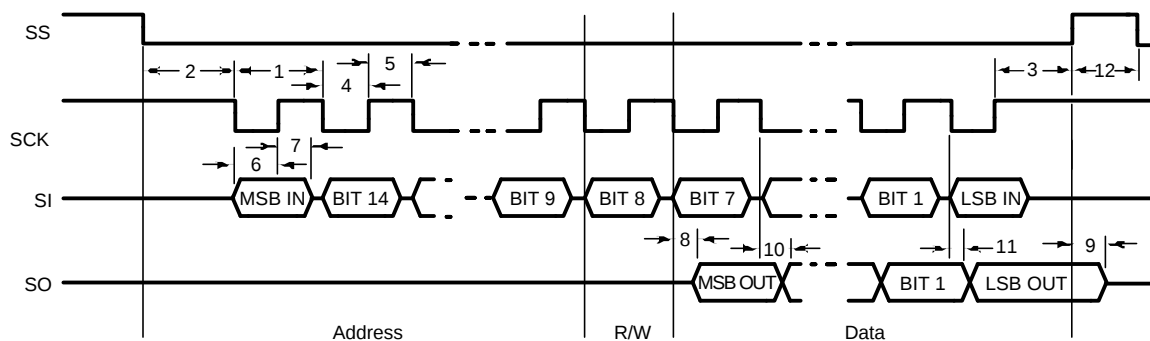
LP3954 is compatible with SPI serial bus specification and it operates as a slave. The transmission consists of 16-bit Write and Read Cycles. One cycle consists of 7 Address bits, 1 Read/Write (RW) bit and 8 Data bits. RW bit high state defines a Write Cycle and low defines a Read Cycle. SO output is normally in high-impedance state and it is active only when Data is sent out during a Read Cycle. A pull-up resistor may be needed in SO line if a floating logic signal can cause unintended current consumption in the input circuits where SO is connected. The Address and Data are transmitted MSB first. The Slave Select signal SS must be low during the Cycle transmission. SS resets the interface when high and it has to be taken high between successive Cycles. Data is clocked in on the rising edge of the SCK clock signal, while data is clocked out on the falling edge of SCK.



**Figure 35. SPI Write Cycle**



**Figure 36. SPI Read Cycle**



**Figure 37. SPI Timing Diagram**

### SPI Timing Parameters

$$V_{DD} = V_{DD\_IO} = 2.775V$$

| Symbol | Parameter        | Limit <sup>(1)</sup> |     | Unit |
|--------|------------------|----------------------|-----|------|
|        |                  | Min                  | Max |      |
| 1      | Cycle Time       | 70                   |     | ns   |
| 2      | Enable Lead Time | 35                   |     | ns   |

(1) **Note:** Data ensured by design.

| Symbol | Parameter        | Limit <sup>(1)</sup> |     | Unit |
|--------|------------------|----------------------|-----|------|
|        |                  | Min                  | Max |      |
| 3      | Enable Lag Time  | 35                   |     | ns   |
| 4      | Clock Low Time   | 35                   |     | ns   |
| 5      | Clock High Time  | 35                   |     | ns   |
| 6      | Data Setup Time  | 20                   |     | ns   |
| 7      | Data Hold Time   | 0                    |     | ns   |
| 8      | Data Access Time |                      | 20  | ns   |
| 9      | Disable Time     |                      | 10  | ns   |
| 10     | Data Valid       |                      | 20  | ns   |
| 11     | Data Hold Time   | 0                    |     | ns   |

## I<sup>2</sup>C COMPATIBLE INTERFACE

### I<sup>2</sup>C Signals

In I<sup>2</sup>C mode the LP3954 pin SCK is used for the I<sup>2</sup>C clock SCL and the pin SS is used for the I<sup>2</sup>C data signal SDA. Both these signals need a pull-up resistor according to I<sup>2</sup>C specification. SI pin is the address select pin. I<sup>2</sup>C address for LP3954 is 54h when SI = 0 and 55h when SI = 1. Unused pin SO can be left unconnected.

### I<sup>2</sup>C Data Validity

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.

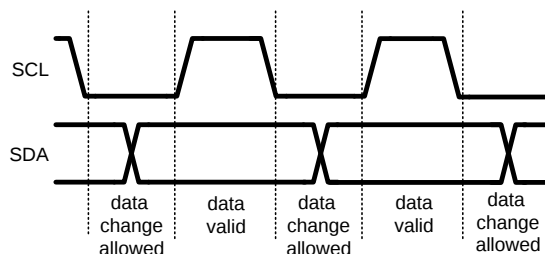
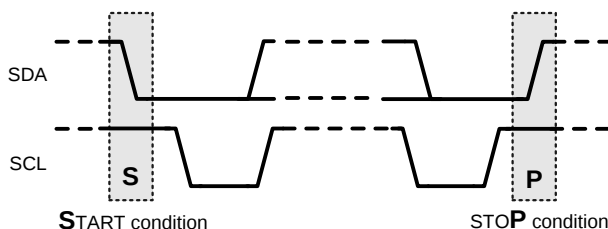


Figure 38. I<sup>2</sup>C Signals: Data Validity

### I<sup>2</sup>C Start and Stop Conditions

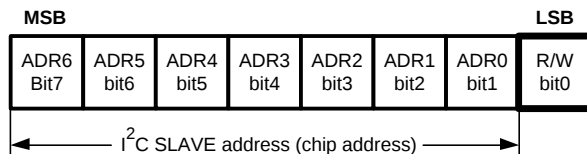
START and STOP bits classify the beginning and the end of the I<sup>2</sup>C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I<sup>2</sup>C master always generates START and STOP bits. The I<sup>2</sup>C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I<sup>2</sup>C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.



## Transferring Data

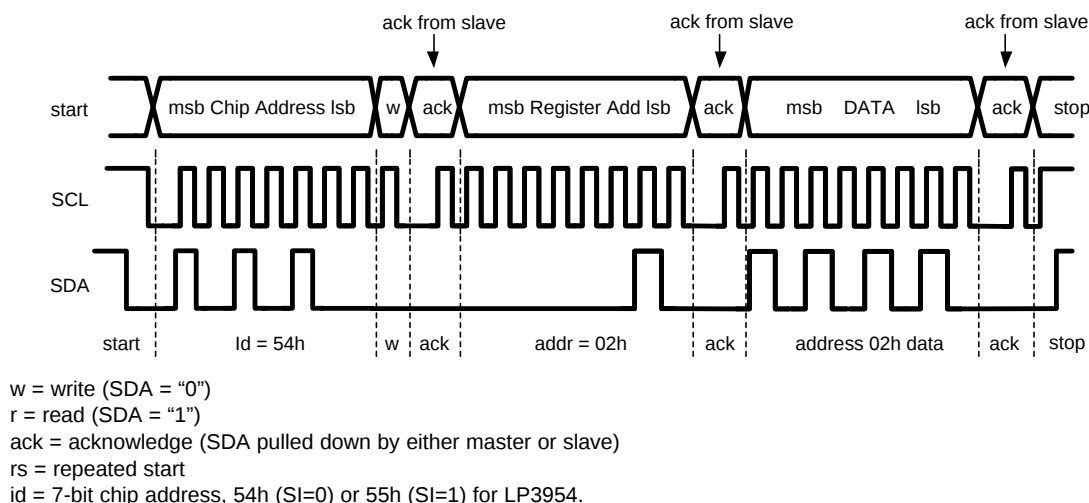
Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9<sup>th</sup> clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, the I<sup>2</sup>C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LP3954 address is 54h or 55h as selected with SI pin. For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.



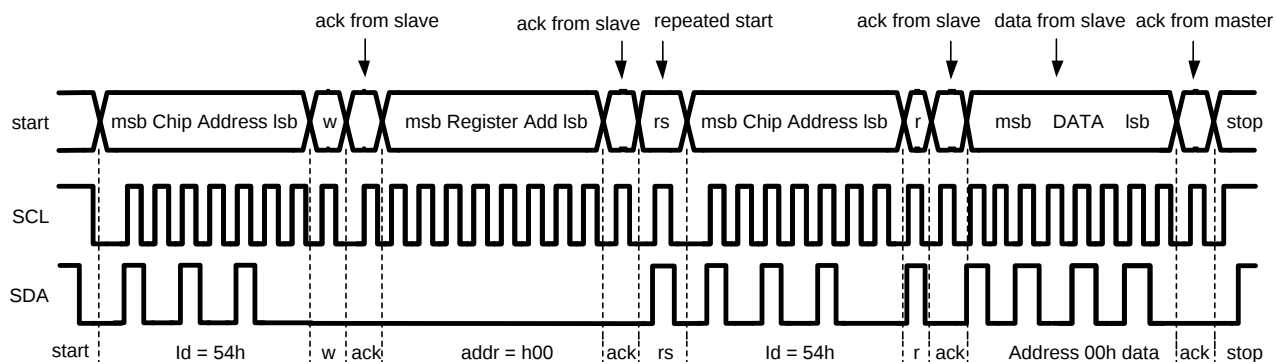
**Figure 39. I<sup>2</sup>C Chip Address**

Register changes take an effect at the SCL rising edge during the last ACK from slave.

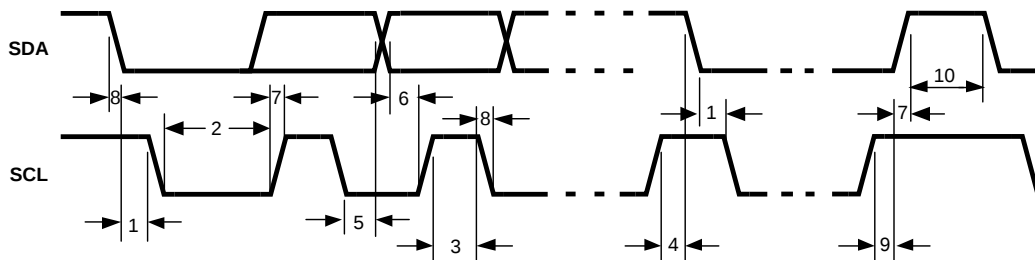


**Figure 40. I<sup>2</sup>C Write Cycle**

When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in the Read Cycle waveform.



**Figure 41. I<sup>2</sup>C Read Cycle**

Figure 42. I<sup>2</sup>C Timing Diagram

**I<sup>2</sup>C Timing Parameters** ( $V_{DD1,2} = 3.0$  to  $4.5V$ ,  $V_{DD\_IO} = 1.65V$  to  $V_{DD1,2}$ )

| Symbol | Parameter                                                       | Limit <sup>(1)</sup> |     | Unit |
|--------|-----------------------------------------------------------------|----------------------|-----|------|
|        |                                                                 | Min                  | Max |      |
| 1      | Hold Time (repeated) START Condition                            | 0.6                  |     | μs   |
| 2      | Clock Low Time                                                  | 1.3                  |     | μs   |
| 3      | Clock High Time                                                 | 600                  |     | ns   |
| 4      | Setup Time for a Repeated START Condition                       | 600                  |     | ns   |
| 5      | Data Hold Time (Output direction, delay generated by LP3954)    | 300                  | 900 | ns   |
| 5      | Data Hold Time (Input direction, delay generated by the Master) | 0                    | 900 | ns   |
| 6      | Data Setup Time                                                 | 100                  |     | ns   |
| 7      | Rise Time of SDA and SCL                                        | $20+0.1C_b$          | 300 | ns   |
| 8      | Fall Time of SDA and SCL                                        | $15+0.1C_b$          | 300 | ns   |
| 9      | Set-up Time for STOP condition                                  | 600                  |     | ns   |
| 10     | Bus Free Time between a STOP and a START Condition              | 1.3                  |     | μs   |
| $C_b$  | Capacitive Load for Each Bus Line                               | 10                   | 200 | pF   |

(1) **NOTE:** Data ensured by design

Autoincrement mode is available, with this possible read or write few byte with autoincreasing addresses, but LP3954 has holes in address register map, and is recommended to use autoincrement mode only for the pattern command registers.

## Recommended External Components

### OUTPUT CAPACITOR, $C_{OUT}$

The output capacitor  $C_{OUT}$  directly affects the magnitude of the output ripple voltage. In general, the higher the value of  $C_{OUT}$ , the lower the output ripple magnitude. Multilayer ceramic capacitors with low ESR are the best choice. At the lighter loads, the low ESR ceramics offer a much lower  $V_{out}$  ripple than the higher ESR tantalums of the same value. At the higher loads, the ceramics offer a slightly lower  $V_{out}$  ripple magnitude than the tantalums of the same value. However, the  $dv/dt$  of the  $V_{out}$  ripple with the ceramics is much lower than the tantalums under all load conditions. Capacitor voltage rating must be sufficient, 10V or greater is recommended.

**Some ceramic capacitors, especially those in small packages, exhibit a strong capacitance reduction with the increased applied voltage. The capacitance value can fall to below half of the nominal capacitance. Too low output capacitance will increase the noise and it can make the boost converter unstable.**

### INPUT CAPACITOR, $C_{IN}$

The input capacitor  $C_{IN}$  directly affects the magnitude of the input ripple voltage and to a lesser degree the  $V_{OUT}$  ripple. A higher value  $C_{IN}$  will give a lower  $V_{IN}$  ripple. Capacitor voltage rating must be sufficient, 10V or greater is recommended.

## OUTPUT DIODE, $D_{OUT}$

A Schottky diode should be used for the output diode. To maintain high efficiency the average current rating of the schottky diode should be larger than the peak inductor current (1A). Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency in portable applications. Choose a reverse breakdown of the schottky diode larger than the output voltage. Do not use ordinary rectifier diodes, since slow switching speeds and long recovery times cause the efficiency and the load regulation to suffer.

## INDUCTOR, $L_1$

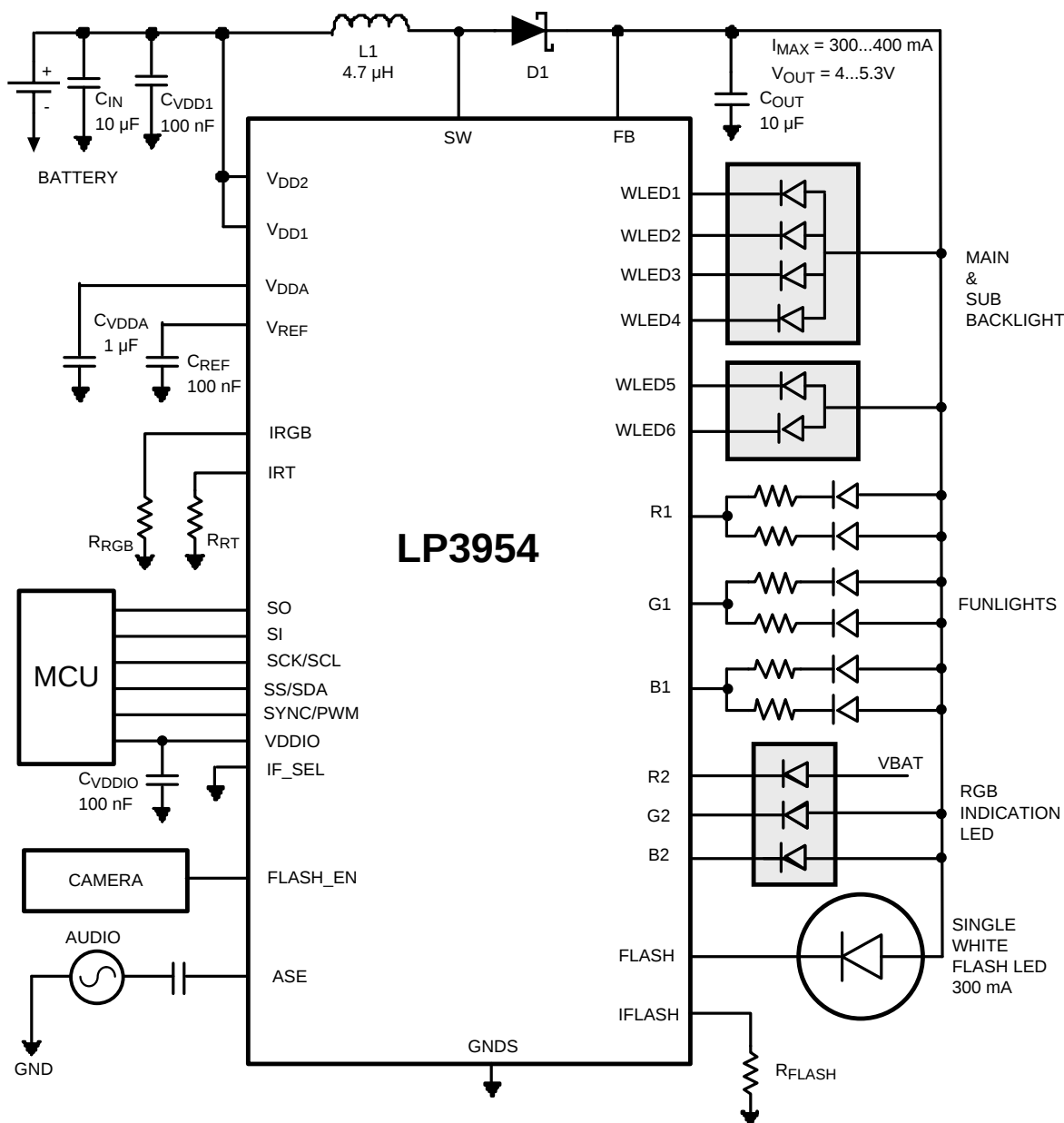
The LP3954's high switching frequency enables the use of the small surface mount inductor. A 4.7  $\mu$ H shielded inductor is suggested for 2 MHz operation, 10  $\mu$ H should be used at 1 MHz. The inductor should have a saturation current rating higher than the peak current it will experience during circuit operation (**1A**). Less than 300 m $\Omega$  ESR is suggested for high efficiency. Open core inductors cause flux linkage with circuit components and interfere with the normal operation of the circuit. This should be avoided. For high efficiency, choose an inductor with a high frequency core material such as ferrite to reduce the core losses. To minimize radiated noise, use a toroid, pot core or shielded core inductor. The inductor should be connected to the SW pin as close to the IC as possible.

## LIST OF RECOMMENDED EXTERNAL COMPONENTS

| Symbol      | Symbol Explanation                   | Value        | Unit       | Type                       |
|-------------|--------------------------------------|--------------|------------|----------------------------|
| $C_{VDD1}$  | C between VDD1 and GND               | 100          | nF         | Ceramic, X7R / X5R         |
| $C_{VDD2}$  | C between VDD2 and GND               | 100          | nF         | Ceramic, X7R / X5R         |
| $C_{VDDIO}$ | C between VDDIO and GND              | 100          | nF         | Ceramic, X7R / X5R         |
| $C_{VDDA}$  | C between VDDA and GND               | 1            | $\mu$ F    | Ceramic, X7R / X5R         |
| $C_{OUT}$   | C between FB and GND                 | 10           | $\mu$ F    | Ceramic, X7R / X5R, 10V    |
| $C_{IN}$    | C between battery voltage and GND    | 10           | $\mu$ F    | Ceramic, X7R / X5R         |
| $L_{BOOST}$ | L between SW and $V_{BAT}$ at 2 MHz  | 4.7          | $\mu$ H    | Shielded, low ESR, Isat 1A |
| $C_{VREF}$  | C between $V_{REF}$ and GND          | 100          | nF         | Ceramic, X7R               |
| $C_{VDDIO}$ | C between $V_{DDIO}$ and GND         | 100          | nF         | Ceramic, X7R               |
| $R_{FLASH}$ | R between $I_{FLASH}$ and GND        | 1.2          | k $\Omega$ | $\pm 1\%$                  |
| $R_{RBG}$   | R between $I_{RGB}$ and GND          | 5.6          | k $\Omega$ | $\pm 1\%$                  |
| $R_{RT}$    | R between $I_{RT}$ and GND           | 82           | k $\Omega$ | $\pm 1\%$                  |
| $D_{OUT}$   | Rectifying Diode ( $V_f$ at maxload) | 0.3          | V          | Schottky diode             |
| $C_{ASE}$   | C between Audio input and ASE        | 100          | nF         | Ceramic, X7R / X5R         |
| LEDs        |                                      | User defined |            |                            |
| $D_{LIGHT}$ | Light Sensor                         | TDK BSC2015  |            |                            |

## Application Examples

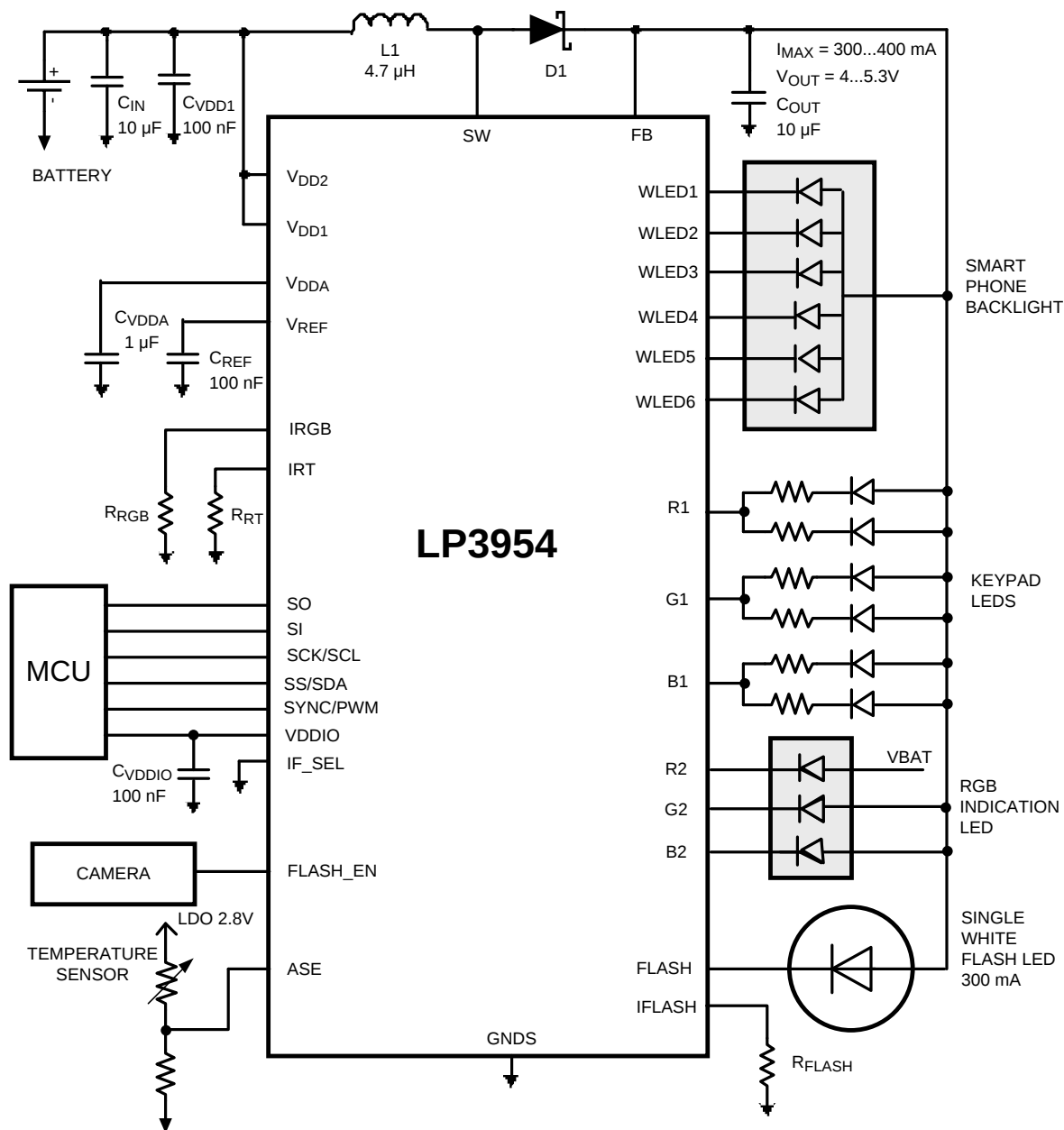
### EXAMPLE 1



- MAIN BACKLIGHT
- SUB BACKLIGHT
- AUDIO SYNCHRONIZED FUNLIGHTS
- RGB INDICATION LIGHT
- FLASH LED

**Figure 43. Flip Phone**

## EXAMPLE 2



- 6 WHITE LED BACKLIGHT
- KEY PAD LIGHTS
- RGB INDICATION LED
- WHITE SINGLE LED FLASH
- TEMPERATURE SENSOR

Figure 44. Smart Phone

### EXAMPLE 3

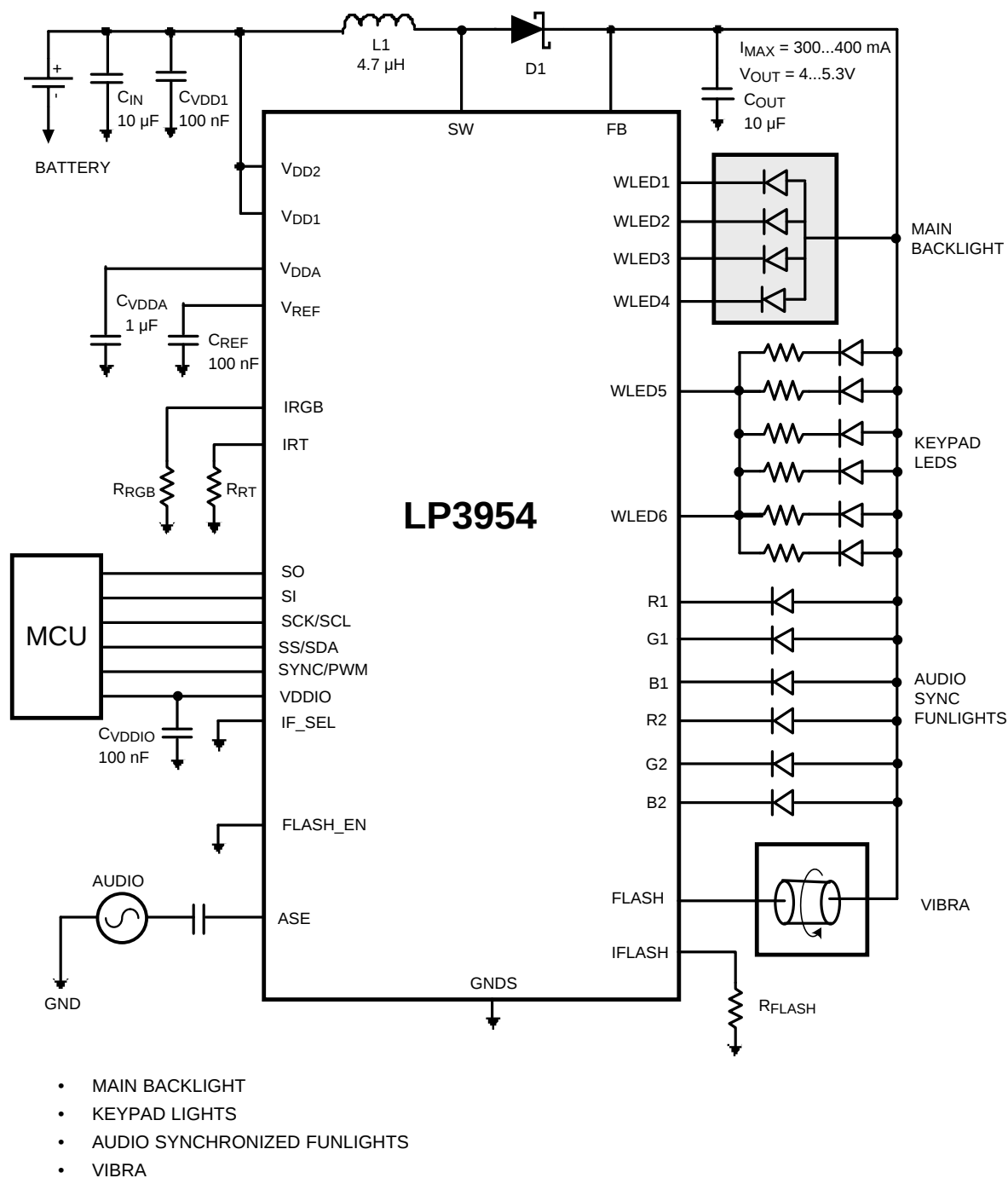
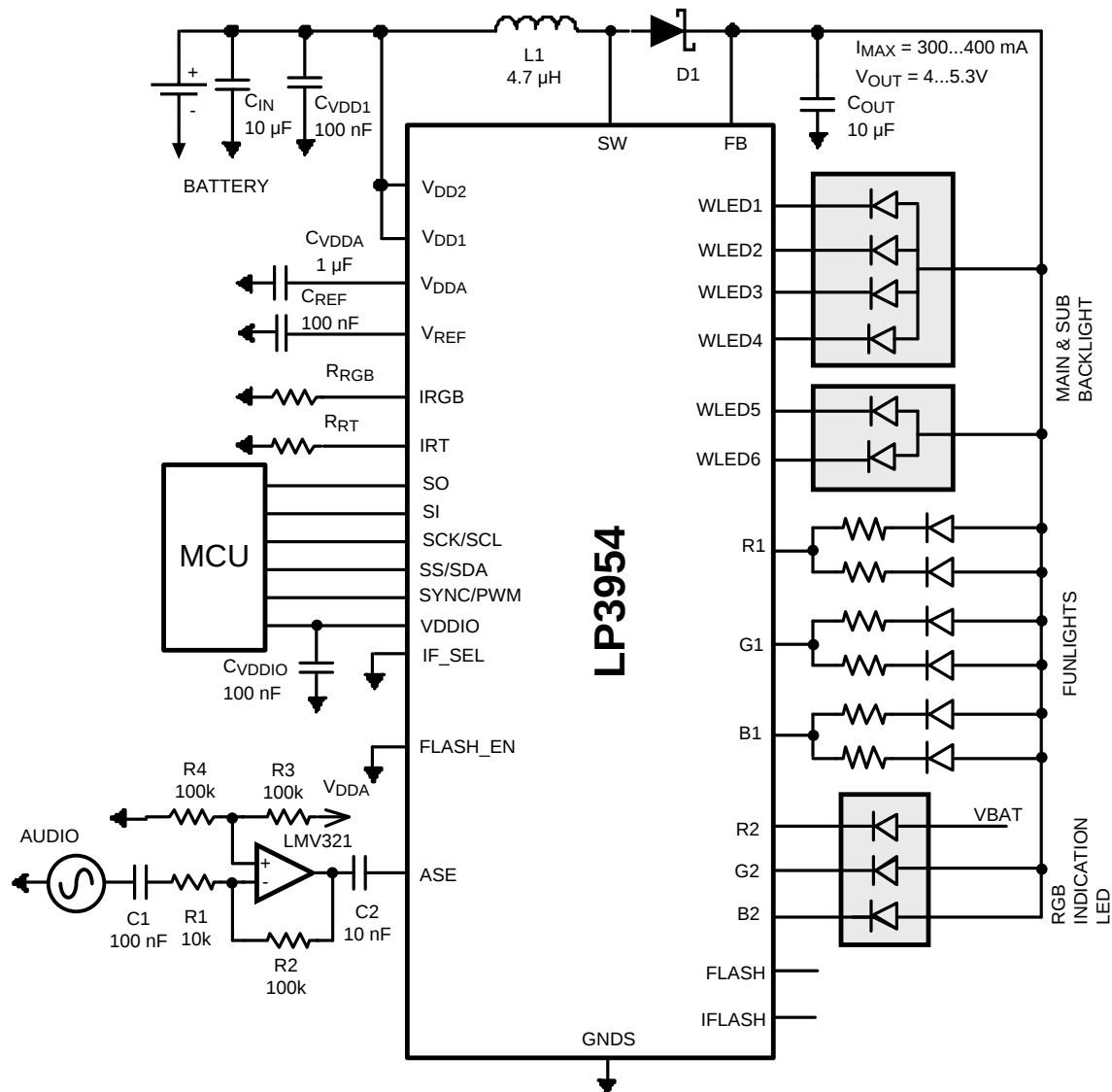


Figure 45. Candybar Phone

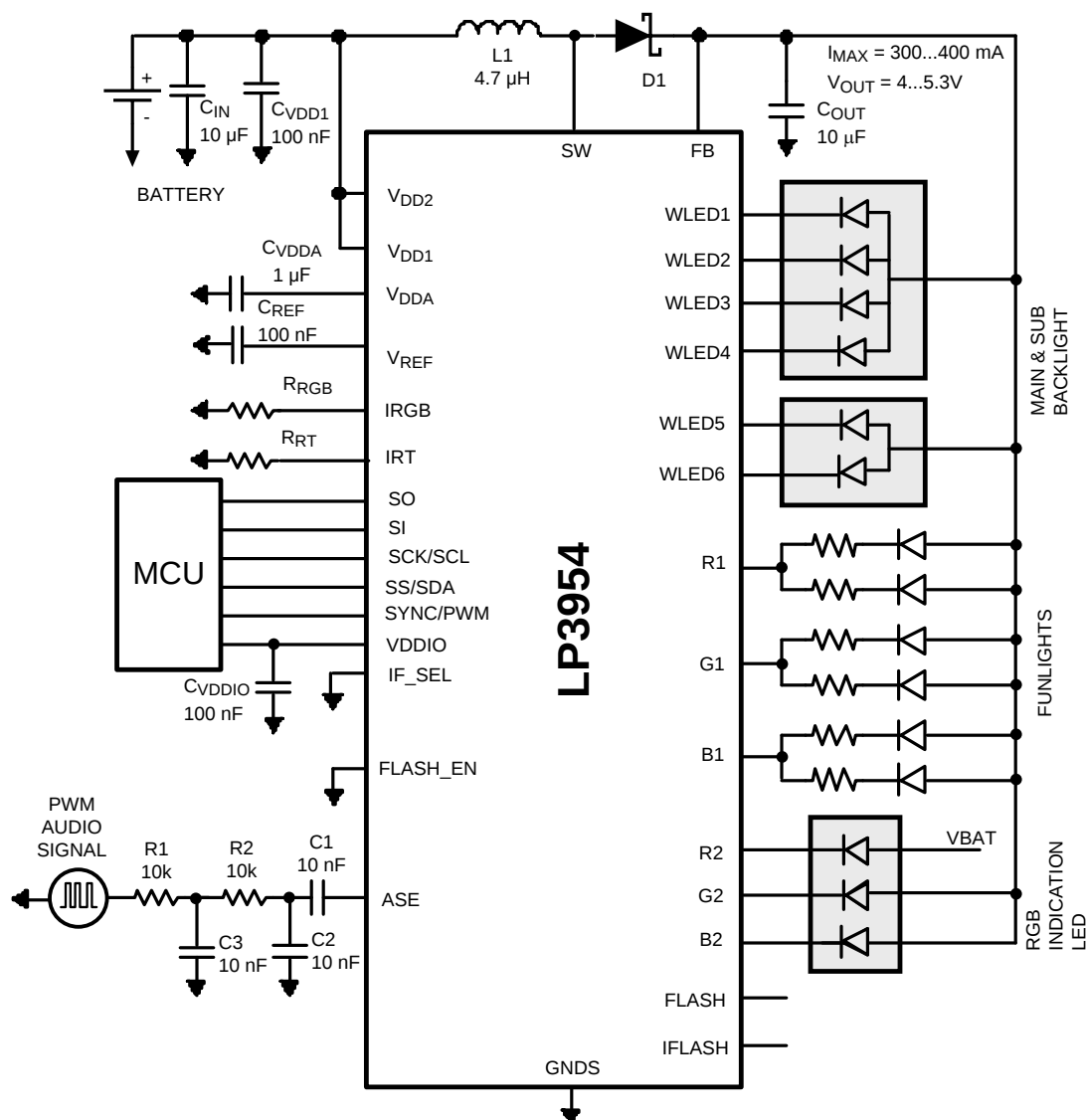
## EXAMPLE 4



- MAIN BACKLIGHT
- SUB BACKLIGHT
- AUDIO SYNCHRONIZED FUNLIGHTS
- RGB INDICATION LIGHT

There may be cases where the audio input signal going into the LP3954 is too weak for audio synchronization. This figure presents a single-supply inverting amplifier connected to the ASE input for audio signal amplification. The amplification is +20 dB, which is well enough for 20 mVp-p audio signal. Because the amplifier (LMV321) is operating in single supply voltage, a voltage divider using R3 and R4 is implemented to bias the amplifier so the input signal is within the input common-mode voltage range of the amplifier. The capacitor C1 is placed between the inverting input and resistor R1 to block the DC signal going into the audio signal source. The values of R1 and C1 affect the cutoff frequency,  $f_c = 1/(2\pi R1 C1)$ , in this case it is around 160 Hz. As a result, the LMV321 output signal is centered around mid-supply, that is  $V_{DDA}/2$ . The output can swing to both rails, maximizing the signal-to-noise ratio in a low voltage system

**Figure 46. Using Extra Amplifier**

**EXAMPLE 5**

- MAIN BACKLIGHT
- SUB BACKLIGHT
- AUDIO SYNCHRONIZED FUNLIGHTS
- RGB INDICATION LIGHT

Here, a second order RC-filter is used on the ASE input to convert a PWM signal to an analog waveform.

**Figure 47. Using PWM Signal**

More application information is available in the document "LP3954 Evaluation Kit".

## LP3954 Control Registers

**Table 3. LP3954 Control Register Names and Default Values**

| ADDR<br>(HEX) | REGISTER         | D7            | D6          | D5       | D4        | D3             | D2            | D1              | D0         |
|---------------|------------------|---------------|-------------|----------|-----------|----------------|---------------|-----------------|------------|
| 00            | RGB Ctrl         | cc_rgb1       | cc_rgb2     | r1sw     | g1sw      | b1sw           | r2sw          | g2sw            | b2sw       |
|               |                  | 1             | 1           | 0        | 0         | 0              | 0             | 0               | 0          |
| 07            | Ext. PWM control | wled1_4_pwm   | wled5_6_pwm | r1_pwm   | g1_pwm    | b1_pwm         | r2_pwm        | g2_pwm          | b2_pwm     |
|               |                  | 0             | 0           | 0        | 0         | 0              | 0             | 0               | 0          |
| 08            | WLED control     |               |             | slope    | fade_sel  | en_fade        | displ         | en_w1_4         | en_w5_6    |
|               |                  |               |             | 0        | 0         | 0              | 0             | 0               | 0          |
| 09            | WLED1-4          | wled1_4[7:0]  |             |          |           |                |               |                 |            |
|               |                  | 0             | 0           | 0        | 0         | 0              | 0             | 0               | 0          |
| 0A            | WLED5-6          | wled5_6[7:0]  |             |          |           |                |               |                 |            |
|               |                  | 0             | 0           | 0        | 0         | 0              | 0             | 0               | 0          |
| 0B            | Enables          | pwm_sync      | nstby       | en_boost |           |                | en_autoload   | rgb_sel[1:0]    |            |
|               |                  | 0             | 0           | 0        |           |                | 1             | 0               | 0          |
| 0C            | ADC output       | data[7:0]     |             |          |           |                |               |                 |            |
|               |                  | 0             | 0           | 0        | 0         | 0              | 0             | 0               | 0          |
| 0D            | Boost output     | boost[7:0]    |             |          |           |                |               |                 |            |
|               |                  | 0             | 0           | 1        | 1         | 1              | 1             | 1               | 1          |
| 0E            | Boost_frq        |               |             |          |           |                | freq_sel[2:0] |                 |            |
|               |                  |               |             |          |           |                | 1             | 1               | 1          |
| 10            | HC_Flash         |               |             | hc_pwm   | fl_t[1:0] |                | hc[1:0]       |                 | en_hcflash |
|               |                  |               |             | 0        | 0         | 0              | 0             | 0               | 0          |
| 11            | Pattern gen ctrl |               |             |          |           |                | rgb_start     | loop            | log        |
|               |                  |               |             |          |           |                | 0             | 0               | 0          |
| 12            | RGB1 max current |               |             | ir1[1:0] |           | ig1[1:0]       |               | ib1[1:0]        |            |
|               |                  |               |             | 0        | 0         | 0              | 0             | 0               | 0          |
| 13            | RGB2 max current |               |             | ir2[1:0] |           | ig2[1:0]       |               | ib2[1:0]        |            |
|               |                  |               |             | 0        | 0         | 0              | 0             | 0               | 0          |
| 2A            | audio sync CTRL1 | gain_sel[2:0] |             |          | sync_mode | en_agc         | en_sync       | input_sel[1:0]  |            |
|               |                  | 0             | 0           | 0        | 0         | 0              | 0             | 1               | 1          |
| 2B            | audio sync CTRL2 |               |             |          | en_avg    | mode_ctrl[1:0] |               | speed_ctrl[1:0] |            |
|               |                  |               |             |          | 0         | 0              | 0             | 0               | 0          |
| 50            | Command 1A       | r[2:0]        |             | g[2:0]   |           |                | cet[3:2]      |                 |            |
|               |                  | 0             | 0           | 0        | 0         | 0              | 0             | 0               | 0          |
| 51            | Command 1B       | cet[1:0]      |             | b[2:0]   |           |                | tt[2:0]       |                 |            |
|               |                  | 0             | 0           | 0        | 0         | 0              | 0             | 0               | 0          |
| 52            | Command 2A       | r[2:0]        |             | g[2:0]   |           |                | cet[3:2]      |                 |            |
|               |                  | 0             | 0           | 0        | 0         | 0              | 0             | 0               | 0          |
| 53            | Command 2B       | cet[1:0]      |             | b[2:0]   |           |                | tt[2:0]       |                 |            |
|               |                  | 0             | 0           | 0        | 0         | 0              | 0             | 0               | 0          |
| 54            | Command 3A       | r[2:0]        |             | g[2:0]   |           |                | cet[3:2]      |                 |            |
|               |                  | 0             | 0           | 0        | 0         | 0              | 0             | 0               | 0          |
| 55            | Command 3B       | cet[1:0]      |             | b[2:0]   |           |                | tt[2:0]       |                 |            |
|               |                  | 0             | 0           | 0        | 0         | 0              | 0             | 0               | 0          |
| 56            | Command 4A       | r[2:0]        |             | g[2:0]   |           |                | cet[3:2]      |                 |            |
|               |                  | 0             | 0           | 0        | 0         | 0              | 0             | 0               | 0          |
| 57            | Command 4B       | cet[1:0]      |             | b[2:0]   |           |                | tt[2:0]       |                 |            |
|               |                  | 0             | 0           | 0        | 0         | 0              | 0             | 0               | 0          |

**Table 3. LP3954 Control Register Names and Default Values (continued)**

| ADDR<br>(HEX) | REGISTER   | D7                                               | D6 | D5 | D4     | D3 | D2 | D1       | D0 |
|---------------|------------|--------------------------------------------------|----|----|--------|----|----|----------|----|
| 58            | Command 5A | r[2:0]                                           |    |    | g[2:0] |    |    | cet[3:2] |    |
|               |            | 0                                                | 0  | 0  | 0      | 0  | 0  | 0        | 0  |
| 59            | Command 5B | cet[1:0]                                         |    |    | b[2:0] |    |    | tt[2:0]  |    |
|               |            | 0                                                | 0  | 0  | 0      | 0  | 0  | 0        | 0  |
| 5A            | Command 6A | r[2:0]                                           |    |    | g[2:0] |    |    | cet[3:2] |    |
|               |            | 0                                                | 0  | 0  | 0      | 0  | 0  | 0        | 0  |
| 5B            | Command 6B | cet[1:0]                                         |    |    | b[2:0] |    |    | tt[2:0]  |    |
|               |            | 0                                                | 0  | 0  | 0      | 0  | 0  | 0        | 0  |
| 5C            | Command 7A | r[2:0]                                           |    |    | g[2:0] |    |    | cet[3:2] |    |
|               |            | 0                                                | 0  | 0  | 0      | 0  | 0  | 0        | 0  |
| 5D            | Command 7B | cet[1:0]                                         |    |    | b[2:0] |    |    | tt[2:0]  |    |
|               |            | 0                                                | 0  | 0  | 0      | 0  | 0  | 0        | 0  |
| 5E            | Command 8A | r[2:0]                                           |    |    | g[2:0] |    |    | cet[3:2] |    |
|               |            | 0                                                | 0  | 0  | 0      | 0  | 0  | 0        | 0  |
| 5F            | Command 8B | cet[1:0]                                         |    |    | b[2:0] |    |    | tt[2:0]  |    |
|               |            | 0                                                | 0  | 0  | 0      | 0  | 0  | 0        | 0  |
| 60            | Reset      | Writing any data to Reset Register resets LP3954 |    |    |        |    |    |          |    |

## LP3954 Registers

### REGISTER BIT EXPLANATIONS

Each register is shown with a key indicating the accessibility of the each individual bit, and the initial condition:

| Register Bit Accessibility and Initial Condition |                     |
|--------------------------------------------------|---------------------|
| Key                                              | Bit Accessibility   |
| rw                                               | Read/write          |
| r                                                | Read only           |
| –0,–1                                            | Condition after POR |

### RGB CTRL (00H) – RGB LEDS CONTROL REGISTER

| D7      | D6      | D5   | D4   | D3   | D2   | D1   | D0   |
|---------|---------|------|------|------|------|------|------|
| cc_rgb1 | cc_rgb2 | r1sw | g1sw | b1sw | r2sw | g2sw | b2sw |
| rw-1    | rw-1    | rw-0 | rw-0 | rw-0 | rw-0 | rw-0 | rw-0 |

|         |       |                                                                                                                                                          |
|---------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| cc_rgb1 | Bit 7 | 0 – R1, G1 and B1 are constant current sinks, current limited internally<br>1 – R1, G1 and B1 are switches, limit current with external ballast resistor |
| cc_rgb2 | Bit 6 | 0 – R2, G2 and B2 are constant current sinks, current limited internally<br>1 – R2, G2 and B2 are switches, limit current with external ballast resistor |
| r1sw    | Bit 5 | 0 – R1 disabled<br>1 – R1 enabled                                                                                                                        |
| g1sw    | Bit 4 | 0 – G1 disabled<br>1 – G1 enabled                                                                                                                        |
| b1sw    | Bit 3 | 0 – B1 disabled<br>1 – B1 enabled                                                                                                                        |
| r2sw    | Bit 2 | 0 – R2 disabled<br>1 – R2 enabled                                                                                                                        |
| g2sw    | Bit 1 | 0 – G2 disabled<br>1 – G2 enabled                                                                                                                        |
| b2sw    | Bit 0 | 0 – B2 disabled<br>1 – B2 enabled                                                                                                                        |

**EXT\_PWM\_CONTROL (07H) – EXTERNAL PWM CONTROL REGISTER**

| D7          | D6          | D5     | D4     | D3     | D2     | D1     | D0     |
|-------------|-------------|--------|--------|--------|--------|--------|--------|
| wled1_4_pwm | wled5_6_pwm | r1_pwm | g1_pwm | b1_pwm | r2_pwm | g2_pwm | b2_pwm |
| rw-0        | rw-0        | rw-0   | rw-0   | rw-0   | rw-0   | rw-0   | rw-0   |

|             |       |                                                                                 |
|-------------|-------|---------------------------------------------------------------------------------|
| wled1_4_pwm | Bit 7 | 0 – WLED1...WLED4 PWM control disabled<br>1 – WLED1...WLED4 PWM control enabled |
| wled5_6_pwm | Bit 6 | 0 – WLED5, WLED6 PWM control disabled<br>1 – WLED5, WLED6 PWM control enabled   |
| r1_pwm      | Bit 5 | 0 – R1 PWM control disabled<br>1 – R1 PWM control enabled                       |
| g1_pwm      | Bit 4 | 0 – G1 PWM control disabled<br>1 – G1 PWM control enabled                       |
| b1_pwm      | Bit 3 | 0 – RB PWM control disabled<br>1 – B1 PWM control enabled                       |
| r2_pwm      | Bit 2 | 0 – R2 PWM control disabled<br>1 – R2 PWM control enabled                       |
| g2_pwm      | Bit 1 | 0 – G2 PWM control disabled<br>1 – G2 PWM control enabled                       |
| b2_pwm      | Bit 0 | 0 – B2 PWM control disabled<br>1 – B2 PWM control enabled                       |

**WLED CONTROL (08H) – WLED CONTROL REGISTER**

| D7  | D6  | D5    | D4       | D3      | D2    | D1      | D0      |
|-----|-----|-------|----------|---------|-------|---------|---------|
|     |     | slope | fade_sel | en_fade | displ | en_w1_4 | en_w5_6 |
| r-0 | r-0 | rw-0  | rw-0     | rw-0    | rw-0  | rw-0    | rw-0    |

|          |       |                                                                                                                   |
|----------|-------|-------------------------------------------------------------------------------------------------------------------|
| slope    | Bit 5 | 0 – fade execution time 1.3 sec<br>1 – fade execution time 0.65 sec                                               |
| fade_sel | Bit 4 | 0 – fade control for WLED1... WLED4<br>1 – fade control for WLED5, WLED6                                          |
| en_fade  | Bit 3 | 0 – automatic fade disabled<br>1 – automatic fade enabled                                                         |
| displ    | Bit 2 | 0 – WLED1-4 and WLED5-6 are controlled separately<br>1 – WLED1-4 and WLED5-6 are controlled with WLED1-4 controls |
| en_w1_4  | Bit 1 | 0 – WLED1...WLED4 disabled<br>1 – WLED1...WLED4 enabled                                                           |
| en_w5_6  | Bit 0 | 0 – WLED5,WLED6 disabled<br>1 – WLED5,WLED6 enabled                                                               |

**WLED1-4 (09H) – WLED1...WLED4 BRIGHTNESS CONTROL REGISTER**

| D7           | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
|--------------|------|------|------|------|------|------|------|
| wled1_4[7:0] |      |      |      |      |      |      |      |
| rw-0         | rw-0 | rw-0 | rw-0 | rw-0 | rw-0 | rw-0 | rw-0 |

| wled1_4[7:0] | Bits 7-0 | Adjustment   |                             |
|--------------|----------|--------------|-----------------------------|
|              |          | wled1_4[7:0] | Typical driver current (ma) |
|              |          | 0000 0000    | 0                           |
|              |          | 0000 0001    | 0.1                         |
|              |          | 0000 0010    | 0.2                         |
|              |          | 0000 0011    | 0.3                         |
|              |          | 0000 0100    | 0.4                         |
|              |          | ...          | ...                         |
|              |          | 1111 1101    | 25.3                        |
|              |          | 1111 1110    | 25.4                        |
|              |          | 1111 1111    | 25.5                        |

**WLED5-6 (0AH) – WLED5, WLED6 BRIGHTNESS CONTROL REGISTER**

| D7           | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
|--------------|------|------|------|------|------|------|------|
| wled5_5[7:0] |      |      |      |      |      |      |      |
| rw-0         | rw-0 | rw-0 | rw-0 | rw-0 | rw-0 | rw-0 | rw-0 |

| wled5_6[7:0] | Bits 7-0 | Adjustment   |                             |
|--------------|----------|--------------|-----------------------------|
|              |          | wled5_6[7:0] | Typical driver current (ma) |
|              |          | 0000 0000    | 0                           |
|              |          | 0000 0001    | 0.1                         |
|              |          | 0000 0010    | 0.2                         |
|              |          | 0000 0011    | 0.3                         |
|              |          | 0000 0100    | 0.4                         |
|              |          | ...          | ...                         |
|              |          | 1111 1101    | 25.3                        |
|              |          | 1111 1110    | 25.4                        |
|              |          | 1111 1111    | 25.5                        |

**ENABLES (0BH) – ENABLES REGISTER**

| D7       | D6    | D5       | D4  | D3  | D2          | D1           | D0   |
|----------|-------|----------|-----|-----|-------------|--------------|------|
| pwm_sync | nstby | en_boost |     |     | en_autoload | rgb_sel[1:0] |      |
| rw-0     | rw-0  | rw-0     | r-0 | r-0 | rw-1        | rw-0         | rw-0 |

| pwm_sync     | Bit 7    | 0 – synchronization to external clock disabled<br>1 – synchronization to external clock enabled |  |                         |  |                                |  |
|--------------|----------|-------------------------------------------------------------------------------------------------|--|-------------------------|--|--------------------------------|--|
| nstby        | Bit 6    | 0 – LP3954 standby mode<br>1 – LP3954 active mode                                               |  |                         |  |                                |  |
| en_boost     | Bit 5    | 0 – boost converter disabled<br>1 – boost converter enabled                                     |  |                         |  |                                |  |
| en_autoload  | Bit 2    | 0 – internal boost converter active load off<br>1 – internal boost converter active load on     |  |                         |  |                                |  |
| rgb_sel[1:0] | Bits 1-0 | Color LED control mode selection                                                                |  |                         |  |                                |  |
|              |          | rgb_sel[1:0]                                                                                    |  | Audio sync connected to |  | Pattern generator connected to |  |
|              |          | 00                                                                                              |  | none                    |  | RGB1 & RGB2                    |  |
|              |          | 01                                                                                              |  | RGB1                    |  | RGB2                           |  |
|              |          | 10                                                                                              |  | RGB2                    |  | RGB1                           |  |
|              |          | 11                                                                                              |  | RGB1 & RGB2             |  | none                           |  |

**ADC\_OUTPUT (0CH) – ADC DATA REGISTER**

|                  |     |     |     |     |     |     |     |
|------------------|-----|-----|-----|-----|-----|-----|-----|
| D7               | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
| <b>data[7:0]</b> |     |     |     |     |     |     |     |
| r-0              | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 |

|                  |          |                                                               |
|------------------|----------|---------------------------------------------------------------|
| <b>data[7:0]</b> | Bits 7-0 | Data register ADC (Audio input, light or temperature sensors) |
|------------------|----------|---------------------------------------------------------------|

**BOOST\_OUTPUT (0DH) – BOOST OUTPUT VOLTAGE CONTROL REGISTER**

|                   |      |      |      |      |      |      |      |
|-------------------|------|------|------|------|------|------|------|
| D7                | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
| <b>Boost[7:0]</b> |      |      |      |      |      |      |      |
| rw-0              | rw-0 | rw-1 | rw-1 | rw-1 | rw-1 | rw-1 | rw-1 |

| <b>Boost[7:0]</b> | Bits 7-0 | <b>Adjustment</b> |                                 |
|-------------------|----------|-------------------|---------------------------------|
|                   |          | <b>Boost[7:0]</b> | <b>Typical boost output (V)</b> |
|                   |          | 0000 0000         | 4.00                            |
|                   |          | 0000 0001         | 4.25                            |
|                   |          | 0000 0011         | 4.40                            |
|                   |          | 0000 0111         | 4.55                            |
|                   |          | 0000 1111         | 4.70                            |
|                   |          | 0001 1111         | 4.85                            |
|                   |          | 0011 1111         | 5.00 (default)                  |
|                   |          | 0111 1111         | 5.15                            |
|                   |          | 1111 1111         | 5.30                            |

**BOOST\_FRQ (0EH) – BOOST FREQUENCY CONTROL REGISTER**

|     |     |     |     |     |                      |      |      |
|-----|-----|-----|-----|-----|----------------------|------|------|
| D7  | D6  | D5  | D4  | D3  | D2                   | D1   | D0   |
|     |     |     |     |     | <b>freq_sel[2:0]</b> |      |      |
| r-0 | r-0 | r-0 | r-0 | r-0 | rw-1                 | rw-1 | rw-1 |

| <b>freq_sel[2:0]</b> | Bits 7-0 | <b>Adjustment</b>    |                  |
|----------------------|----------|----------------------|------------------|
|                      |          | <b>freq_sel[2:0]</b> | <b>Frequency</b> |
|                      |          | 1xx                  | 2.00 MHz         |
|                      |          | 01x                  | 1.67 MHz         |
|                      |          | 00x                  | 1.00 MHz         |

**HC\_FLASH (10H) – HIGH CURRENT FLASH DRIVER CONTROL REGISTER**

|     |     |               |                  |      |                |      |                   |
|-----|-----|---------------|------------------|------|----------------|------|-------------------|
| D7  | D6  | D5            | D4               | D3   | D2             | D1   | D0                |
|     |     | <b>hc_pwm</b> | <b>fl_t[1:0]</b> |      | <b>hc[1:0]</b> |      | <b>en_hcflash</b> |
| r-0 | r-0 | rw-0          | rw-0             | rw-0 | rw-0           | rw-0 | rw-0              |

| <b>hc_pwm</b>    | Bit 5    | 0 – PWM for high current flash driver disabled<br>1 – PWM for high current flash driver enabled |                                    |  |  |  |  |
|------------------|----------|-------------------------------------------------------------------------------------------------|------------------------------------|--|--|--|--|
| <b>fl_t[1:0]</b> | Bits 4-3 | <b>Flash duration for high current driver</b>                                                   |                                    |  |  |  |  |
|                  |          | <b>fl_t[1:0]</b>                                                                                | <b>Typical flash duration</b>      |  |  |  |  |
|                  |          | 00                                                                                              | 200 ms                             |  |  |  |  |
|                  |          | 01                                                                                              | 400 ms                             |  |  |  |  |
|                  |          | 10                                                                                              | 600 ms                             |  |  |  |  |
|                  |          | 11                                                                                              | According EN_FLASH pin on duration |  |  |  |  |

| hc[1:0]    | Bits 2-1 | Current control for high current flash driver                                   |                              |
|------------|----------|---------------------------------------------------------------------------------|------------------------------|
|            |          | hc[1:0]                                                                         | current                      |
|            |          | 00                                                                              | $0.25 \times I_{MAX(FLASH)}$ |
|            |          | 01                                                                              | $0.50 \times I_{MAX(FLASH)}$ |
|            |          | 10                                                                              | $0.75 \times I_{MAX(FLASH)}$ |
|            |          | 11                                                                              | $1.00 \times I_{MAX(FLASH)}$ |
| en_hcflash | Bit 0    | 0 – high current flash driver disabled<br>1 – high current flash driver enabled |                              |

**PATTERN\_GEN\_CTRL (11H) – PATTERN GENERATOR CONTROL REGISTER**

| D7  | D6  | D5  | D4  | D3  | D2        | D1   | D0   |
|-----|-----|-----|-----|-----|-----------|------|------|
|     |     |     |     |     | rgb_start | loop | log  |
| r-0 | r-0 | r-0 | r-0 | r-0 | rw-0      | rw-0 | rw-0 |

|           |       |                                                                                                                   |
|-----------|-------|-------------------------------------------------------------------------------------------------------------------|
| rgb_start | Bit 2 | 0 – Pattern generator disabled<br>1 – execution pattern starting from command 1                                   |
| loop      | Bit 1 | 0 – pattern generator loop disabled (single patter)<br>1 – pattern generator loop enabled (execute until stopped) |
| log       | Bit 0 | 0 – color intensity mode 0<br>1 – color intensity mode 1                                                          |

**RGB1\_MAX\_CURRENT (12H) – RGB1 DRIVER INDIVIDUAL MAXIMUM CURRENT CONTROL REGISTER**

| D7  | D6  | D5       | D4   | D3       | D2   | D1       | D0   |
|-----|-----|----------|------|----------|------|----------|------|
|     |     | ir1[1:0] |      | ig1[1:0] |      | ib1[1:0] |      |
| r-0 | r-0 | rw-0     | rw-0 | rw-0     | rw-0 | rw-0     | rw-0 |

| ir1[1:0] | Bits 5-4 | Maximum current for R1 driver |                        |
|----------|----------|-------------------------------|------------------------|
|          |          | ir1[2:0]                      | Maximum output current |
|          |          | 00                            | $0.25 \times I_{MAX}$  |
|          |          | 01                            | $0.50 \times I_{MAX}$  |
|          |          | 10                            | $0.75 \times I_{MAX}$  |
|          |          | 11                            | $1.00 \times I_{MAX}$  |
| ig1[1:0] | Bits 3-2 | Maximum current for G1 driver |                        |
|          |          | ig2[1:0]                      | Maximum output current |
|          |          | 00                            | $0.25 \times I_{MAX}$  |
|          |          | 01                            | $0.50 \times I_{MAX}$  |
|          |          | 10                            | $0.75 \times I_{MAX}$  |
|          |          | 11                            | $1.00 \times I_{MAX}$  |
| ib1[1:0] | Bits 1-0 | Maximum current for B1 driver |                        |
|          |          | ib1[1:0]                      | Maximum output current |
|          |          | 00                            | $0.25 \times I_{MAX}$  |
|          |          | 01                            | $0.50 \times I_{MAX}$  |
|          |          | 10                            | $0.75 \times I_{MAX}$  |
|          |          | 11                            | $1.00 \times I_{MAX}$  |

**RGB2\_MAX\_CURRENT (13H) – RGB2 DRIVER INDIVIDUAL MAXIMUM CURRENT CONTROL REGISTER**

| D7   | D6   | D5       | D4   | D3       | D2   | D1       | D0   |
|------|------|----------|------|----------|------|----------|------|
|      |      | ir2[1:0] |      | ig2[1:0] |      | ib2[1:0] |      |
| rw-0 | rw-0 | rw-0     | rw-0 | rw-0     | rw-0 | rw-0     | rw-0 |

|          |          |                               |                        |
|----------|----------|-------------------------------|------------------------|
| ir2[1:0] | Bits 5-4 | Maximum current for R2 driver |                        |
|          |          | ir2[2:0]                      | Maximum output current |
|          |          | 00                            | 0.25×I <sub>MAX</sub>  |
|          |          | 01                            | 0.50×I <sub>MAX</sub>  |
|          |          | 10                            | 0.75×I <sub>MAX</sub>  |
|          |          | 11                            | 1.00×I <sub>MAX</sub>  |
| ig2[1:0] | Bits 3-2 | Maximum current for G2 driver |                        |
|          |          | ig2[1:0]                      | Maximum output current |
|          |          | 00                            | 0.25×I <sub>MAX</sub>  |
|          |          | 01                            | 0.50×I <sub>MAX</sub>  |
|          |          | 10                            | 0.75×I <sub>MAX</sub>  |
|          |          | 11                            | 1.00×I <sub>MAX</sub>  |
| ib2[1:0] | Bits 1-0 | Maximum current for B2 driver |                        |
|          |          | ib2[1:0]                      | Maximum output current |
|          |          | 00                            | 0.25×I <sub>MAX</sub>  |
|          |          | 01                            | 0.50×I <sub>MAX</sub>  |
|          |          | 10                            | 0.75×I <sub>MAX</sub>  |
|          |          | 11                            | 1.00×I <sub>MAX</sub>  |

**AUDIO\_SYNC\_CTRL1 (2AH) – AUDIO SYNCHRONIZATION AND ADC CONTROL REGISTER 1**

|               |      |      |           |        |         |                |      |
|---------------|------|------|-----------|--------|---------|----------------|------|
| D7            | D6   | D5   | D4        | D3     | D2      | D1             | D0   |
| gain_sel[2:0] |      |      | sync_mode | en_agc | en_sync | input_sel[1:0] |      |
| rw-0          | rw-0 | rw-0 | rw-0      | rw-0   | rw-0    | rw-1           | rw-1 |

|                |          |                                                                           |                                 |
|----------------|----------|---------------------------------------------------------------------------|---------------------------------|
| gain_sel[2:0]  | Bits 7-5 | Input signal gain control                                                 |                                 |
|                |          | gain_sel[2:0]                                                             | gain, db                        |
|                |          | 000                                                                       | 0 (default)                     |
|                |          | 001                                                                       | 3                               |
|                |          | 010                                                                       | 6                               |
|                |          | 011                                                                       | 9                               |
|                |          | 100                                                                       | 12                              |
|                |          | 101                                                                       | 15                              |
|                |          | 110                                                                       | 18                              |
|                |          | 111                                                                       | 21                              |
| sync_mode      | Bit 4    | Input filter mode control<br>0 – Amplitude mode<br>1 – Frequency mode     |                                 |
| en_agc         | Bit 3    | 0 – automatic gain control disabled<br>1 – automatic gain control enabled |                                 |
| en_sync        | Bit 2    | 0 – audio synchronization disabled<br>1 – audio synchronization enabled   |                                 |
| input_sel[1:0] | Bits 1-0 | ADC input selector                                                        |                                 |
|                |          | input_sel[1:0]                                                            | Input                           |
|                |          | 00                                                                        | Single ended input signal (ASE) |
|                |          | 01                                                                        | Temperature measurement         |
|                |          | 10                                                                        | Ambient light measurement       |
|                |          | 11                                                                        | No input (default)              |

**AUDIO\_SYNC\_CTRL2 (2BH) – AUDIO SYNCHRONIZATION AND ADC CONTROL REGISTER 2**

|     |     |     |               |                       |      |                        |      |
|-----|-----|-----|---------------|-----------------------|------|------------------------|------|
| D7  | D6  | D5  | D4            | D3                    | D2   | D1                     | D0   |
|     |     |     | <b>en_avg</b> | <b>mode_ctrl[1:0]</b> |      | <b>speed_ctrl[1:0]</b> |      |
| r-0 | r-0 | r-0 | rw-0          | rw-0                  | rw-0 | rw-0                   | rw-0 |

|                        |          |                                                 |
|------------------------|----------|-------------------------------------------------|
| <b>en_avg</b>          | Bit 4    | 0 – averaging disabled<br>1 – averaging enabled |
| <b>mode_ctrl[1:0]</b>  | Bits 3-2 | Filtering mode control                          |
| <b>speed_ctrl[1:0]</b> | Bits 1-0 | LEDs light response time to audio input         |
|                        |          | <b>speed_ctrl[1:0]</b> <b>Response</b>          |
|                        |          | 00      FASTEST (default)                       |
|                        |          | 01      FAST                                    |
|                        |          | 10      MEDIUM                                  |
|                        |          | 11      SLOW                                    |

**PATTERN CONTROL REGISTERS**

| Command_[1:8]A – Pattern Control Register A |      |      |               |      |      |                 |      |
|---------------------------------------------|------|------|---------------|------|------|-----------------|------|
| D7                                          | D6   | D5   | D4            | D3   | D2   | D1              | D0   |
| <b>r[2:0]</b>                               |      |      | <b>g[2:0]</b> |      |      | <b>cet[3:2]</b> |      |
| rw-0                                        | rw-0 | rw-0 | rw-0          | rw-0 | rw-0 | rw-0            | rw-0 |

| Command_[1:8]B – Pattern Control Register B |      |               |      |      |                |      |      |
|---------------------------------------------|------|---------------|------|------|----------------|------|------|
| D7                                          | D6   | D5            | D4   | D3   | D2             | D1   | D0   |
| <b>cet[1:0]</b>                             |      | <b>b[2:0]</b> |      |      | <b>tt[2:0]</b> |      |      |
| rw-0                                        | rw-0 | rw-0          | rw-0 | rw-0 | rw-0           | rw-0 | rw-0 |

|        |              |                                           |                       |                       |
|--------|--------------|-------------------------------------------|-----------------------|-----------------------|
| r[2:0] | Bits<br>7-5A | Red color intensity                       |                       |                       |
|        |              | r[2:0]                                    | current, %            |                       |
|        |              |                                           | log=0                 | log=1                 |
|        |              | 000                                       | 0×I <sub>MAX</sub>    | 0×I <sub>MAX</sub>    |
|        |              | 001                                       | 7%×I <sub>MAX</sub>   | 1%×I <sub>MAX</sub>   |
|        |              | 010                                       | 14%×I <sub>MAX</sub>  | 2%×I <sub>MAX</sub>   |
|        |              | 011                                       | 21%×I <sub>MAX</sub>  | 4%×I <sub>MAX</sub>   |
|        |              | 100                                       | 32%×I <sub>MAX</sub>  | 10%×I <sub>MAX</sub>  |
|        |              | 101                                       | 46%×I <sub>MAX</sub>  | 21%×I <sub>MAX</sub>  |
|        |              | 110                                       | 71%×I <sub>MAX</sub>  | 46%×I <sub>MAX</sub>  |
|        |              | 111                                       | 100%×I <sub>MAX</sub> | 100%×I <sub>MAX</sub> |
|        |              | * log bit is in pattern_gen_ctrl register |                       |                       |

| g[2:0]                                    | Bits<br>4-2A          | Green color intensity                     |                       |                       |
|-------------------------------------------|-----------------------|-------------------------------------------|-----------------------|-----------------------|
|                                           |                       | g[2:0]                                    | current, %            |                       |
|                                           |                       |                                           | log=0                 | log=1                 |
|                                           |                       | 000                                       | 0×I <sub>MAX</sub>    | 0×I <sub>MAX</sub>    |
|                                           |                       | 001                                       | 7%×I <sub>MAX</sub>   | 1%×I <sub>MAX</sub>   |
|                                           |                       | 010                                       | 14%×I <sub>MAX</sub>  | 2%×I <sub>MAX</sub>   |
|                                           |                       | 011                                       | 21%×I <sub>MAX</sub>  | 4%×I <sub>MAX</sub>   |
|                                           |                       | 100                                       | 32%×I <sub>MAX</sub>  | 10%×I <sub>MAX</sub>  |
|                                           |                       | 101                                       | 46%×I <sub>MAX</sub>  | 21%×I <sub>MAX</sub>  |
|                                           |                       | 110                                       | 71%×I <sub>MAX</sub>  | 46%×I <sub>MAX</sub>  |
| 111                                       | 100%×I <sub>MAX</sub> | 100%×I <sub>MAX</sub>                     |                       |                       |
| * log bit is in pattern_gen_ctrl register |                       |                                           |                       |                       |
| cet[3:0]                                  | Bits<br>1-0A<br>7-6B  | Command execution time                    |                       |                       |
|                                           |                       | cet[3:0]                                  | CET duration, ms      |                       |
|                                           |                       | 0000                                      | 197                   |                       |
|                                           |                       | 0001                                      | 393                   |                       |
|                                           |                       | 0010                                      | 590                   |                       |
|                                           |                       | 0011                                      | 786                   |                       |
|                                           |                       | 0100                                      | 983                   |                       |
|                                           |                       | 0101                                      | 1180                  |                       |
|                                           |                       | 0110                                      | 1376                  |                       |
|                                           |                       | 0111                                      | 1573                  |                       |
|                                           |                       | 1000                                      | 1769                  |                       |
|                                           |                       | 1001                                      | 1966                  |                       |
|                                           |                       | 1010                                      | 2163                  |                       |
|                                           |                       | 1011                                      | 2359                  |                       |
|                                           |                       | 1100                                      | 2556                  |                       |
|                                           |                       | 1101                                      | 2753                  |                       |
|                                           |                       | 1110                                      | 2949                  |                       |
|                                           |                       | 1111                                      | 3146                  |                       |
| b[2:0]                                    | Bits<br>5-3B          | Blue color intensity                      |                       |                       |
|                                           |                       | b[2:0]                                    | current, %            |                       |
|                                           |                       |                                           | log=0                 | log=1                 |
|                                           |                       | 000                                       | 0×I <sub>MAX</sub>    | 0×I <sub>MAX</sub>    |
|                                           |                       | 001                                       | 7%×I <sub>MAX</sub>   | 1%×I <sub>MAX</sub>   |
|                                           |                       | 010                                       | 14%×I <sub>MAX</sub>  | 2%×I <sub>MAX</sub>   |
|                                           |                       | 011                                       | 21%×I <sub>MAX</sub>  | 4%×I <sub>MAX</sub>   |
|                                           |                       | 100                                       | 32%×I <sub>MAX</sub>  | 10%×I <sub>MAX</sub>  |
|                                           |                       | 101                                       | 46%×I <sub>MAX</sub>  | 21%×I <sub>MAX</sub>  |
|                                           |                       | 110                                       | 71%×I <sub>MAX</sub>  | 46%×I <sub>MAX</sub>  |
|                                           |                       | 111                                       | 100%×I <sub>MAX</sub> | 100%×I <sub>MAX</sub> |
|                                           |                       | * log bit is in pattern_gen_ctrl register |                       |                       |

| tt[2:0] | Bits<br>2-0B | Transition time |                     |
|---------|--------------|-----------------|---------------------|
|         |              | tt[2:0]         | Transition time, ms |
|         |              | 000             | 0                   |
|         |              | 001             | 55                  |
|         |              | 010             | 110                 |
|         |              | 011             | 221                 |
|         |              | 100             | 442                 |
|         |              | 101             | 885                 |
|         |              | 110             | 1770                |
|         |              | 111             | 3539                |

**RESET (60H) - RESET REGISTER**

| D7                                                                 | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
|--------------------------------------------------------------------|-----|-----|-----|-----|-----|-----|-----|
| Writing any data to Reset Register in address 60H can reset LP3954 |     |     |     |     |     |     |     |
| r-0                                                                | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 |

## REVISION HISTORY

| Changes from Revision C (March 2013) to Revision D         | Page               |
|------------------------------------------------------------|--------------------|
| • Changed layout of National Data Sheet to TI format ..... | <a href="#">52</a> |

## PACKAGING INFORMATION

| Orderable part number          | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|--------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">LP3954TL/NOPB</a>  | Active        | Production           | DSBGA (YZR)   36 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -30 to 85    | D49B                |
| LP3954TL/NOPB.A                | Active        | Production           | DSBGA (YZR)   36 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -30 to 85    | D49B                |
| <a href="#">LP3954TLX/NOPB</a> | Active        | Production           | DSBGA (YZR)   36 | 1000   SMALL T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -30 to 85    | D49B                |
| LP3954TLX/NOPB.A               | Active        | Production           | DSBGA (YZR)   36 | 1000   SMALL T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -30 to 85    | D49B                |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

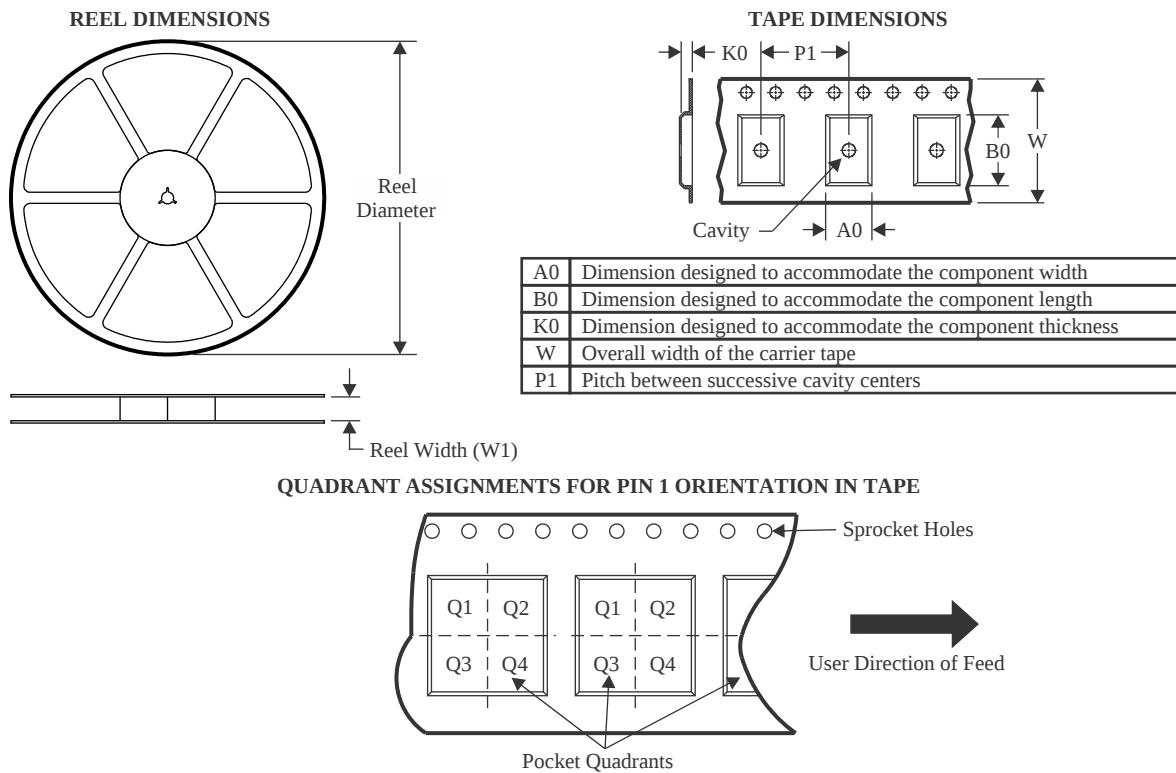
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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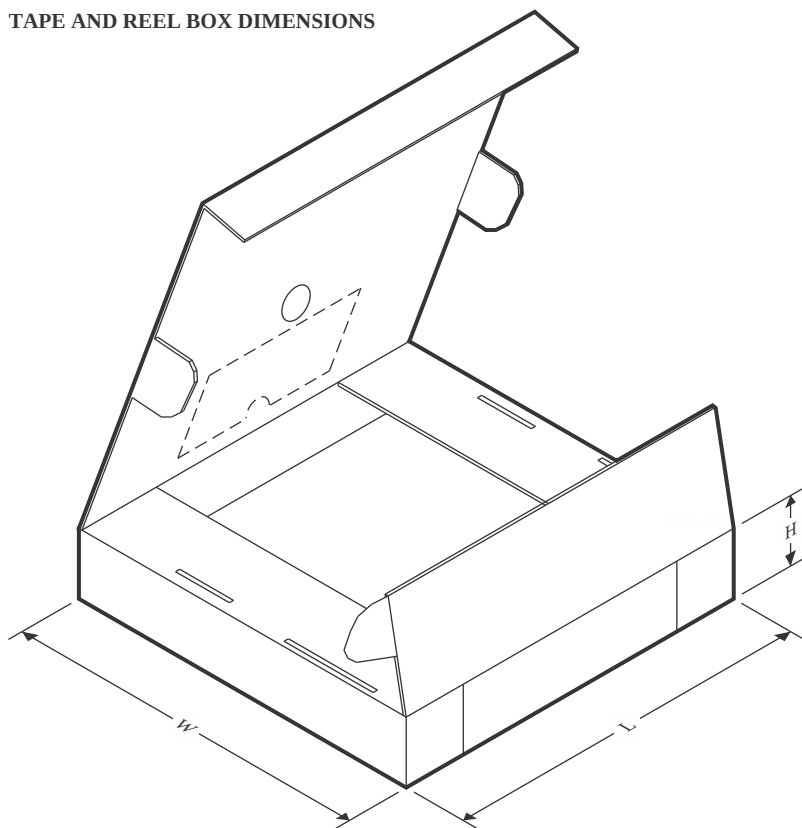
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LP3954TL/NOPB  | DSBGA        | YZR             | 36   | 250  | 177.8              | 12.4               | 3.21    | 3.21    | 0.76    | 8.0     | 12.0   | Q1            |
| LP3954TLX/NOPB | DSBGA        | YZR             | 36   | 1000 | 177.8              | 12.4               | 3.21    | 3.21    | 0.76    | 8.0     | 12.0   | Q1            |

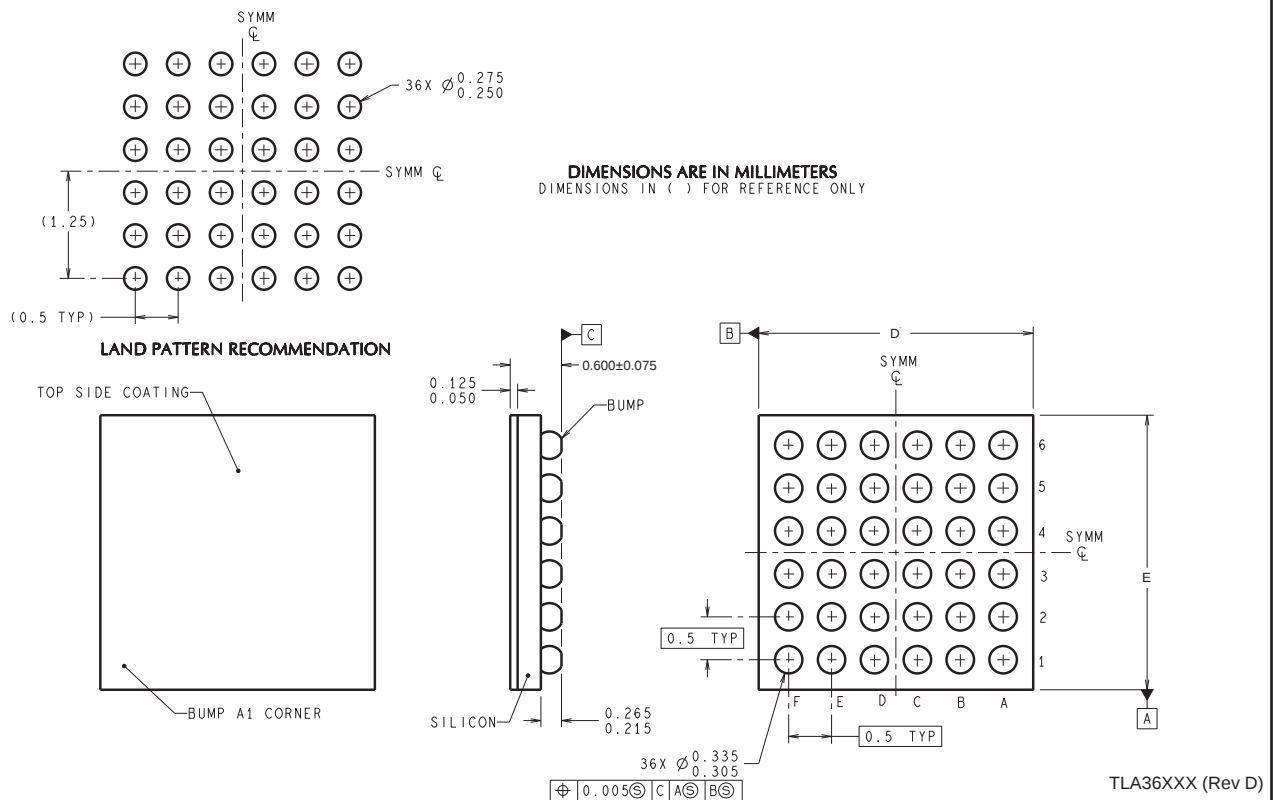
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LP3954TL/NOPB  | DSBGA        | YZR             | 36   | 250  | 208.0       | 191.0      | 35.0        |
| LP3954TLX/NOPB | DSBGA        | YZR             | 36   | 1000 | 208.0       | 191.0      | 35.0        |

YZR0036



D: Max = 3.013 mm, Min = 2.952 mm

E: Max = 3.013 mm, Min = 2.952 mm

4215058/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  
B. This drawing is subject to change without notice.

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