2 0A16

004481

4481 MOT

MC5496 • MC7496
MC9396 • MC8396

ISSUE A

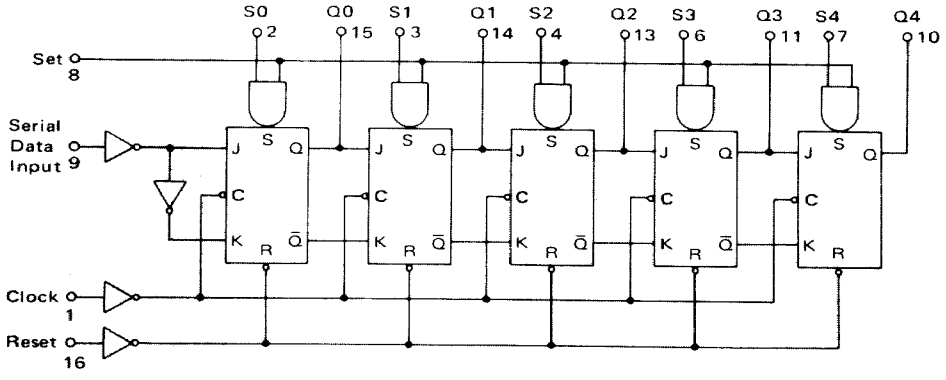
Add Suffix L for 16-pin ceramic dual in-line package (Case 620)
Suffix P for 16-pin plastic dual in-line package (Case 648) MC7496, MC8396

These 5-bit shift registers perform serial in/parallel out, parallel in/serial out, serial in/serial out, and parallel in/parallel out operation.

The output of each flip-flop can be set to the desired state by the proper selection of Set and Reset inputs. By applying a "0" level to the common Reset input, all flip-flop outputs will be forced to the "0" state, and by applying a "1" level to both the common Set input and the input of a specific flip-flop, the output of that flip-flop will be forced to the "1" state. The Set input is independent of the state of the clock and the Reset inputs.

Information is transferred through each flip-flop, as the clock goes from the "0" level to the "1" level and therefore input data must be present prior to the positive edge of the clock.

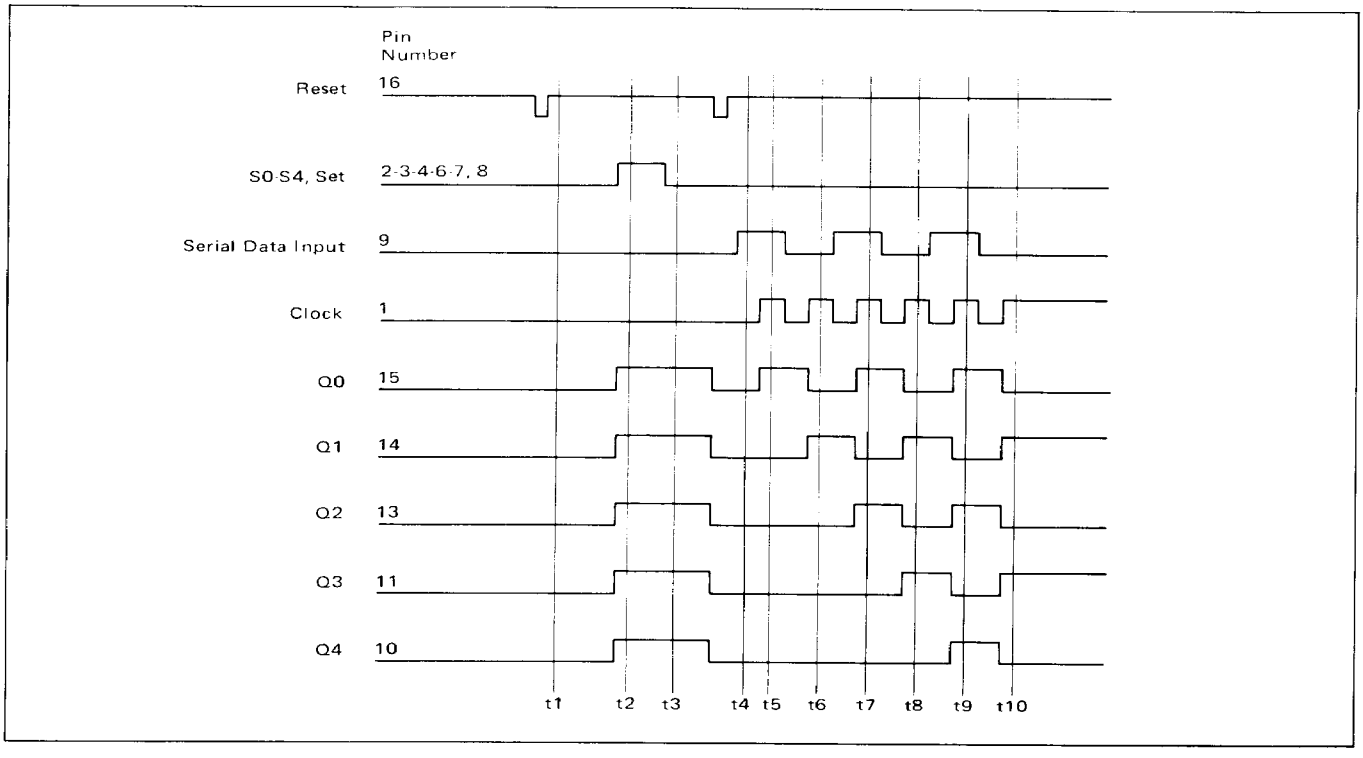
Note that the Reset inputs must be held in the "1" level and Set inputs in the "0" level when clocking occurs.



V_{CC} = Pin 5
Gnd = Pin 12

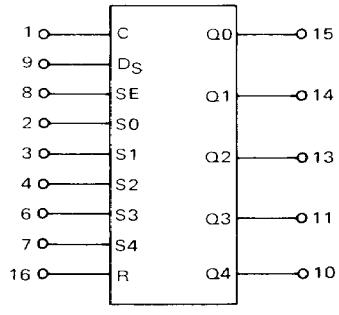
Total Power Dissipation = 240 mW typ/pkg
Minimum Toggle Frequency = 10 MHz

TIMING DIAGRAM



ELECTRICAL CHARACTERISTICS

Tests shown are for only one Set input. The other Set inputs are tested in the same manner.



			TEST CURRENT/VOLTAGE VALUES (All Temperatures)									
			mA		Volts							
			I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{ILT}	V_{IHT}	V_{CCL}	V_{CCH}	
	MC5496, MC9396		16	-0.4	0.4	2.4	5.5	0.8	2.0	4.5	5.5	
	MC7496, MC8396		16	-0.4	0.4	2.4	5.5	0.8	2.0	4.75	5.25	
Characteristic	Symbol	Pin Under Test	MC5496/MC9396 Test Limits −55 to +125°C Min	Max	Unit	MC7496/MC8396 Test Limits 0 to +75°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{ILT}	V_{IHT}	V_{CCL}	V_{CCH}	Gnd
Input																		
Forward Current	I_{IL}	1		-1.6	mAdc		-1.6	mAdc			1					—	5	12
		2		-1.6			-1.6				2					8		
		8		-8.0			-8.0				8					2,3,4,6,7		
		9		-1.6			-1.6				9					—		
		16		-1.6			-1.6				16					—		
Leakage Current	I_{IH}	1		40	μAdc		40	μAdc				1					5	12
		2		40			40					2						8,12
		8		200			200					8						2,3,4,6,7,12
		9		40			40					9						12
		16		40			40					16						12
	I_{IHH}	1		1.0	mAdc		1.0	mAdc					1				5	12
		2											2					8,12
		8											8					2,3,4,6,7,12
		9											9					12
		16											16					12
Output																		
Output Voltage	V_{OL}	10		0.4	Vdc		0.4	Vdc	10					2,3,4,6,7,8,16		—	5	12
		11							11							—		
		13							13							—		
		14							14							—		
		15							15							—		
	V_{OH}	10	2.4		Vdc	2.4		Vdc		10				—	2,3,4,6,7,8	5		12
		11								11				—				
		13								13				—				
		14								14				—				
		15								15				—				
Short Circuit Current	I_{OS}†	10	-20	-57	mAdc	-18	-57	mAdc				7,8					5	10,12
		11										6,8						11,12
		13										4,8						12,13
		14										3,8						12,14
		15										2,8						12,15
Power Requirements (Total Device) Power Supply Drain	I_{CC}	5		68	mAdc		79	mAdc									5	12

†Only one output should be shorted at a time.