# SE98

## SO-DIMM SMBus/I²C-bus temperature sensor

Rev. 01 — 10 May 2006 Product data sheet

## 1. General description

The SE98 is a JEDEC compliant local temperature sensor specifically designed for higher performance SO-DIMM applications. The temperature sensor is mounted on the SO-DIMM module and communicates with the processor via the I²C-bus/SMBus. Since the DRAM refresh rate is dependent on temperature, mounting the temperature sensor on the module allows the processor to adjust the refresh rate based on the actual temperature instead of the calculated worst-case temperature. The end result being longer battery life and better system performance.

The SE98 consists of a ΔΣ A-D converter that continuously monitors and updates its own temperature readings, converts the reading to digital data, and registers into the data temperature register. The data is compared to three alarm registers which are programmed and read via a 2-wire serial bus (SMBus, I²C-bus Standard-mode and I²C-bus Fast-mode). The device also supports the SMBus time-out function that prevents system lock-ups.

SO-DIMM applications normally use the C-grade accuracy SE98TK temperature sensor. For applications requiring higher B-grade accuracy, the SE98TK/1 is available.

## 2. Features

- Monitor local temperature
- JEDEC (JC-42.4) SO-DIMM temperature sensor compliant
- Local temperature sensor accuracy ($V_{DD}$ = 3.3 V ± 10 %):
  - 75 °C to 95 °C—sensor grade B = ±1 °C; sensor grade C = ±2.0 °C
  - 40 °C to 125 °C—sensor grade B = ±2 °C; sensor grade C = ±3 °C
  - –20 °C to 125 °C—sensor grade B = ±3 °C; sensor grade C = ±4 °C
- ADC resolution: 0.125 °C
- Conversion rate: 8 Hz minimum
- Programmable hysteresis threshold: 0 °C, 1.5 °C, 3 °C, 6 °C
- Over/under/critical temperature $\overline{\text{EVENT}}$ output
- Security lock bit for data protection
- Operating voltage range: 3.0 V to 3.6 V
- Maximum operating current: 250 μA
- Maximum standby current is 15 μA
- I²C-bus and SMBus compatible, supporting:
  - Bus speed: 0 Hz to 400 kHz
  - SMBus Alert and Time-out (programmable)
- Operating temperature range: –20 °C to +125 °C

PHILIPS

- Offered in TSSOP8 and HVSON8 packages

## 3. Applications

- Memory module
- Notebook, desktop, server
- Enterprise networking

## 4. Ordering information

**Table 1. Ordering information**

| Type number | Topside mark | Package | | |
|---|---|---|---|---|
| | | Name | Description | Version |
| SE98PW | SE98 | TSSOP8 | plastic thin shrink small outline package; 8 leads; body width 4.4 mm | SOT530-1 |
| SE98PW/1 | 98/1 | | | |
| SE98TK | SE98 | HVSON8 | plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 × 3 × 0.85 mm | SOT908-1 |
| SE98TK/1 | S98/1 | | | |

## 5. Block diagram

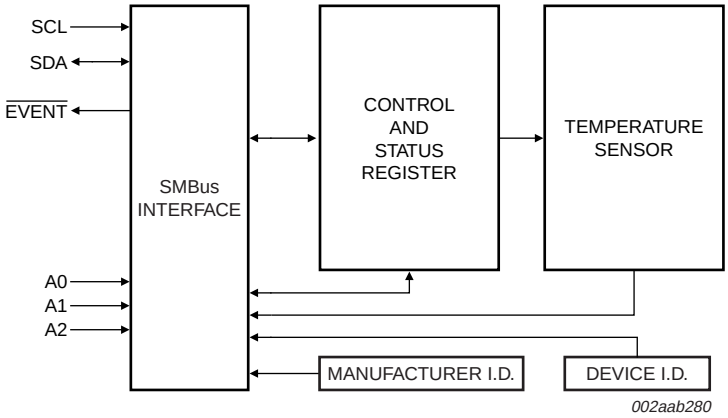



**Fig 1. Block diagram of SE98**

# 6. Pinning information

## 6.1 Pinning

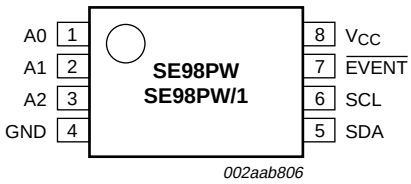



Fig 2. Pin configuration for TSSOP8

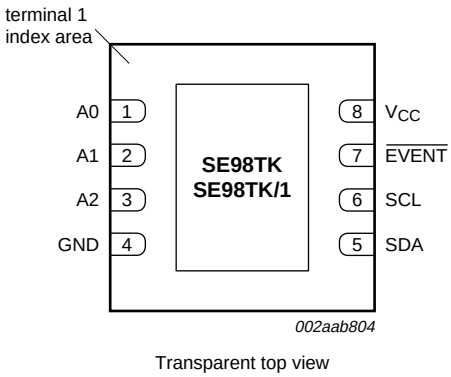



Fig 3. Pin configuration for HVSON8

## 6.2 Pin description

Table 2. Pin description

| Symbol | Pin | Type | Description |
|---|---|---|---|
| A0 | 1 | I | I²C-bus/SMBus slave address bit 0 |
| A1 | 2 | I | I²C-bus/SMBus slave address bit 1 |
| A2 | 3 | I | I²C-bus/SMBus slave address bit 2 |
| GND | 4 | ground | device ground |
| SDA | 5 | I/O | SMBus/I²C-bus serial data input/output (open-drain). Must have external pull-up resistor. |
| SCL | 6 | I | SMBus/I²C-bus serial clock input/output (open-drain). Must have external pull-up resistor. |
| $\overline{\text{EVENT}}$ | 7 | O | Thermal alarm output for high/low and critical temperature limit (open-drain). Must have external pull-up resistor. |
| $V_{CC}$ | 8 | power | device power supply (3.0 V to 3.6 V) |

# 7. Functional description

## 7.1 Serial bus interface

The SE98 uses the 2-wire serial bus (I2C-bus/SMBus) to communicate with a host controller. The serial bus consists of a clock (SCL) and data (SDA) signals. The device can operate on either the I2C-bus Standard/Fast mode or SMBus. The I2C-bus Standard mode is defined to have bus speeds from 0 Hz to 100 kHz, I2C-bus Fast mode from 0 Hz to 400 kHz, and the SMBus is from 10 kHz to 100 kHz. The host or bus master generates the SCL signal, and the SE98 uses the SCL signal to receive or send data on the SDA line. Data transfer is serial, bidirectional, and is one bit at a time with the Most Significant Bit (MSB) transferred first, and a complete I2C-bus data is 1 byte. Since SCL and SDA are open-drain, pull-up resistors must be installed on these pins.

## 7.2 Slave address

The SE98 uses a 4-bit fixed and 3-bit programmable (A0, A1 and A2) 7-bit slave address that allows a total of eight devices to co-exist on the same bus. The input of each pin is sampled at the start of each I2C-bus/SMBus access. The temperature sensor's fixed address is 0011.

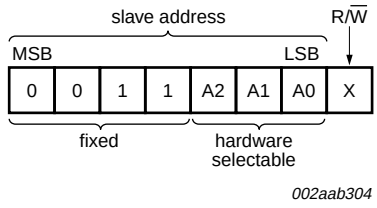



**Fig 4. Slave address**

## 7.3 $\overline{\text{EVENT}}$ output

The $\overline{\text{EVENT}}$ pin is an open-drain output whose function can be programmed as an interrupt, comparator, or critical alarm mode. When the device operates in Interrupt mode, and the temperature reaches a critical temperature, the device switches to the comparator mode automatically and asserts the $\overline{\text{EVENT}}$ pin. When the temperature drops below critical temperature, the device reverts back to either interrupt or comparator mode, as programmed in the Configuration Register. The interrupt latch can be cleared by writing a '1' to the 'clear $\overline{\text{EVENT}}$' bit in the Configuration Register or by performing the SMBus Alert Response Address (ARA).

In comparator mode, the $\overline{\text{EVENT}}$ pin remains asserted until the temperature falls below the value programmed in the Upper Boundary Alarm Trip Register or rises above the value programmed in the Lower Boundary Alarm Trip register, or until the range of these alarm registers are reprogrammed and the temperature falls inside the alarm limits. Figure 5 depicts the $\overline{\text{EVENT}}$ output for all the three modes. All event thresholds use hysteresis as programmed in the Configuration Register.

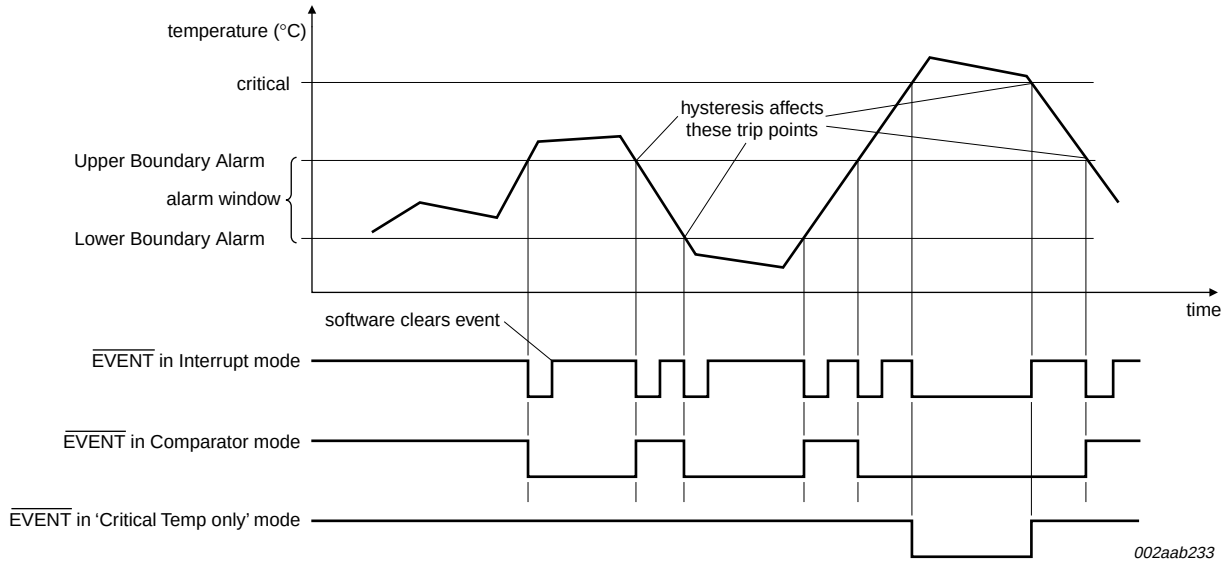



**Fig 5. $\overline{\text{EVENT}}$ output for 'Interrupt', 'Comparator', and 'Critical Temp only' modes**

### 7.3.1 Alarm window

The alarm window consists of two registers: an Upper Boundary Alarm Trip register (02h), and a Lower Boundary Alarm Trip register (03h). The Upper Boundary Alarm Trip register holds the upper temperature trip point, while the Lower Boundary Alarm Trip register holds the lower temperature trip point. When the $\overline{\text{EVENT}}$ control is enabled, the $\overline{\text{EVENT}}$ output will be triggered whenever entering or exiting the alarm window.

### 7.3.2 Critical trip

The device can be programmed in such a way that the $\overline{\text{EVENT}}$ output is triggered when the temperature exceeds the critical trip point set by the Critical Alarm Trip register (04h).

When the temperature sensor reaches the critical temperature value, the device is automatically placed in comparator mode; the $\overline{\text{EVENT}}$ output is only cleared when the temperature falls below the critical temperature value and cannot be cleared through the clear $\overline{\text{EVENT}}$ bit or SMBus Alert.

## 7.4 Conversion rate

The conversion time is the amount of time required for the ADC to complete a temperature measurement for the local temperature sensor. The conversion rate is the inverse of the conversion period which describes the number of cycles the temperature measurement completes in one second—the faster the conversion rate, the faster the temperature reading is updated. The SE98's conversion rate is at least 8 Hz or 125 ms.

## 7.5 Power-up default condition

After power-on, the SE98 is initialized to the following default condition:

- Starts monitoring local sensor
- $\overline{\text{EVENT}}$ register is cleared—$\overline{\text{EVENT}}$ output is pulled HIGH by external pull-ups
- $\overline{\text{EVENT}}$ hysteresis is defaulted to 0 °C
- Command pointer is defaulted to ‘00h’
- Critical Temp, Alarm Temperature Upper and Lower Boundary Trip register are defaulted to 0 °C
- Operational mode: comparator

## 7.6 SMBus Time-out

The SE98 supports SMBus time-out feature. If the host holds SCL LOW between 25 ms and 35 ms, the SE98 would reset its internal state machine to the bus IDLE state to prevent the system bus hang-up. This feature is turned on by default. The SMBus time-out is disabled by writing a logic 1 to bit 7 of register 22h.

**Remark:** When SMBus time-out is enabled, the I²C-bus minimum bus speed is limited by the SMBus time-out timer, and goes down to only 10 kHz.

## 7.7 SMBus Alert

The SE98 supports SMBus Alert when it is programmed for the Interrupt mode and when the $\overline{\text{EVENT}}$ polarity bit is set to logic 0. The $\overline{\text{EVENT}}$ pin can be ANDed with other $\overline{\text{EVENT}}$ or $\overline{\text{ALERT}}$ signals from other slave devices to signal their intention to communicate with the host controller. When the host detects $\overline{\text{EVENT}}$ or $\overline{\text{ALERT}}$ signal LOW, it issues an Alert Response Address (ARA) to which a slave device would respond with its address. When there are multiple slave devices generating an Alert the SE98 performs bus arbitration. If it wins the bus, it responds to the ARA and then clears the $\overline{\text{EVENT}}$ pin.

**Remark:** Either in comparator mode or when the SE98 crosses the critical temperature, the host must also read the $\overline{\text{EVENT}}$ status bit and provide remedy to the situation by bringing the temperature to within the alarm window or below the critical temperature if that bit is set. Otherwise, the $\overline{\text{EVENT}}$ pin will not get de-asserted.

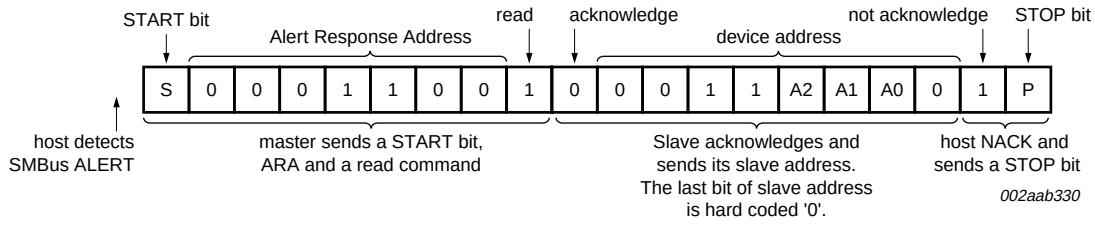



**Fig 6. How SE98 responds to SMBus Alert**

## 7.8 SMBus/I²C-bus interface

The data registers in this device are selected by the Pointer Register. At power-up, the Pointer Register is set to '00', the location for the Capability Register. The Pointer Register latches the last location is was set to. Each data register falls into one of three types of user accessibility:

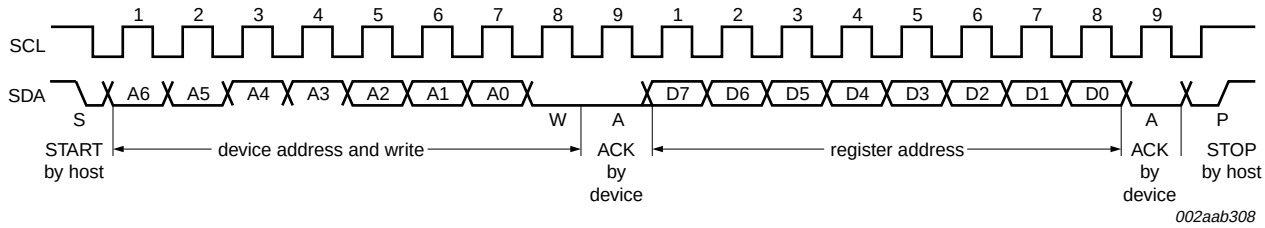
- Read only
- Write only
- Write/Read same address.

A 'write' to this device will always include the address byte and the pointer byte. A write to any register other than the Pointer register requires two data bytes.

Reading this device can take place either of two ways:

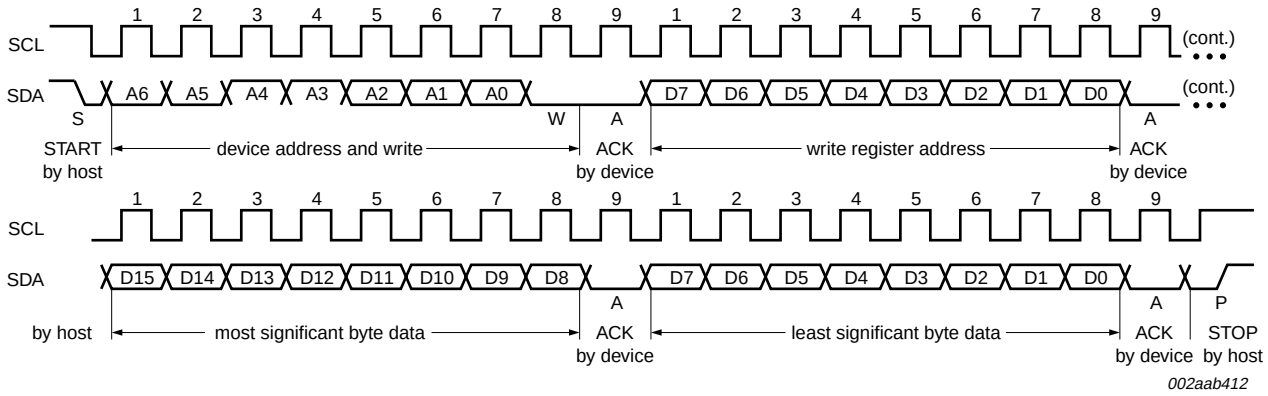
- If the location latched in the Pointer Register is correct (most of the time it is expected that the Pointer Register will point to one of the Temperature Register (as it will be the data most frequently read), then the read can simply consist of an address byte, followed by retrieving the two data bytes.
- If the Pointer Register needs to be set, then an address byte, pointer byte, repeat START, and another address byte will accomplish a read.

The data byte has the most significant bit first. At the end of a read, this device can accept either Acknowledge (ACK) or No Acknowledge (NACK) from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte). It takes this device 125 ms to measure the temperature. Refer to the following timing diagrams on how to program the device.



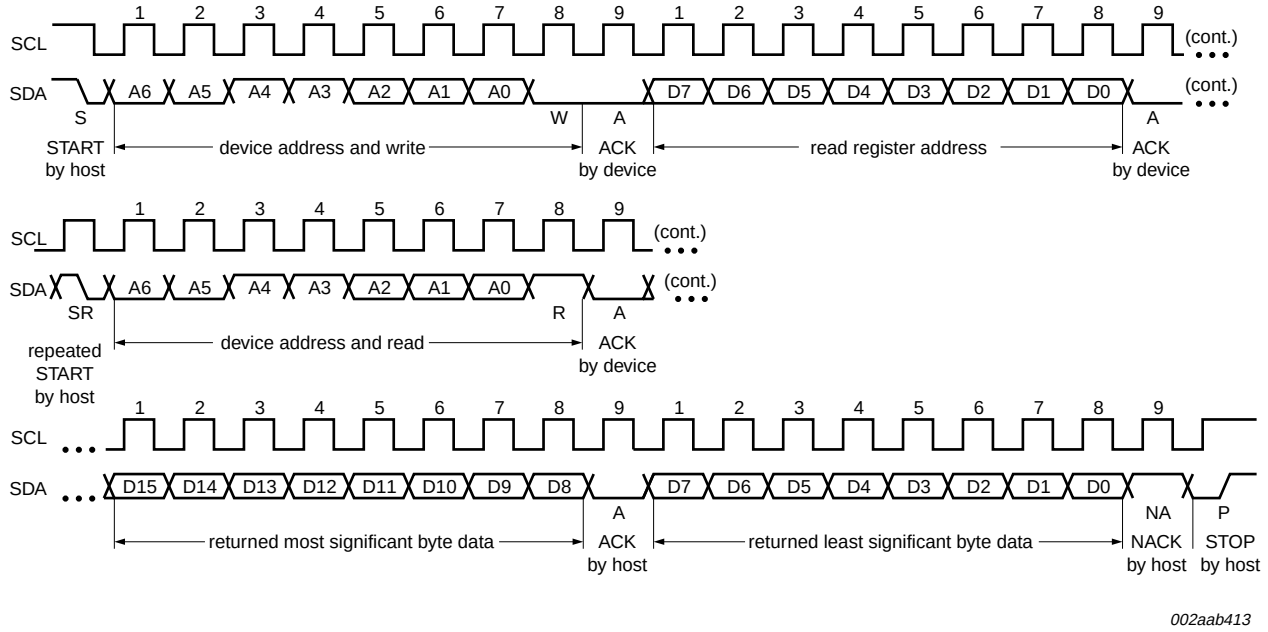

A = ACK = Acknowledge bit. W = Write bit = 0. R = Read bit = 1.

**Fig 7. SMBus/I²C-bus write to the Pointer Register**



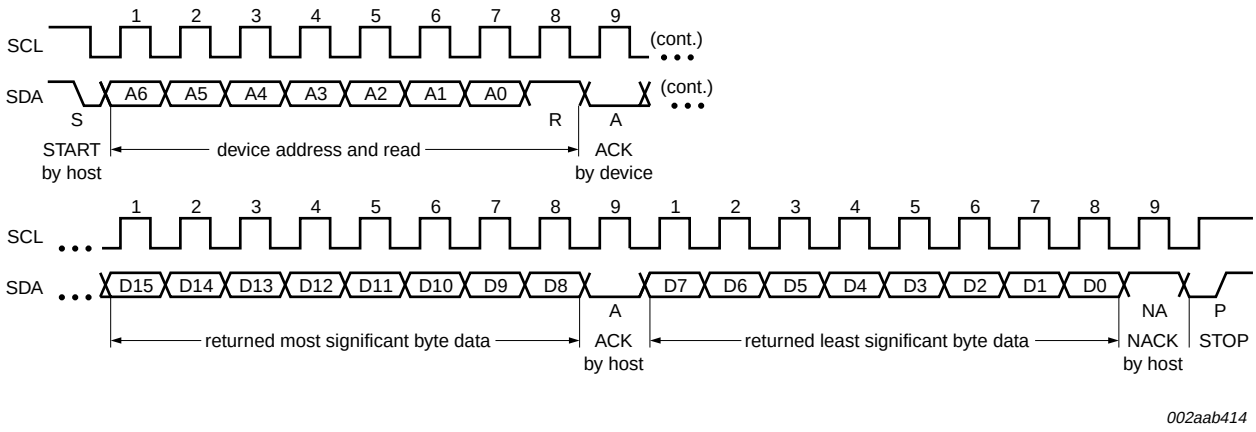

A = ACK = Acknowledge bit. W = Write bit = 0. R = Read bit = 1.

**Fig 8. SMBus/I²C-bus write to the Pointer Register followed by a write data word**




A = ACK = Acknowledge bit. NA = Not Acknowledge bit. W = Write bit = 0. R = Read bit = 1.

**Fig 9. SMBus/I²C-bus write to Pointer Register followed by a repeat START and an immediate data word read**




A = ACK = Acknowledge bit. NA = Not Acknowledge bit. W = Write bit = 0. R = Read bit = 1.

**Fig 10. SMBus/I²C-bus word read from register with a pre-set pointer**

# 8. Register descriptions

## 8.1 Register overview

This section describes all the registers used in the SE98. The registers are used for latching the temperature reading, storing the low and high temperature limits, configuring, the hysteresis threshold and the ADC, as well as reporting status. The device uses the pointer register to access these registers. Read registers, as the name implies, are used for read only, and the write registers are for write only. Any attempt to read from a write-only register will result in reading zeroes. Writing to a read-only register will have no effect on the read even though the write command is acknowledged. The Pointer register is an 8-bit register. All other registers are 16-bit.

**Table 3. Register summary**

| Address (hex) | POR state (hex) | Register name |
|---|---|---|
| n/a | n/a | Pointer Register |
| 00h | 0015h/0017h | Capability Register (B-grade = 0017h, C-grade = 0015h) |
| 01h | 0000h | Configuration Register |
| 02h | 0000h | Upper Boundary Alarm Trip Register |
| 03h | 0000h | Lower Boundary Alarm Trip Register |
| 04h | 0000h | Critical Alarm Trip Register |
| 05h | n/a | Temperature Register |
| 06h | 1131h | Manufacturer ID Register |
| 07h | A101h | Device ID/Revision Register |
| 08h to 21h | 0000h | reserved registers |
| 22h | 0000h | SMBus Register |
| 23h to FFh | 0000h | reserved registers |

A write to reserved registers my cause unexpected results which may result in requiring a reset by removing and re-applying its power.

## 8.2 Capability Register (00h, 16-bit read-only)

**Table 4. Capability Register (address 00h) bit allocation**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Symbol | RFU | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R | R | R | R |
| **Bit** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| Symbol | RFU | | | TRES | | WRNG | HACC | BCAP |
| Reset | 0 | 0 | 0 | 1 | 0 | 1 | [1] | 1 |
| Access | R | R | R | R | R | R | R | R |

[1] See Table 5.

**Table 5. Capability Register (address 00h) bit description**

| Bit | Symbol | Description |
|---|---|---|
| 15:5 | RFU | Reserved for future use. Must be zero. |
| 4:3 | TRES | Temperature resolution.<br>10 — 0.125 °C LSB |
| 2 | WRNG | Wider range.<br>1 — can read temperatures below 0 °C and set sign bit accordingly |
| 1 | HACC | Higher accuracy.<br>0 — Accuracy ±2 °C over the active range and ±3 °C over the monitor range (C-grade)<br>1 — High accuracy ±1 °C over the active range and ±2 °C over the monitor range (B-grade) |
| 0 | BCAP | Basic capability.<br>1 — Has Alarm and Critical Trips capability. |

## 8.3 Configuration Register (01h, 16-bit read/write)

Table 6. Configuration Register (address 01h) bit allocation

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Symbol | RFU | | | | | HEN | | SHMD |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R | R/W | R/W | R/W |
| **Bit** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| Symbol | CTLB | AWLB | CEVNT | ESTAT | EOCTL | CVO | EP | EMD |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 7. Configuration Register (address 01h) bit description

| Bit | Symbol | Description |
|---|---|---|
| 15:11 | RFU | reserved for future use; must be ‘0’. |
| 10:9 | HEN | Hysteresis Enable<br>00 — Disable hysteresis (default)<br>01 — Enable hysteresis at 1.5 °C<br>10 — Enable hysteresis at 3 °C<br>11 — Enable hysteresis at 6 °C<br>When enabled, hysteresis is applied to temperature movement around trigger points. For example, consider the behavior of the ‘Above Alarm Window’ bit (bit 14 of the Temperature register) when the hysteresis is set to 3 °C. As the temperature rises, bit 14 will be set to 1 (temperature is above the alarm window) when the Temperature register contains a value that is greater than the value in the Alarm Temperature Upper Boundary Register. If the temperature decreases, bit 14 will remain set until the measured temperature is less than or equal to the value in the Alarm Temperature Upper Boundary register minus 3 °C. (Refer to Figure 5 and Table 8).<br>Similarly, the ‘Below Alarm Window’ bit (bit 13 of the Temperature register) will be set to 0 (temperature is equal to or above the Alarm Window Lower Boundary Trip Register) when the value in the Temperature register is equal to or greater than the value in the Alarm Temperature Lower Boundary Register. As the temperature decreases, bit 13 will be set to 1 when the value in the Temperature Register is equal to or less than the value in the Alarm Temperature Lower Boundary Register minus 3 °C. Note that hysteresis is also applied to $\overline{\text{EVENT}}$ pin functionality.<br>When either of the lock bits is set, these bits cannot be altered. |
| 8 | SHMD | Shutdown Mode.<br>0 — Enabled Temperature Sensor (default)<br>1 — Disabled Temperature Sensor<br>When shut down, the thermal sensor diode and A/D converter are disabled to save power, no events will be generated. When either of the lock bits is set, this bit cannot be set until unlocked. However, it can be cleared at any time. |

**Table 7. Configuration Register (address 01h) bit description** *…continued*

| Bit | Symbol | Description |
|---|---|---|
| 7 | CTLB | Critical Trip Lock bit.<br>0 — Critical Alarm Trip Register is not locked and can be altered (default).<br>1 — Critical Alarm Trip Register settings cannot be altered.<br>This bit is initially cleared. When set, this bit will return a 1, and remains locked until cleared by internal Power-on reset. This bit can be written with a single write and do not require double writes. |
| 6 | AWLB | Alarm Window Lock bit.<br>0 — Upper and Lower Alarm Trip Registers are not locked and can be altered (default).<br>1 — Upper and Lower Alarm Trip Registers setting cannot be altered.<br>This bit is initially cleared. When set, this bit will return a 1 and remains locked until cleared by internal power-on reset. This bit can be written with a single write and does not require double writes. |
| 5 | CEVNT | Clear $\overline{\text{EVENT}}$ (write only).<br>0 — No effect (default).<br>1 — Clears active $\overline{\text{EVENT}}$ in Interrupt mode. Writing to this register has no effect in Comparator mode.<br>When read, this register always returns zero. |
| 4 | ESTAT | $\overline{\text{EVENT}}$ Status (read only).<br>0 — $\overline{\text{EVENT}}$ output condition is not being asserted by this device (default).<br>1 — $\overline{\text{EVENT}}$ output pin is being asserted by this device due to Alarm Window or Critical Trip condition.<br>The actual event causing the event can be determined from the Read Temperature Register. Interrupt Events can be cleared by writing to the 'clear $\overline{\text{EVENT}}$' bit. Writing to this bit will have no effect. |
| 3 | EOCTL | $\overline{\text{EVENT}}$ Output Control.<br>0 — $\overline{\text{EVENT}}$ output disabled (default).<br>1 — $\overline{\text{EVENT}}$ output enabled.<br>When either of the lock bits is set, this bit cannot be altered until unlocked. |
| 2 | CVO | Critical Event Only.<br>0 — $\overline{\text{EVENT}}$ output on Alarm or Critical temperature event (default)<br>1 — $\overline{\text{EVENT}}$ only if temperature is above the value in the critical temperature register<br>When the alarm window lock bit is set, this bit cannot be altered until unlocked. |
| 1 | EP | $\overline{\text{EVENT}}$ Polarity.<br>0 — active LOW (default).<br>1 — active HIGH. When either of the alarm or critical lock bits is set, this bit cannot be altered until unlocked. |
| 0 | EMD | $\overline{\text{EVENT}}$ Mode.<br>0 — comparator output mode (default)<br>1 — interrupt mode<br>When either of the alarm or critical lock bits is set, this bit cannot be altered until unlocked. |

**Table 8. Hysteresis Enable**

| Action | Below Alarm Window Bit (bit 13) | | Above Alarm Window Bit (bit 14) | |
|---|---|---|---|---|
| | Temperature slope | Threshold temperature | Temperature slope | Temperature |
| sets | falling | $T_{th(low)}$ – Hyst | rising | $T_{th(high)}$ |
| clears | rising | $T_{th(low)}$ | falling | $T_{th(high)}$ – Hyst |

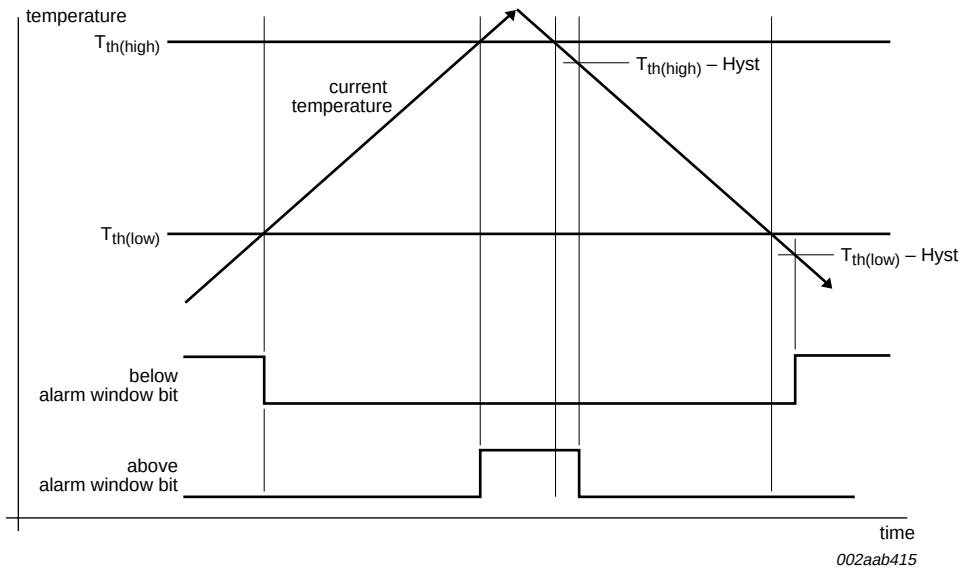



**Fig 11. Hysteresis timing**

## 8.4 Temperature format

The 16-bit value used in the following Trip Point Set and Temperature Read-Back registers is 2's complement with the Least Significant Bit (LSB) equal to 0.0625 °C. For example:

- A value of 019Ch will represent 25.75 °C
- A value of 07C0h will represent 124 °C
- A value of 1E64h will represent –25.75 °C.

The resolution is 0.125 °C. The unused LSB (bit 0) is set to '0'. Bit 11 will have a resolution of 128 °C.

The upper 3 bits of the temperature register indicate Trip Status based on the current temperature, and are not affected by the status of the Event Output.

## 8.5 Temperature Trip Point registers

### 8.5.1 Upper Boundary Alarm Trip Register (16-bit read/write)

The value is the upper threshold temperature value for Alarm mode. The data format is 2's complement with bit 2 = 0.25 °C. 'RFU' bits will always report zero. Interrupts will respond to the presently programmed boundary values. If boundary values are being altered in-system, it is advised to turn off interrupts until a known state can be obtained to avoid superfluous interrupt activity.

**Table 9. Upper Boundary Alarm Trip Register bit allocation**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Symbol | RFU | | | SIGN | UBT | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R/W | R/W | R/W | R/W | R/W |
| **Bit** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| Symbol | UBT | | | | | | RFU | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R | R |

**Table 10. Upper Boundary Alarm Trip Register bit description**

| Bit | Symbol | Description |
|---|---|---|
| 15:13 | RFU | reserved; always 0 |
| 12 | SIGN | Sign (MSB) |
| 11:2 | UBT | Upper Boundary Alarm Trip Temperature (LSB = 0.25 °C) |
| 1:0 | RFU | reserved; always 0 |

### 8.5.2 Lower Boundary Alarm Trip Register (16-bit read/write)

The value is the lower threshold temperature value for Alarm mode. The data format is 2's complement with bit 2 = 0.25 °C. RFU bits will always report zero. Interrupts will respond to the presently programmed boundary values. If boundary values are being altered in-system, it is advised to turn off interrupts until a known state can be obtained to avoid superfluous interrupt activity.

**Table 11. Lower Boundary Alarm Trip Register bit allocation**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Symbol | | RFU | | SIGN | | LBT | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R/W | R/W | R/W | R/W | R/W |
| **Bit** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| Symbol | | | | LBT | | | RFU | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R | R |

**Table 12. Lower Boundary Alarm Trip Register bit description**

| Bit | Symbol | Description |
|---|---|---|
| 15:13 | RFU | reserved; always 0 |
| 12 | SIGN | Sign (MSB) |
| 11:2 | LBT | Lower Boundary Alarm Trip Temperature (LSB = 0.25 °C) |
| 1:0 | RFU | reserved; always 0 |

### 8.5.3 Critical Alarm Trip Register (16-bit read/write)

The value is the critical temperature. The data format is 2's complement with bit 2 = 0.25 °C. RFU bits will always report zero.

**Table 13. Lower Boundary Alarm Trip Register bit allocation**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Symbol | | RFU | | SIGN | | CT | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R/W | R/W | R/W | R/W | R/W |
| **Bit** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| Symbol | | | | CT | | | RFU | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R | R |

**Table 14. Critical Alarm Trip Register bit description**

| Bit | Symbol | Description |
|---|---|---|
| 15:13 | RFU | reserved; always 0 |
| 12 | SIGN | Sign (MSB) |
| 11:2 | CT | Critical Alarm Trip Temperature (LSB = 0.25 °C) |
| 1:0 | RFU | reserved; always 0 |

## 8.6 Temperature Register (16-bit read-only)

Table 15. Temperature Register bit allocation

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Symbol | ACT | AAW | BAW | SIGN | TEMP | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R | R | R | R |
| **Bit** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| Symbol | TEMP | | | | | | | RFU |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R | R | R | R |

Table 16. Temperature Register bit description

| Bit | Symbol | Description |
|---|---|---|
| 15 | ACT | Above Critical Trip.<br>0 — temperature is below the Critical Alarm Trip Register setting<br>1 — temperature is equal to or above the Critical Alarm Trip Register setting |
| 14 | AAW | Above Alarm Window.<br>0 — temperature is equal to or below the Upper Boundary Alarm Trip Register<br>1 — temperature is above the Alarm window |
| 13 | BAW | Below Alarm Window.<br>0 — temperature is equal to or above the Lower Boundary Alarm Trip Register<br>1 — temperature is below the Alarm window |
| 12 | SIGN | Sign bit.<br>0 — positive temperature value<br>1 — negative temperature value |
| 11:1 | TEMP | Temperature Value (2's complement). (LSB = 0.125 °C) |
| 0 | RFU | reserved; always 0 |

## 8.7 Manufacturer's ID register (16-bit read-only)

The manufacture's ID matches that assigned to Philips' PCI SIG (1131h), and is intended for use to identify the manufacturer of the device.

Table 17. Manufacturer's ID register bit allocation

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Symbol | Manufacturer ID | | | | | | | |
| Reset | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| Access | R | R | R | R | R | R | R | R |
| **Bit** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| Symbol | (cont.) | | | | | | | |
| Reset | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Access | R | R | R | R | R | R | R | R |

## 8.8 Device ID register

The device ID and device revision are A1h and 00h, respectively.

**Table 18. Device ID register bit allocation**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Symbol | Device ID | | | | | | | |
| Reset | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| Access | R | R | R | R | R | R | R | R |
| **Bit** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| Symbol | Device revision | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Access | R | R | R | R | R | R | R | R |

## 8.9 SMBus Register

**Table 19. SMBus Time-out register bit allocation**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Symbol | RFU | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R | R | R | R |
| **Bit** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| Symbol | STMOUT | RFU | | | | | | SALRT |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R | R | R | R | R | R | R/W |

**Table 20. SMBus Time-out register bit description**

| Bit | Symbol | Description |
|---|---|---|
| 15:8 | RFU | reserved; always 0 |
| 7 | STMOUT | SMBus time-out.<br>0 — SMBus time-out is enabled (default)<br>1 — disable SMBus time-out<br>When either of the lock bits is set, this bit cannot be altered until unlocked. |
| 6:1 | RFU | reserved; always 0 |
| 0 | SALRT | SMBus Alert.<br>0 — SMBus Alert is enabled (default)<br>1 — disable SMBus Alert<br>When either of the lock bits is set, this bit cannot be altered until unlocked. |

# 9. Application design-in information

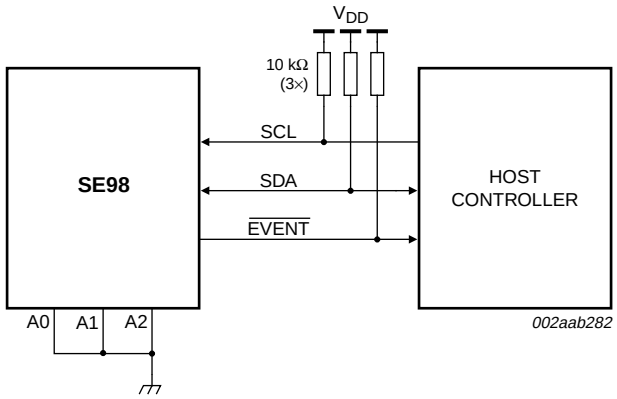



Fig 12. Typical application

# 10. Limiting values

Table 21. Limiting values

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | –0.3 | +6 | V |
| $V_n$ | voltage on any other pin | | –0.3 | +6 | V |
| $I_{sink}$ | sink current | SDA, SCL, $\overline{EVENT}$ pins | –1 | 50.0 | mA |
| $V_{esd}$ | electrostatic discharge voltage | HBM | - | 2500 | V |
| | | MM | - | 250 | V |
| | | CDM | - | 1000 | V |
| $T_{j(max)}$ | maximum junction temperature | | - | 150 | °C |
| $T_{stg}$ | storage temperature | | –65 | +165 | °C |

# 11. Characteristics

**Table 22. Characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $T_{lim(acc)}$ | temperature limit accuracy | B-grade temperature accuracy; $V_{DD}$ = 3.3 V ± 10 % | | | | |
| | | $T_{amb}$ = 75 °C to 95 °C | –1.0 | < ±0.5 | +1.0 | °C |
| | | $T_{amb}$ = 40 °C to 125 °C | –2.0 | < ±1 | +2.0 | °C |
| | | $T_{amb}$ = –20 °C to 125 °C | –3.0 | < ±2 | +3.0 | °C |
| | | C-grade temperature accuracy; $V_{DD}$ = 3.3 V ± 10 % | | | | |
| | | $T_{amb}$ = 75 °C to 95 °C | –2.0 | < ±1 | +2.0 | °C |
| | | $T_{amb}$ = 40 °C to 125 °C | –3.0 | < ±2 | +3.0 | °C |
| | | $T_{amb}$ = –20 °C to 125 °C | –4.0 | < ±3 | +4.0 | °C |
| $T_{res}$ | temperature resolution | | - | 0.25 | - | °C |
| $I_{CC(AV)}$ | average supply current | | - | - | 250 | µA |
| $I_{stb(VCC)}$ | power supply standby current | SMBus inactive | - | 8 | 15 | µA |
| $T_{conv}$ | conversion period | | - | 100 | - | ms |
| $E_{f(conv)}$ | conversion rate error | percentage error in programmed data | –30 | - | 30 | % |
| $I_L$ | leakage current | on A0, A1, A2 pins | - | 1 | - | µA |
| $V_{DD}$ | supply voltage | | 3.0 | 3.3 | 3.6 | V |

**Table 23. SMBus DC characteristics**

*$V_{DD}$ = 3.0 V to 3.6 V; $T_{amb}$ = –20 °C to +120 °C; unless otherwise specified. These specifications are guaranteed by design.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | HIGH-level input voltage | SCL, SDA; $V_{DD}$ = 3.0 V to 3.6 V | 2.2 | - | - | V |
| $V_{IL}$ | LOW-level input voltage | SCL, SDA; $V_{DD}$ = 3.0 V to 3.6 V | - | - | 0.8 | V |
| $I_{OL(sink)EVENT\_N}$ | LOW-level output sink current on pin $\overline{EVENT}$ | $V_{OL}$ = 0.4 V | 1 | - | - | mA |
| $I_{OL(sink)(SDA)}$ | LOW-level output sink current on pin SDA | $V_{OL}$ = 0.6 V | 6 | - | - | mA |
| $I_{LOH}$ | HIGH-level output leakage current | $V_{OH} = V_{DD}$ | - | - | 1.0 | µA |
| $I_{LIH}$ | HIGH-level input leakage current | $V_I = V_{DD}$ or GND | –1.0 | - | 1.0 | µA |
| $I_{LIL}$ | LOW-level input leakage current | $V_I = V_{DD}$ or GND | –1.0 | - | 1.0 | µA |
| $C_i$ | input capacitance | SCL, SDA pins | - | 5 | 10 | pF |

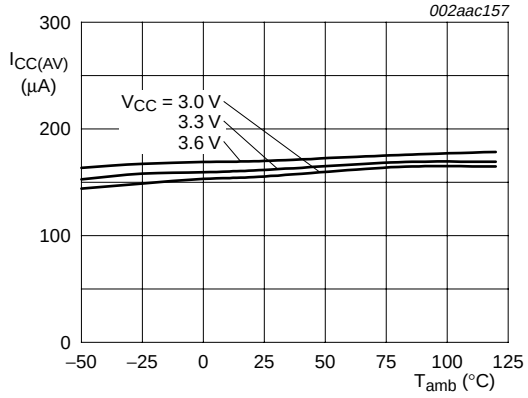



Fig 13. Typical $I_{CC(AV)}$

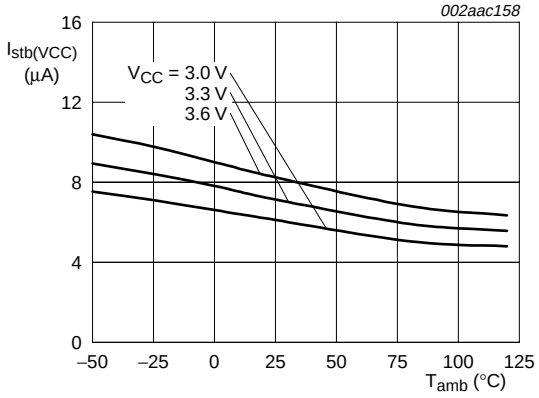



Fig 14. Typical $I_{stb(VCC)}$

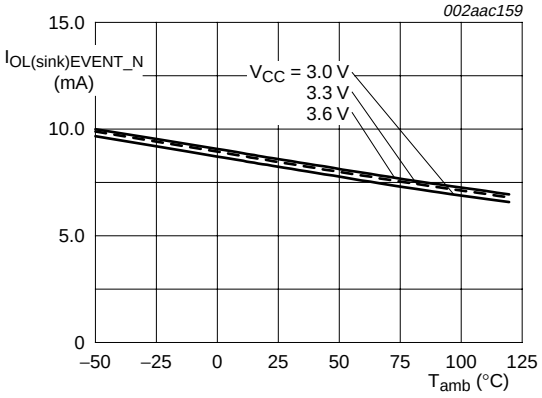



Fig 15. Typical $I_{OL(sink)EVENT\_N}$ at 0.4 V

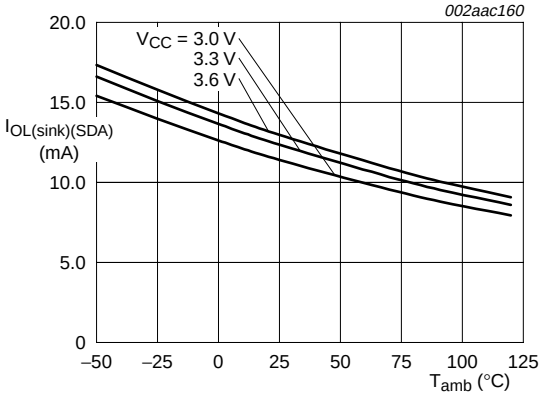
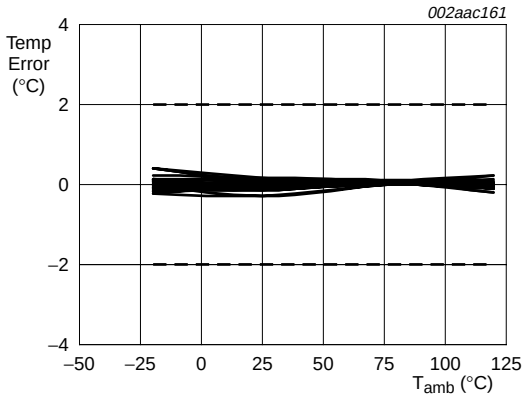



Fig 16. Typical $I_{OL(sink)(SDA)}$ at 0.6 V




Sample of 25 devices at $V_{CC}$ = 3.3 V

Fig 17. Typical Temp Error

**Table 24. SMBus AC characteristics**

*$V_{DD}$ = 3.0 V to 3.6 V; $T_{amb}$ = –20 °C to +120 °C; unless otherwise specified. These specifications are guaranteed by design. The AC specifications fully meet or exceed SMBus 2.0 specifications, but allow the bus to interface with the I²C-bus from DC to 400 kHz.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | | | 0 | - | 400 | kHz |
| $t_{LOW}$ | LOW period of the SCL clock | 10 % to 10 % | | 1.3 | - | - | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | 90 % to 90 % | | 0.6 | - | - | µs |
| $t_{BUF}$ | bus free time between a STOP and START condition | | | 4.7 | - | - | µs |
| $t_{HD;STA}$ | hold time (repeated) START condition | 10 % of SDA to 90 % of SCL | [1] | 4.7 | - | - | µs |
| $t_{HD;DAT}$ | data hold time | | [2] | 300 | - | - | ns |
| $t_{SU;DAT}$ | data set-up time | | | 250 | - | - | ns |
| $t_{SU;STA}$ | set-up time for a repeated START condition | | [3] | 250 | - | - | ns |
| $t_{SU;STO}$ | set-up time for STOP condition | | | 0.6 | - | - | µs |
| $t_r$ | rise time of both SDA and SCL signals | | | - | - | 300 | ns |
| $t_f$ | fall time of both SDA and SCL signals | | | - | - | 300 | ns |
| $t_{f(o)}$ | output fall time | | | - | - | 250 | ns |
| $t_{to(SMBus)}$ | SMBus time-out time | | [4] | 25 | - | 35 | ms |

[1] Delay from SDA START to first SCL HIGH-to-LOW transition.

[2] Delay from SCL HIGH-to-LOW transition to SDA edges.

[3] Delay from SCL LOW-to-HIGH transition to restart SDA.

[4] LOW period to reset SMBus.

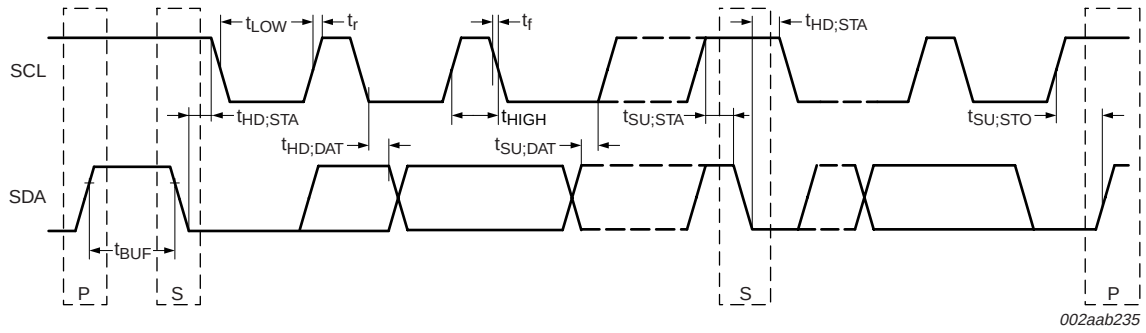
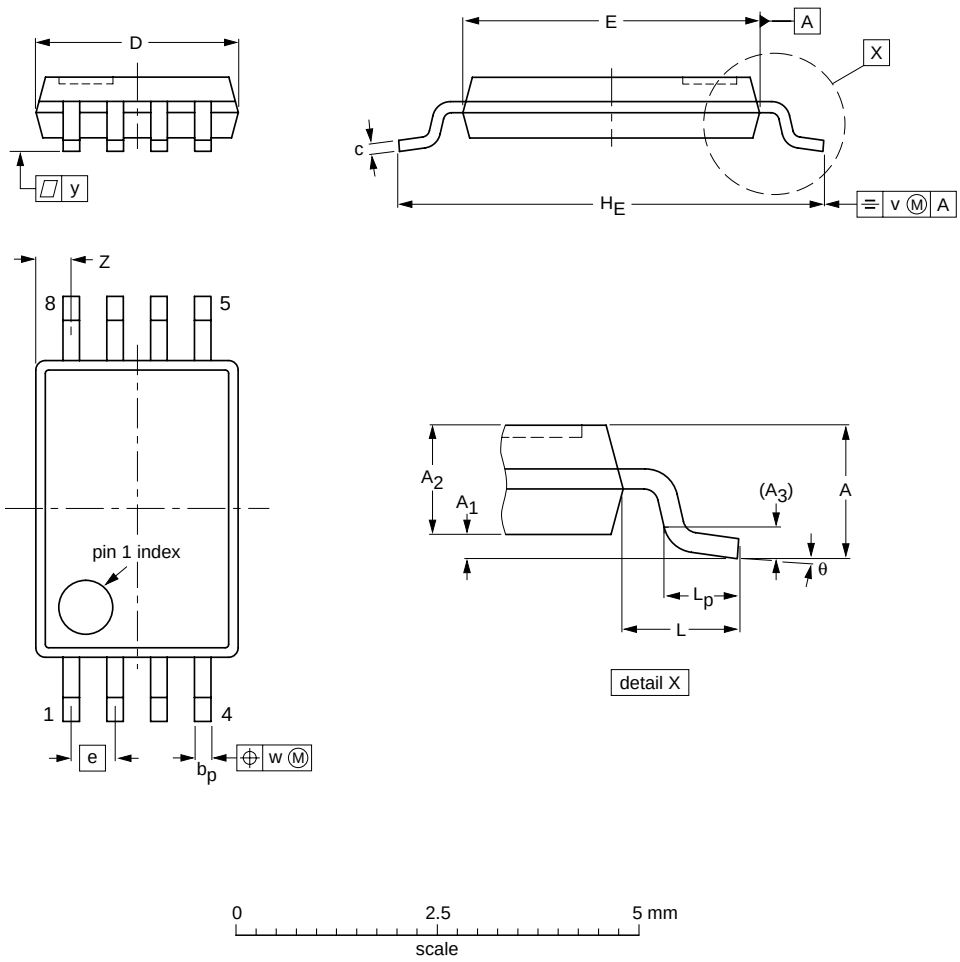



**Fig 18. AC timing diagram**

## 12. Package outline

**TSSOP8: plastic thin shrink small outline package; 8 leads; body width 4.4 mm** **SOT530-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.85 | 0.25 | 0.30<br>0.19 | 0.20<br>0.13 | 3.1<br>2.9 | 4.5<br>4.3 | 0.65 | 6.5<br>6.3 | 0.94 | 0.7<br>0.5 | 0.1 | 0.1 | 0.1 | 0.70<br>0.35 | 8°<br>0° |

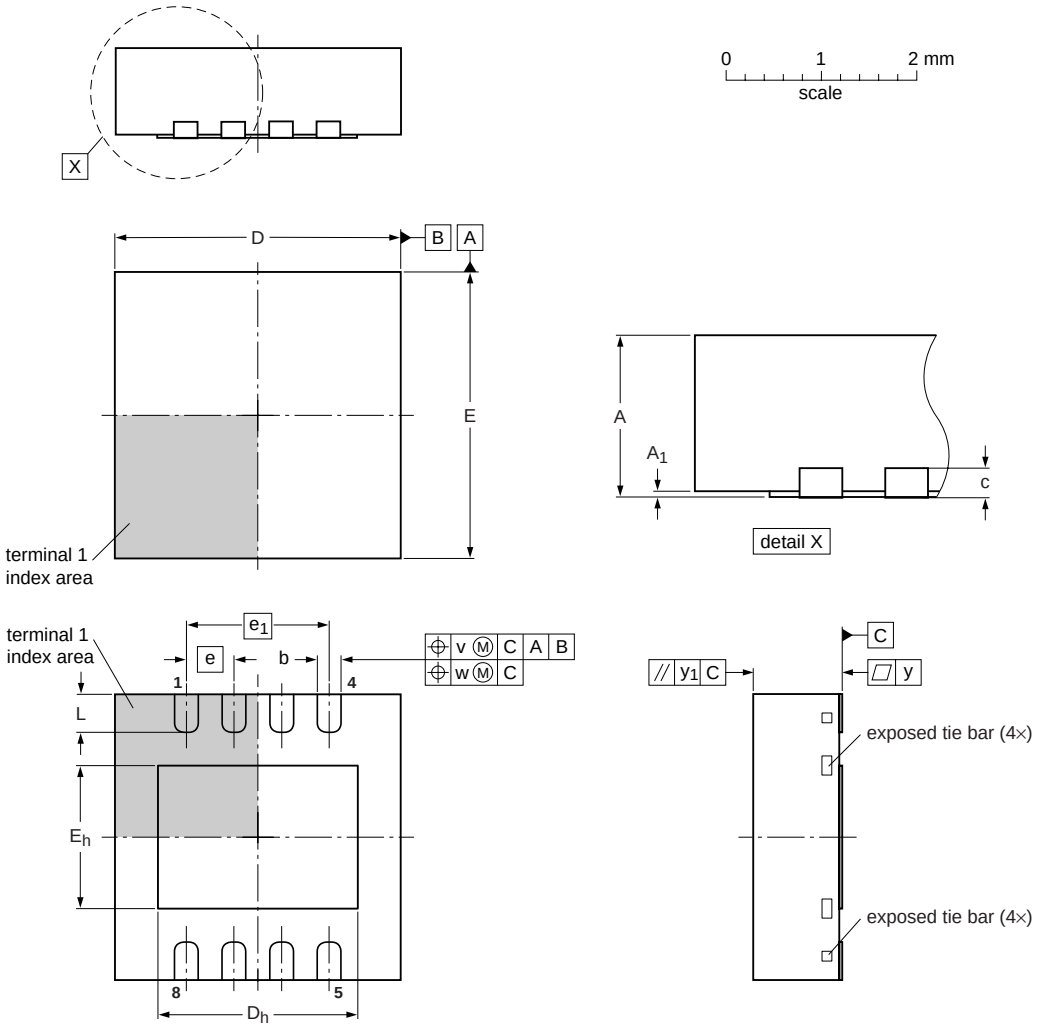
**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT530-1 | | MO-153 | | | | ~~00-02-24~~<br>03-02-18 |

**Fig 19. Package outline SOT530-1 (TSSOP8)**

**HVSON8: plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 x 3 x 0.85 mm** **SOT908-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A(1) max. | $A_1$ | b | c | D(1) | $D_h$ | E(1) | $E_h$ | e | $e_1$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.05<br>0.00 | 0.3<br>0.2 | 0.2 | 3.1<br>2.9 | 2.25<br>1.95 | 3.1<br>2.9 | 1.65<br>1.35 | 0.5 | 1.5 | 0.5<br>0.3 | 0.1 | 0.05 | 0.05 | 0.1 |

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT908-1 | | MO-229 | | | | ~~05-09-26~~<br>05-10-05 |

**Fig 20. Package outline SOT908-1 (HVSON8)**

# 13. Soldering

## 13.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

## 13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 260 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 $mm^3$ so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 $mm^3$ so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

## 13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

## 13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

## 13.5 Package related soldering information

**Table 25. Suitability of surface mount IC packages for wave and reflow soldering methods**

| Package[1] | Soldering method | |
|---|---|---|
| | Wave | Reflow[2] |
| BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, VFBGA, XSON | not suitable | suitable |
| DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS | not suitable[4] | suitable |
| PLCC[5], SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended[5][6] | suitable |
| SSOP, TSSOP, VSO, VSSOP | not recommended[7] | suitable |
| CWQCCN..L[8], PMFP[9], WQCCN..L[8] | not suitable | not suitable |

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

## 14. Abbreviations

**Table 26. Abbreviations**

| Acronym | Description |
|---|---|
| ADC | A-to-D Converter |
| ARA | Alert Response Address |
| CDM | Charged Device Model |
| DIMM | Dual In-line Memory Module |
| HBM | Human Body Model |
| I²C-bus | Inter IC bus |
| LSB | Least Significant Bit |
| MM | Machine Model |
| MSB | Most Significant Bit |
| SO-DIMM | Small Outline Dual In-line Memory Module |
| POR | Power-On Reset |
| SMBus | System Management Bus |

## 15. Revision history

**Table 27. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| SE98_1 (9397 750 14649) | 20060510 | Product data sheet | - | - |

# 16. Legal information

## 16.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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