The RF Sub–Micron MOSFET Line

RF Power Field Effect Transistors

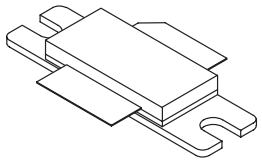
N–Channel Enhancement–Mode Lateral MOSFETs

MRF9080
MRF9080S

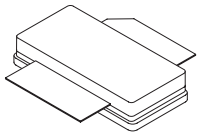
**GSM 900 MHz FREQUENCY BAND,
75 W, 26 V
LATERAL N–CHANNEL
BROADBAND RF POWER MOSFETs**

Designed for GSM 900 MHz frequency band, the high gain and broadband performance of these devices make them ideal for large–signal, common–source amplifier applications in 26 volt base station equipment.

- Typical Performance for GSM Frequencies, 921 to 960 MHz, 26 Volts
  Output Power @ P1db: 75 Watts
  Power Gain @ P1db: 18.5 dB
  Efficiency @ P1db: 55%
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Ease of Design for Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 921 MHz, 90 Watts CW
  Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters



**CASE 465–04, STYLE 1
(MRF9080)**



**CASE 465A–04, STYLE 1
(MRF9080S)**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Typical)
Machine Model	M1 (Typical)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 26 Vds, V_{GS} = 0)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$V_{GS(th)}$	2.0	—	4.0	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 700 mAdc)	$V_{GS(Q)}$	—	3.7	—	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.19	0.4	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 6 Adc)	g_{fs}	—	8.0	—	S
DYNAMIC CHARACTERISTICS (1)					
Output Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	73	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	2.9	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture) (2)					
Power Output, 1 dB Compression Point (V_{DD} = 26 Vdc, I_{DQ} = 600 mA, f = 921 and 960 MHz)	P_{1dB}	68	75	—	W
Common–Source Amplifier Power Gain @ 70 W (Min) (V_{DD} = 26 Vdc, I_{DQ} = 600 mA, f = 921 and 960 MHz)	G_{ps}	17	18.5	20	dB
Drain Efficiency @ P_{out} = 70 W (V_{DD} = 26 Vdc, I_{DQ} = 600 mA, f = 921 and 960 MHz)	$\eta 1$	47	52	—	%
Drain Efficiency @ P1dB (V_{DD} = 26 Vdc, I_{DQ} = 600 mA, f = 921 and 960 MHz)	$\eta 2$	—	55	—	%
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 70 W, I_{DQ} = 600 mA, f = 921 and 960 MHz)	IRL	9.5	12.5	—	dB
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 90 W CW, I_{DQ} = 600 mA, f = 921 MHz, VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally input matched.
(2) To meet application requirements, Motorola test fixtures are designed to cover full GSM 900 band ensuring batch to batch consistency

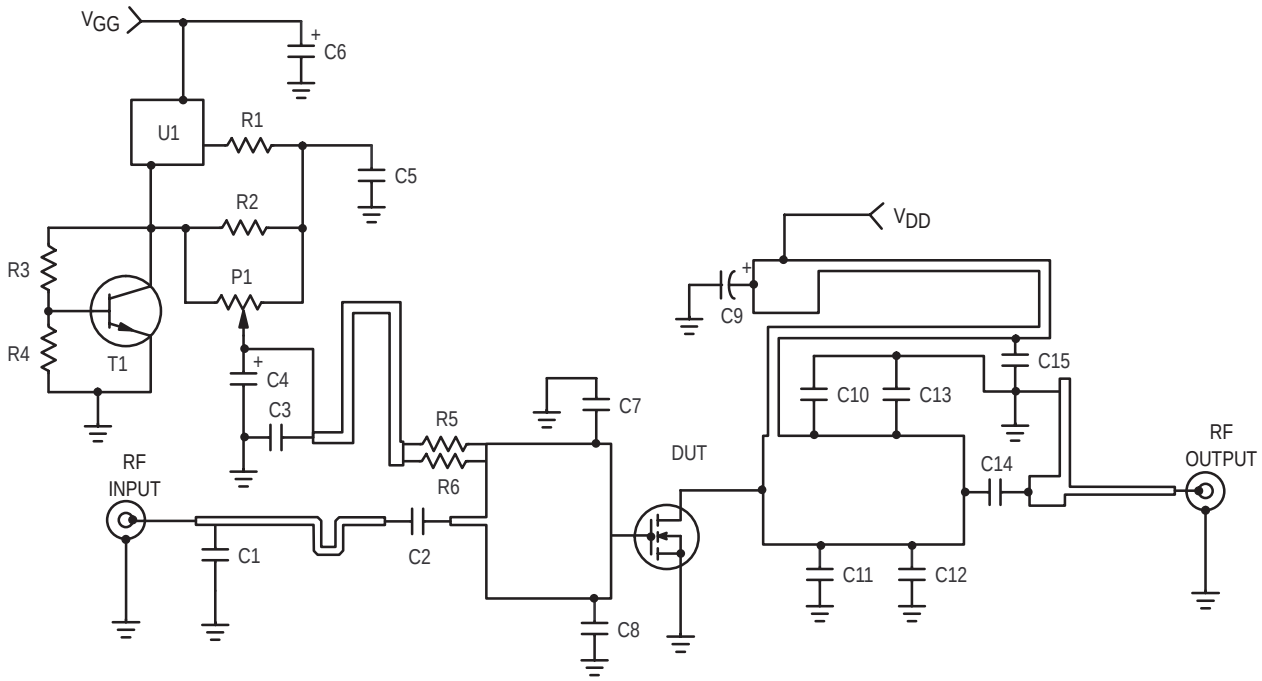


Figure 1. Broadband GSM 900 Optimized Demo Board Schematic

Table 1. Broadband GSM 900 Optimized Demo Board Component Designations and Values

Designators	Description
C1	4.7 pF Chip Capacitor, ACCU–P (0805) AVX #08051J3R9CBT
C2	3.9 pF Chip Capacitor, ACCU–P (0805) AVX #08051J3R9CBT
C3, C15	22 pF Chip Capacitors, ACCU–P (0805) AVX #08051J221
C4, C6	22 μF, 35 V Tantalum Chip Capacitors, Kemet #T491X226K035AS4394
C5	1.0 μF Chip Capacitor, ACCU–P (0805) AVX #08053G105ZATEA
C7, C8	5.6 pF Chip Capacitors, ACCU–P (0805) AVX #08051J5R18CBT
C9	220 μF, 63 V Electrolytic Capacitor
C10, C11	3.3 pF Chip Capacitors, ACCU–P (0805) AVX #08051J8R2CBT
C12, C13	2.2 pF Chip Capacitors, ACCU–P (0805) AVX #08051J2R2CBT
C14	4.7 pF Chip Capacitor, ATC #100B
P1	5.0 kΩ Potentiometer CMS Cermet Multi–turn, Bourns #3224W
R1	10 Ω, 1/8 W Chip Resistor (0805)
R2	1.0 kΩ, 1/8 W Chip Resistor (0805)
R3	1.2 kΩ, 1/8 W Chip Resistor (0805)
R4	2.2 kΩ, 1/8 W Chip Resistor (0805)
R5, R6	1.0 kΩ, 1/8 W Chip Resistor (0805)
T1	Bipolar NPN Transistor, SOT–23, ON Semiconductor #BC847ALT1
U1	Voltage Regulator, Micro–8, ON Semiconductor #LP2951ACDM–5.0R2
	RF Connectors, Type SMA, Radial #R125510001
	Substrate = Taconic RF35, Thickness 0.5mm

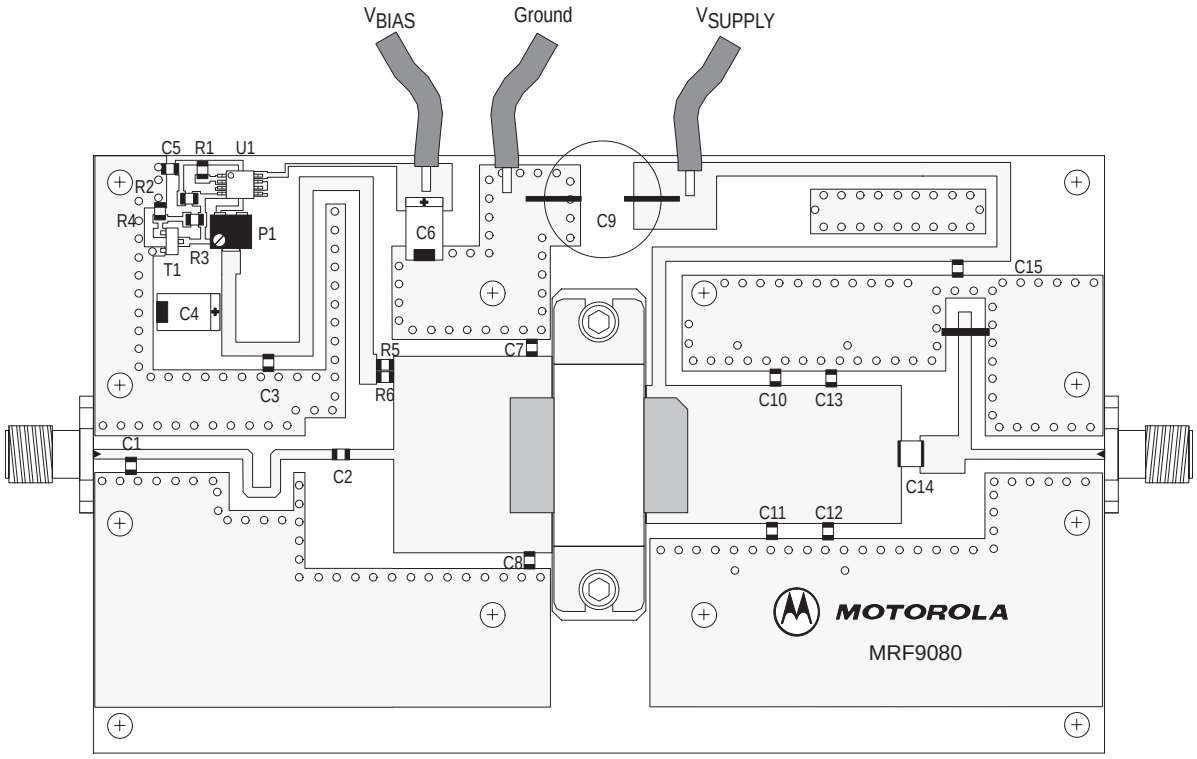


Figure 2. Broadband GSM 900 Optimized Demo Board Component Layout

TYPICAL CHARACTERISTICS
(IN MOTOROLA BROADBAND GSM 900 OPTIMIZED DEMO BOARD)

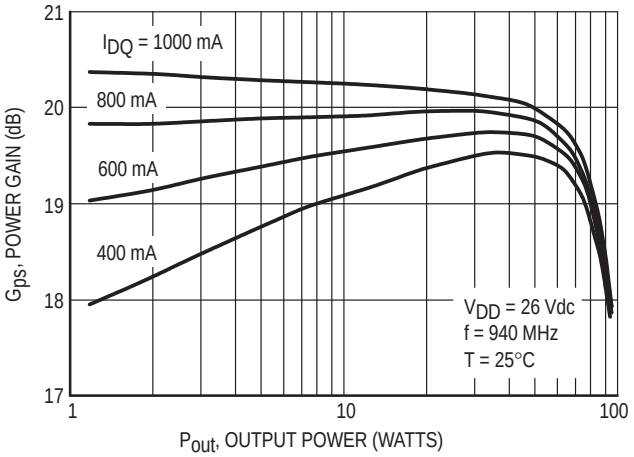


Figure 3. Power Gain versus Output Power

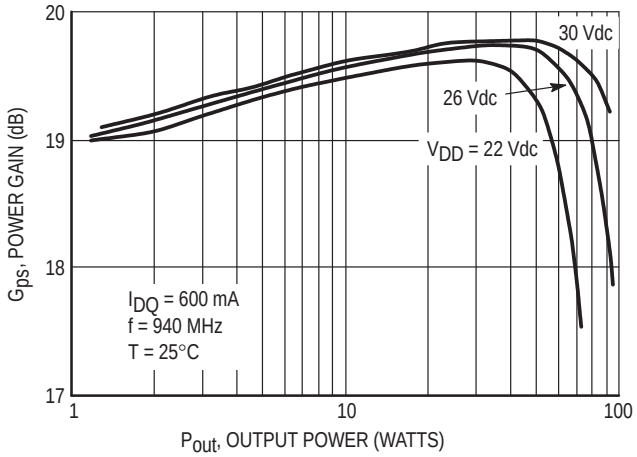


Figure 4. Power Gain versus Output Power

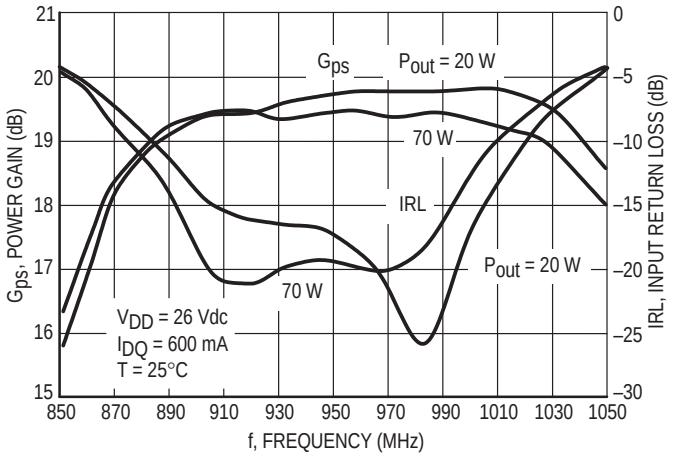


Figure 5. Power Gain and Input Return Loss versus Frequency

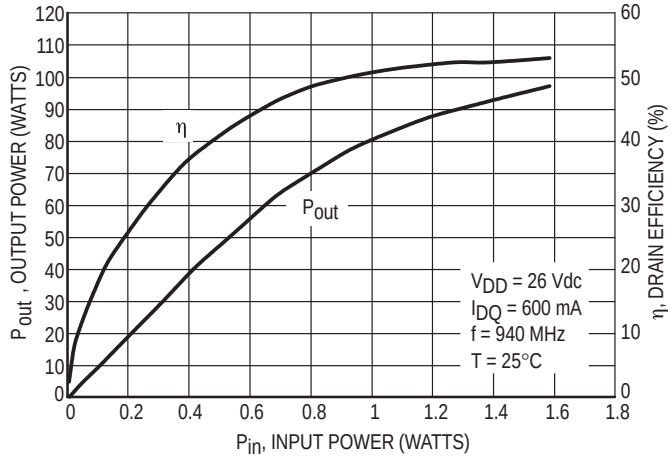


Figure 6. Output Power and Efficiency versus Input Power

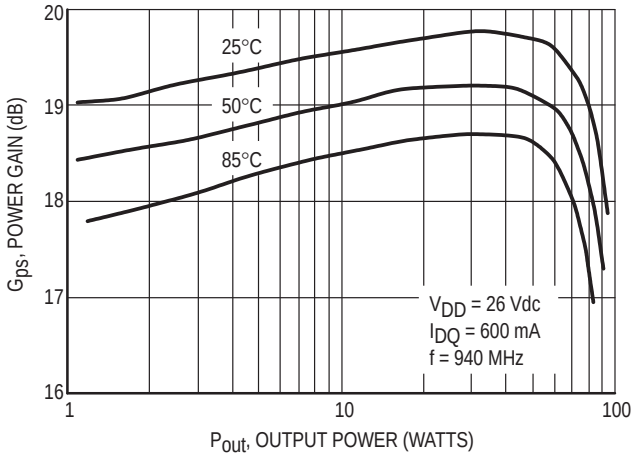


Figure 7. Power Gain versus Output Power

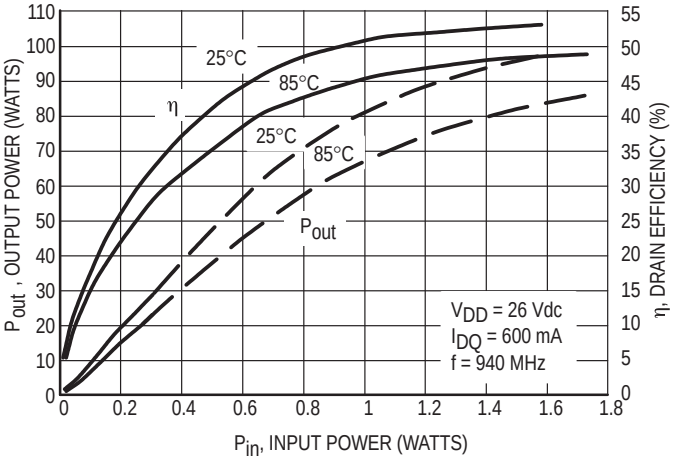
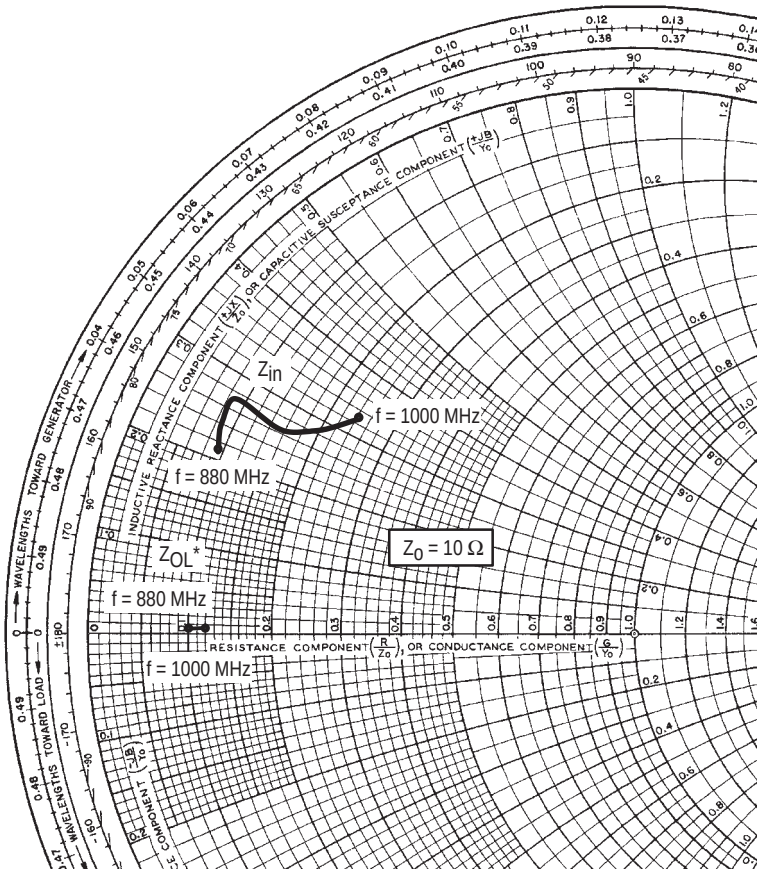


Figure 8. Output Power and Efficiency versus Input Power



V_{DD} = 26 V, I_{DQ} = 600 mA, P_{out} = 90 W (CW)

f MHz	Z_{in} Ω	Z_{OL}* Ω
880	0.91 + j2.11	1.22 + j0.12
920	0.88 + j2.65	1.00 + j0.16
960	1.6 + j2.61	1.22 + j0.22
1000	2.45 + j3.38	1.14 + j0.41

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power and drain efficiency.

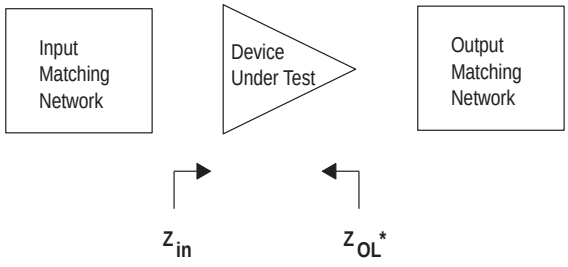
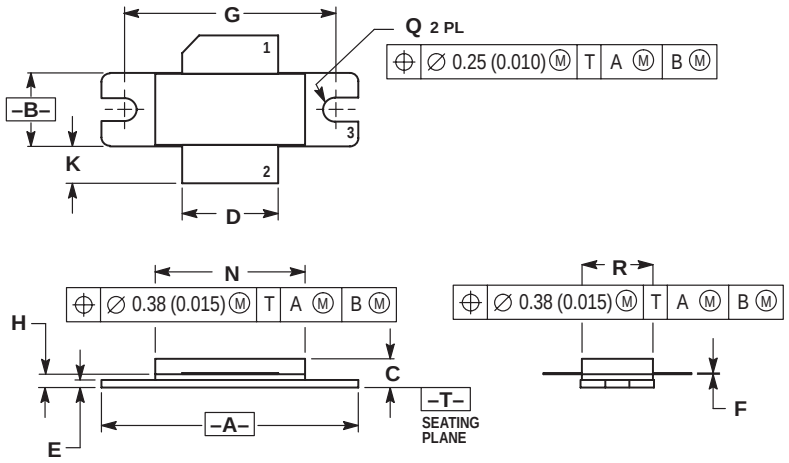


Figure 9. Series Equivalent Input and Output Impedance

PACKAGE DIMENSIONS

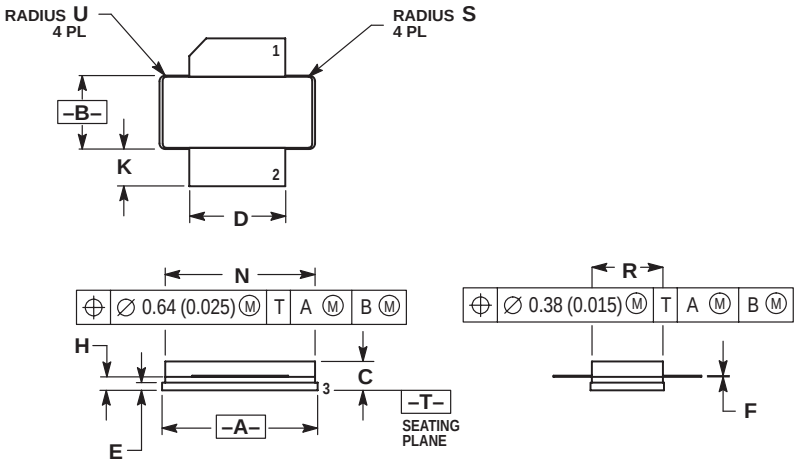


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030" AWAY FROM FLANGE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.055	0.065	1.40	1.65
K	0.170	0.210	4.32	5.33
N	0.772	0.788	19.60	20.00
Q	0.118	0.138	3.00	3.51
R	0.365	0.375	9.27	9.53

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465–04
ISSUE D
(MRF9080)



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	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.055	0.065	1.40	1.65
K	0.170	0.210	4.32	5.33
N	0.775	0.785	19.69	19.94
R	0.365	0.375	9.27	9.53
S	0.020 REF		0.51 REF	
U	0.030 REF		0.76 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
4. SOURCE

CASE 465A–04
ISSUE D
(MRF9080S)

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