SC4605
Low Input, High Efficiency Synchronous, Step Down Controller

Description

The SC4605 is a voltage mode step down (buck) regulator controller that provides accurate high efficiency power conversion from a input supply range of 2.8V to 5.5V. A high level of integration reduces external component count, and makes it suitable for low voltage applications where cost, size and efficiency are critical.

The SC4605 drives external N-channel MOSFETs with 1A peak current. A non-overlap protection is provided for the gate drive signals to prevent shoot through of the MOSFET pair. The voltage drop across the high side MOSFET during its conduction is sensed for lossless short circuit current limiting.

The quiescent supply current in sleep mode is typically lower than 10µA. A 1.8ms soft start is internally provided to prevent output voltage overshoot during start-up.

The SC4605 is an ideal choice for 3.3V, 5V or other low input supply systems. It's available in 10 pin MSOP package.

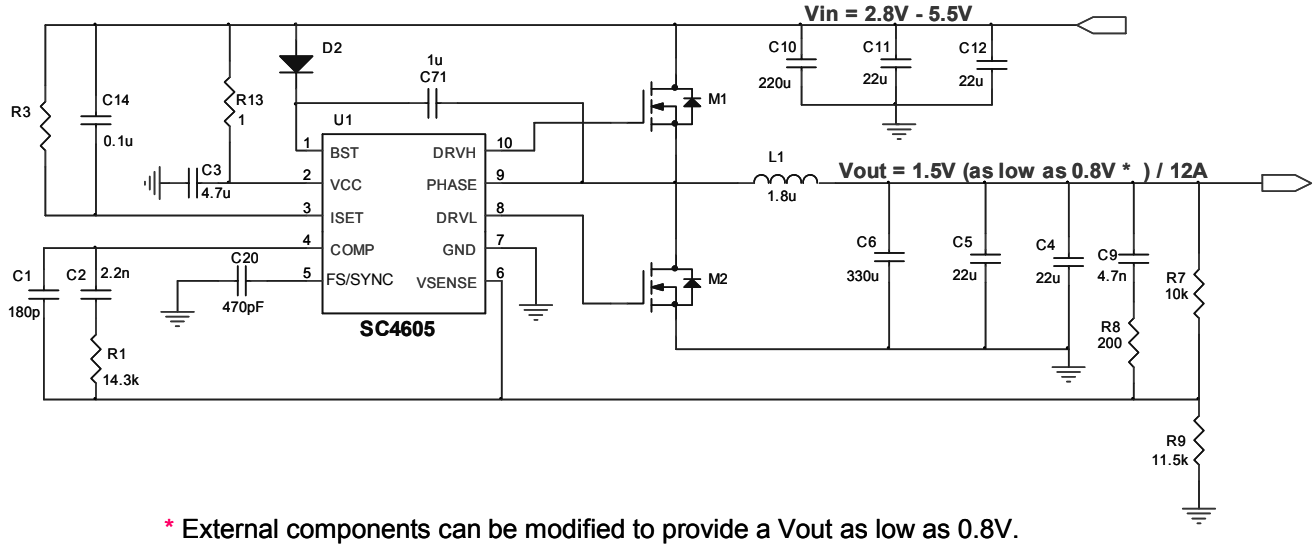
Features

- BICMOS voltage mode PWM controller
- 2.8V to 5.5V Input voltage range
- Output voltages as low as 0.8V
- +/-1% Reference accuracy
- Sleep mode (Icc = 10µA typ)
- Lossless adjustable short circuit current limiting
- Combination pulse by pulse & hiccup mode current limit
- High efficiency synchronous switching
- 0% to 97% Duty cycle range
- 1A Peak current driver
- 10-Pin MSOP package

Applications

- Distributed power architecture
- Servers/workstations
- Local microprocessor core power supplies
- DSP and I/O power supplies
- Battery powered applications
- Telecommunications equipment
- Data processing applications

Typical Application Circuit



* External components can be modified to provide a Vout as low as 0.8V.

Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Supply Voltage (V_{CC})		7	V
Output Drivers (DRVH, DRVL) Currents Continuous Peak		+/-0.25	A
		+/-1.00	A
Inputs (VSENSE, COMP, FS/SYNC, ISET)		-0.3 to 7	V
PHASE		-0.3 to 5.5	V
PHASE Pulse tpulse < 100ns		-2 to 7	V
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Junction Temperature Range	T_J	-55 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	+300	°C

All voltages with respect to GND. Currents are positive into, negative out of the specified terminal.

Electrical Characteristics

Unless otherwise specified, VCC = 5V, CT = 470pF, T_A = -40°C to 85°C, T_A = T_J.

Parameter	Test Conditions	Min	Typ	Max	Unit
Overall					
Supply Voltage		2.8		5.5	V
Supply Current, Sleep	FS/SYNC = 0V		10	15	µA
Supply Current, Bias	V_{CC} = 5.5V		1	3	mA
VCC Turn-on Threshold			2.7	2.8	V
VCC Turn-off Hysteresis			125		mV
Error Amplifier					
Input Voltage (Internal Reference)	T_A = 25°C	0.792	0.8	0.808	V
	V_{CC} = 2.8V ~ 5.5V, T_A = 25°C	0.788	0.8	0.812	
	Temperature	0.786	0.8	0.814	
VSENSE Bias Current			25		nA
Open Loop Gain (1)	V_{COMP} = 0.5 to 2.5V		80		dB
Unity Gain Bandwidth (1)			4		MHz
Slew Rate (1)			2		V/µs
VOUT High	I_{COMP} = -2mA	V_{CC} - 0.5	V_{CC} - 0.2		V
VOUT Low	I_{COMP} = 2mA		0.1	0.25	V

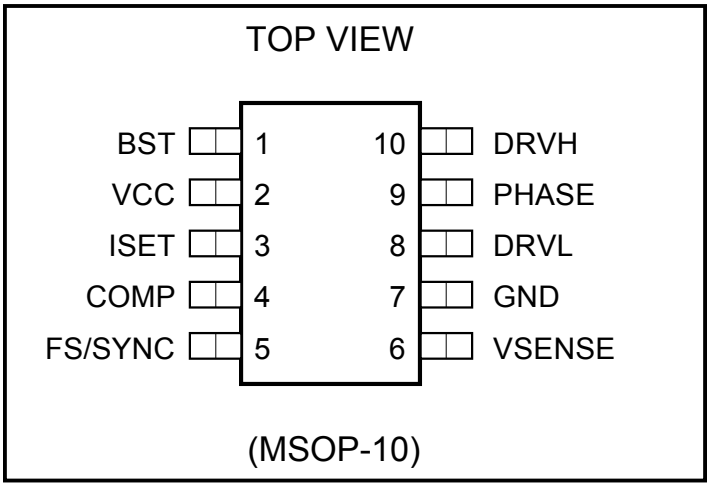
Electrical Characteristics (Cont.)

Unless otherwise specified, VCC = 5V, CT = 470pF, T_A = -40°C to 85°C, T_A = T_J.

Parameter	Test Conditions	Min	Typ	Max	Unit
Oscillator					
Initial Accuracy	T_A = 25°C	255	300	345	kHz
Minimum Operation Frequency (1)			100		kHz
Maximum Operation Frequency (1)			600		kHz
Ramp Peak to Valley (1)			1.5		V
Ramp Peak Voltage (1)			2.0		V
Ramp Valley Voltage (1)			0.5		V
Sleep, Soft Start, Current Limit					
Sleep Threshold	Measured at FS			0.2	V
Soft Start Time (1)			1.8		ms
ISET Bias Current	T_J = 25°C	-43	-50	-57	µA
Current Limit Blank Time (1)			150		ns
Gate Drive					
Duty Cycle		0		97	%
Peak Source (DRVH) (2)	Vgs = 5V, I_{SOURCE} = 100mA			3	Ω
Peak Sink (DRVH) (2)	Vgs = 5V, I_{SINK} = 100mA			3	Ω
Peak Source (DRVL) (2)	Vgs = 5V, I_{SOURCE} = 100mA			3	Ω
Peak Sink (DRVL) (2)	Vgs = 5V, I_{SINK} = 100mA			3	Ω
Output Rise Time (2)	Vgs = 5V, C_{OUT} = 4.7nF		35		ns
Output Fall Time (2)	Vgs = 5V, C_{OUT} = 4.7nF		35		ns
Minimum Non-Overlap (1)		30	40		ns

Notes:
(1). Guaranteed by design.
(2). Guaranteed by characterization.
(3) This device is ESD sensitive. Use of standard ESD handling precautions is required.

Pin Configuration



Ordering Information

Part Number (1)	Device
SC4605IMSTR	MSOP-10
SC4605IMSTRT (2)	

Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

VCC: Positive supply rail for the IC. Bypass this pin to GND with a 0.1 to 4.7µF low ESL/ESR ceramic capacitor.

GND: All voltages are measured with respect to this pin. All bypass and timing capacitors connected to GND should have leads as short and direct as possible.

FS/SYNC: A capacitor from FS pin to GND sets the PWM oscillator frequency. Use a high quality ceramic capacitor with low ESL and ESR for best result. A minimum capacitor value of 200pF ensures good accuracy and less susceptibility to circuit layout parasitics. When the FS is pulled and held below 0.2V, its sleep mode operation is invoked. The Sleepmode supply current is 10µA typical. The oscillator and PWM are designed to provide practical operation up to 600kHz. In synchronous mode operation, a low value resistor has to be connected between ground and the timing capacitor. An external clock is then feed into the resistor capacitor junction to override the internal clock.

VSENSE: This pin is the inverting input of the voltage amplifier and serves as the output voltage feedback point for the Buck converter. It senses the output voltage through an external divider.

COMP: This is the output of the voltage amplifier. The voltage at this output is inverted internally and connected to the non-inverting input of the PWM comparator. A lead-lag network around the voltage amplifier compensates for the two pole LC filter characteristic inherent to voltage mode control and is required in order to optimize the dynamic performance of the voltage mode control loop.

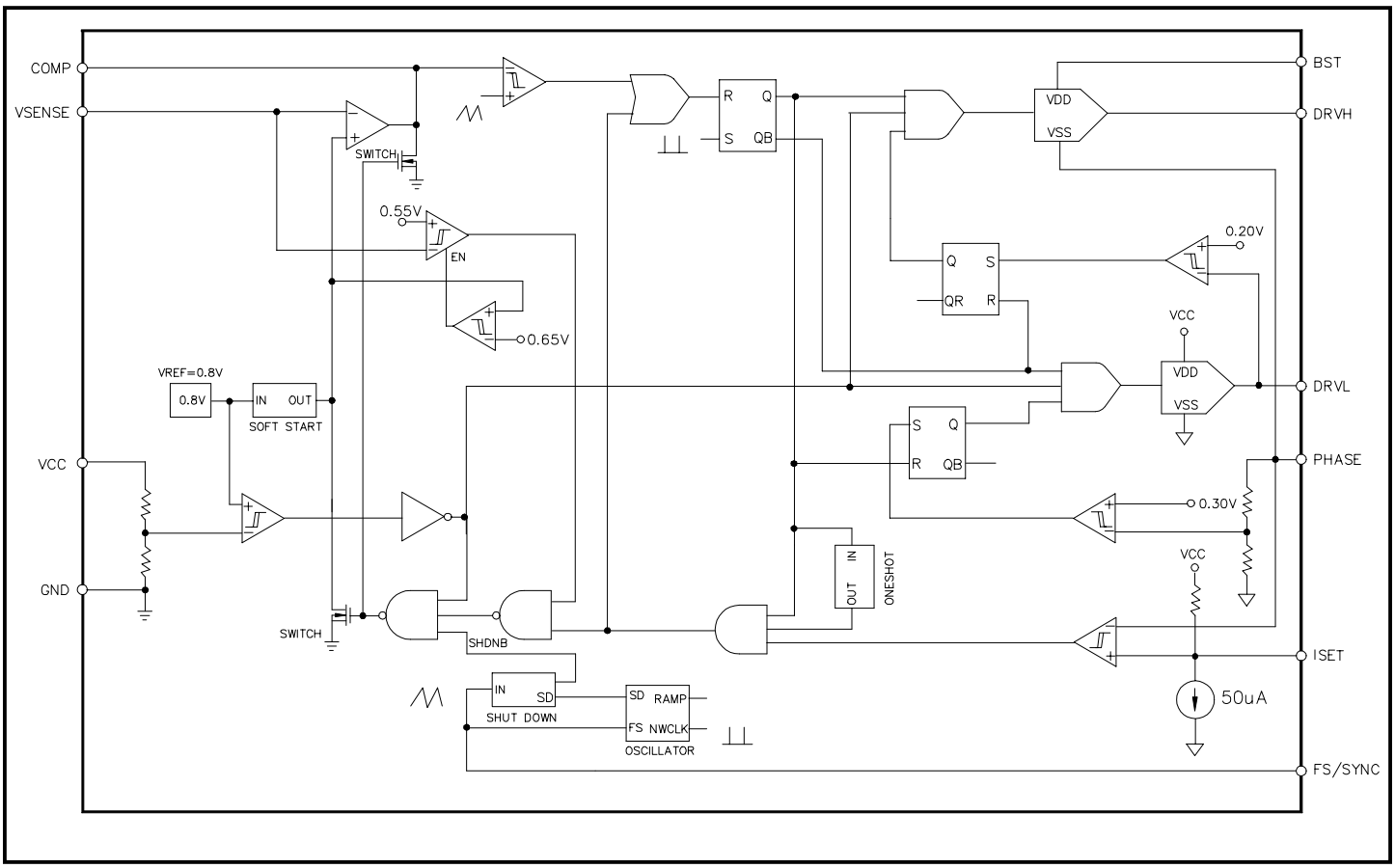
ISET / PHASE: PHASE is connected to the junction between the two external power MOSFET transistors. The voltage drop across the high side MOSFET during its conduction is compared with the voltage drop generated by the internal 50µA current source and the external current limit resistor connected between PHASE and Vin, and forms the current limit comparator and logic sets the PWM latch and terminates the output pulse. If the converter output voltage drops below 68.75% of its nominal voltage, the controller stops switching and goes through a soft start sequence. This prevents excess power dissipation in the low side MOSFET during a short circuit. The current limit threshold is set by the external resistor between VCC and ISET.

BST: This pin connects the external charge pump, and powers the high side MOSFET gate drive.

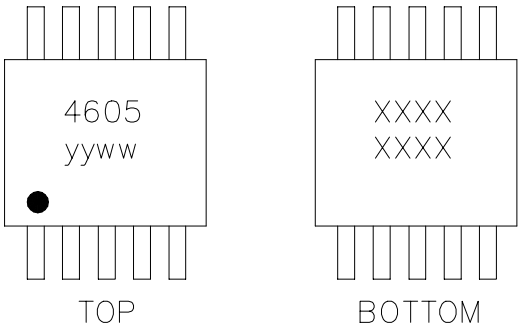
DRVH, DRVL: The output drivers are rated for 1A peak currents. The PWM circuitry provides complementary drive signals to the output stages. The cross conduction of the external MOSFETs is prevented by monitoring the voltage on the driver pins of the MOSFET pair in conjunction with a time delay optimized for FET turn-off characteristics.

POWER MANAGEMENT

Block Diagram



Marking Information



yyww = Datecode (Example: 0012)
xxxx = Semtech Lot # (Example: E901
xxxx 01-1)

Applications Information

Enable

Pulling and holding the FS/SYNC pin below 0.2V initializes the SLEEP mode of the SC4605 with its typical SLEEP mode supply current of 10µA. During the SLEEP mode, the high side and low side MOSFETs are turned off and the internal soft start voltage is held low.

Oscillator

The oscillator uses an external capacitor between FS and GND to set the oscillation frequency. The ramp waveform is a triangle at the PWM frequency with a peak voltage of 2V and a valley voltage of 0.5V. The PWM duty ratio is limited to a maximum of 97%, which allows the bootstrap capacitor to be charged during each cycle. The capacitor tolerance adds to the accuracy of the oscillator frequency. The approximate operating frequency is determined by the external capacitor connected to the FS/SYNC pin as shown below:

$$f_s = \frac{1.55 \cdot 10^{-4}}{C_T}$$

In its synchronous mode, a low value resistor needs to be connected between ground and the frequency setting capacitor, CT. Then an external clock connects to the junction of the resistor and the capacitor to activate its synchronous mode. The frequency of the clock can be used up to 700kHz. This external clock signal should have a duty cycle from 5% to 10% and the peak voltage at the junction from the clock signal should be about 0.2V.

UVLO

When the FS/SYNC pin is not pulled and held below 0.2V, the voltage on the Vcc pin determines the operation of the SC4605. As Vcc increases during start up, the UVLO block senses Vcc and keeps the high side and low side MOSFETs off and the internal soft start voltage low until Vcc reaches 2.8V. If no faults are present, the SC4605 will initiate a soft start when Vcc exceeds 2.8V. A hysteresis (150mV) in the UVLO comparator provides noise immunity during its start up.

Soft Start

The soft start function is required for step down controllers to prevent excess inrush current through the DC bus during start up. Generally this can be done by sourcing a controlled current into a timing capacitor and then using the voltage across this capacitor to slowly ramp up the error amp reference. The closed loop creates narrow width driver pulses while the output voltage is low and allows these pulses to increase to their steady state duty cycle as the output voltage reaches its regulated value. With this, the inrush current from the input side is controlled. The duration of the soft start in the SC4605 is controlled by an internal timing circuit which is used during start up and over current to set the hiccup time. The soft start time can be calculated by:

$$T_{SOFT\_START} = \frac{720}{f_s}$$

As can be seen here, the soft start time is switching frequency dependant. For example, if fs = 300kHz, TSOFT_START = 720/300k = 2.4ms. But if fs = 600kHz, TSOFT_START = 720/600k = 1.2ms.

The SC4605 implements its soft start by ramping up the error amplifier reference voltage providing a controlled slew rate of the output voltage, then preventing overshoot and limiting inrush current during its start up.

Over Current Protection

Over current protection for the SC4605 is implemented by detecting the voltage drop of the high side N-MOSFET during its conduction, also known as high side RDS(ON) detection. This loss-less detection eliminates the sense resistor and its loss. The overall efficiency is improved and the number of components and cost of the converter are reduced. RDS(ON) sensing is by default inaccurate and is mainly used to protect the power supply during a fault case. The over current trigger point will vary from unit to unit as the RDS(ON) of N-MOSFET varies. Even for the same unit, the over current trigger point will vary as the junction temperature of N-MOSFET varies. The SC4605 provides a built-in 50µA current source, which is combined with RSET (connected between VCC and ISET) to determine the current limit threshold. The value of RSET can be properly selected according to the desired current limit point IMAX and the internal 50µA pull down current available on the ISET pin based on the following expression:

Applications Information (Cont.)

$$R_{SET} = \frac{I_{MAX} \cdot R_{DS(ON)}}{50\mu A}$$

Kelvin sensing connections should be used at the drain and source of N-MOSFET. R_{SET} needs to be adjusted if the input of the application changes significantly, say from 3.3V to 5V for the same load and same output voltage. A 0.1µA ceramic capacitor paralled to this resistor should be used to decouple the noise.

The RDS(ON) sensing used in the SC4605 has an additional feature that enhances the performance of the over current protection. Because the RDS(ON) has a positive temperature coefficient, the 50µA current source has a positive coefficient of about 0.17%/C° providing first order correction for current sensing vs temperature. This compensation depends on the high amount of thermal transferring that typically exists between the high side N-MOSFET and the SC4605 due to the compact layout of the power supply.

When the converter detects an over current condition (I > IMAX) as shown in Figure 1, the first action the SC4605 takes is to enter the cycle by cycle protection mode (Point B to Point C), which responds to minor over current cases. Then the output voltage is monitored. If the over current and low output voltage (set at 68.75% of nominal output voltage) occur at the same time, the Hiccup mode operation (Point C to Point D) of the SC4605 is invoked and the internal soft start capacitor is discharged. This is like a typical soft start cycle.

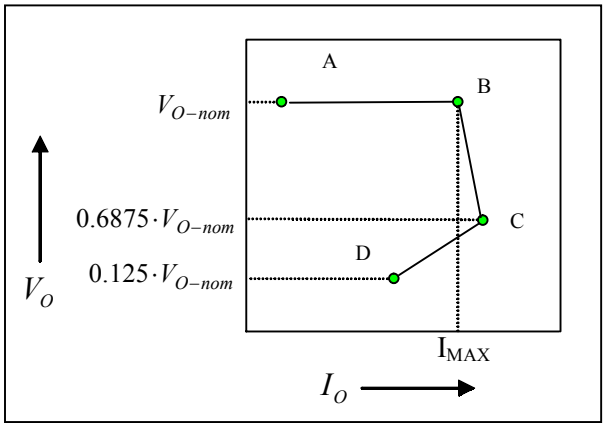


Figure 1. Over current protection characteristic of SC4605

Power MOSFET Drivers

The SC4605 has two drivers for external power N-MOSFETs. The driver block consists of one high side N-MOSFET, 1A driver, DRVH, and one low side 1A, N-MOSFET driver, DRVL, which are optimized for driving external power MOSFETs in a synchronous buck converter. The output drivers also have gate drive non-overlap mechanism that gives a dead time between DRVH and DRVL transitions to avoid potential shoot through problems in the external MOSFETs. By using the proper design and the appropriate MOSFETs, a 12A converter can be achieved. As shown in Figure 2, td1, the delay from the top MOSFET off to the bottom MOSFET on is adaptive by detecting the voltage of the phase node. td2, the delay from the bottom MOSFET off to the top MOSFET on is fixed, is 50ns for the SC4605. This control scheme guarantees avoiding the cross conduction or shoot through between two MOSFETs and minimizes the conduction loss in the bottom diode for high efficiency applications.

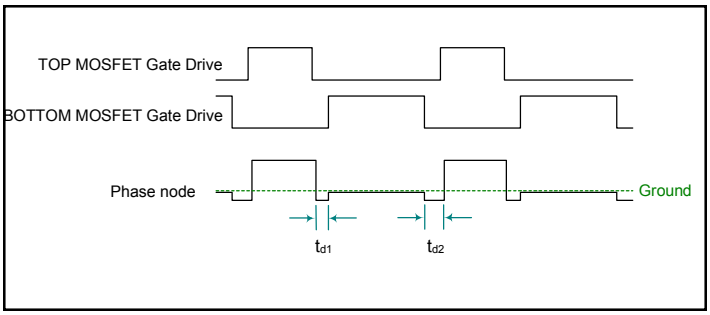


Figure 2. Timing Waveforms for Gate Drives and Phase Node

Inductor Selection

The factors for selecting the inductor include its cost, efficiency, size and EMI. For a typical SC4605 application, the inductor selection is mainly based on its value, saturation current and DC resistance. Increasing the inductor value will decrease the ripple level of the output voltage while the output transient response will be degraded. Low value inductors offer small size and fast transient responses while they cause large ripple currents, poor efficiencies and more output capacitance to smooth out the large ripple currents. The inductor should be able to handle the peak current without saturating and its copper resistance in the winding should be as low as possible to minimize its resistive power loss. A good trade-off among its size, loss and cost is to set the inductor ripple current to be within 15% to 30% of the maximum output current.

Applications Information (Cont.)

The inductor value can be determined according to its operating point and the switching frequency as follows:

$$L = \frac{V_O \cdot (V_I - V_O)}{V_I \cdot f_s \cdot \Delta I \cdot I_{OMAX}}$$

Where:
fs = switching frequency and
DI = ratio of the peak to peak inductor current to the maximum output load current.

The peak to peak inductor current is:

$$I_{P-P} = \Delta I \bullet I_{OMAX}$$

After the required inductor value is selected, the proper selection of the core material is based on the peak inductor current and efficiency requirements. The core must be able to handle the peak inductor current IPEAK without saturation and produce low core loss during the high frequency operation.

$$I_{PEAK} = I_{OMAX} + \frac{I_{p-p}}{2}$$

The power loss for the inductor includes its core loss and copper loss. If possible, the winding resistance should be minimized to reduce inductor's copper loss. The core loss can be found in the manufacturer's datasheet. The inductor' copper loss can be estimated as follows:

$$P_{COPPER} = I^2_{LRMS} \cdot R_{WINDING}$$

Where:
ILRMS is the RMS current in the inductor. This current can be calculated as follows:

$$I_{LRMS} = I_{OMAX} \cdot \sqrt{1 + \frac{1}{3} \cdot \Delta I^2}$$

Output Capacitor Selection

Basically there are two major factors to consider in selecting the type and quantity of the output capacitors. The first one is the required ESR (Equivalent Series Resistance) which should be low enough to reduce the voltage deviation from its nominal one during its load changes. The second one is the required capacitance, which should be high enough to hold up the output voltage. Before the SC4605 regulates the inductor current to a new value during a load transient, the output capacitor delivers all the additional current needed by the load. The ESR and ESL of the output capacitor, the loop parasitic inductance between the output capacitor and the load combined with inductor ripple current are all major contributors to the output voltage ripple. Surface mount speciality polymer aluminum electrolytic chip capacitors in UE series from Panasonic provide low ESR and reduce the total capacitance required for a fast transient response. POSCAP from Sanyo is a solid electrolytic chip capacitor that has a low ESR and good performance for high frequency with a low profile and high capacitance. Above mentioned capacitors are recommended to use in SC4605 applications.

Boost Capacitor Selection

The boost capacitor selection is based on its discharge ripple voltage, worst case condition time and boost current. The worst case conduction time T_W can be estimated as follows:

$$Tw = \frac{1}{f_s} \cdot D_{max}$$

Where:
f_S = the switching frequency and
Dmax = maximum duty ratio, 0.97 for the SC4605.

The required minimum capacitance for boost capacitor will be:

$$C_{boost} = \frac{I_B}{V_D} \cdot T_W$$

Where:
I_B = the boost current and
V_D = discharge ripple voltage

With f_S = 300kH, V_D = 0.3V and I_B = 50mA, the required capacitance for the boost capacitor is:

$$C_{boost} = \frac{I_B}{V_D} \cdot \frac{1}{f_s} \cdot D_{max} = \frac{0.05}{0.3} \cdot \frac{1}{300k} \cdot 0.97 = 540nF$$

Input Capacitor Selection

The input capacitor selection is based on its ripple current level, required capacitance and voltage rating. This capacitor must be able to provide the ripple current by the switching actions. For the continuous conduction

Applications Information (Cont.)

mode, the RMS value of the input capacitor can be calculated from:

$$I_{CIN(RMS)} = I_{OMAX} \cdot \sqrt{\frac{V_O \cdot (V_I - V_O)}{V^2_I}}$$

This current gives the capacitor's power loss as follows:

$$P_{CIN} = I^2_{CIN(RMS)} \cdot R_{CIN(ESR)}$$

This capacitor's RMS loss can be a significant part of the total loss in the converter and reduce the overall converter efficiency. The input ripple voltage mainly depends on the input capacitor's ESR and its capacitance for a given load, input voltage and output voltage. Assuming that the input current of the converter is constant, the required input capacitance for a given voltage ripple can be calculated by:

$$C_{IN} = I_{OMAX} \cdot \frac{D \cdot (1-D)}{fs \cdot (\Delta V_I - I_{OMAX} \cdot R_{CIN(ESR)})}$$

Where:
D = VO/VI , duty ratio and
DVI = the given input voltage ripple.
Because the input capacitor is exposed to the large surge current, attention is needed for the input capacitor. If tantalum capacitors are used at the input side of the converter, one needs to ensure that the RMS and surge ratings are not exceeded. For generic tantalum capacitors, it is wise to derate their voltage ratings at a ratio of 2 to protect these input capacitors.

Power Mosfet Selection

The SC4605 can drive an N-MOSFET at the high side and an N-MOSFET synchronous rectifier at the low side. The use of the high side N-MOSFET will significantly reduce its conduction loss for high current. For the top MOSFET, its total power loss includes its conduction loss, switching loss, gate charge loss, output capacitance loss and the loss related to the reverse recovery of the bottom diode, shown as follows:

$$P_{TOP\_TOTAL} = I^2_{TOP\_RMS} \cdot R_{TOP\_ON} + \frac{I_{TOP\_PEAK} \cdot V_I \cdot f_s}{V_{GATE} / R_G} \cdot (Q_{GD} + Q_{GS2}) + Q_{GT} \cdot V_{GATE} \cdot f_s + (Q_{OSS} + Q_{rr}) \cdot V_I \cdot f_s$$

Where:
RG = gate drive resistor,
QGD = the gate to drain charge of the top MOSFET,
QGS2 = the gate to source charge of the top MOSFET,
QGT = the total gate charge of the top MOSFET,
QOSS = the output charge of the top MOSFET and
Qrr = the reverse recovery charge of the bottom diode.

For the top MOSFET, it experiences high current and high voltage overlap during each on/off transition. But for the bottom MOSFET, its switching voltage is the bottom diode's forward drop during its on/off transition. So the switching loss for the bottom MOSFET is negligible. Its total power loss can be determined by:

$$P_{BOT\_TOTAL} = I^2_{BOT\_RMS} \cdot R_{BOT\_ON} + Q_{GB} \cdot V_{GATE} \cdot f_s + I_{D\_AVG} \cdot V_F$$

Where:
QGB = the total gate charge of the bottom MOSFET and
VF = the forward voltage drop of the bottom diode.

For a low voltage and high output current application such as the 3.3V/1.5V@12A case, the conduction loss is often dominant and selecting low RDS(ON) MOSFETs will noticeably improve the efficiency of the converter even though they give higher switching losses.

The gate charge loss portion of the top/bottom MOSFET's total power loss is derived from the SC4605. This gate charge loss is based on certain operating conditions (fs, VGATE, and I_0).

The thermal estimations have to be done for both MOSFETs to make sure that their junction temperatures do not exceed their thermal ratings according to their total power losses PTOTAL, ambient temperature Ta and their thermal resistance Rθja as follows:

$$T_{j(max)} < T_a + \frac{P_{TOTAL}}{R_{\theta ja}}$$

Applications Information (Cont.)

Loop Compensation Design

For a DC/DC converter, it is usually required that the converter has a loop gain of a high cross-over frequency for fast load response, high DC and low frequency gain for low steady state error, and enough phase margin for its operating stability. Often one can not have all these properties at the same time. The purpose of the loop compensation is to arrange the poles and zeros of the compensation network to meet the requirements for a specific application.

The SC4605 has an internal error amplifier and requires the compensation network to connect among the COMP pin and VSENSE pin, GND, and the output as shown in Figure 3. The compensation network includes C1, C2, R1, R7, R8 and C9. R9 is used to program the output voltage according to:

$$V_O = 0.8 \cdot (1 + \frac{R_7}{R_9})$$

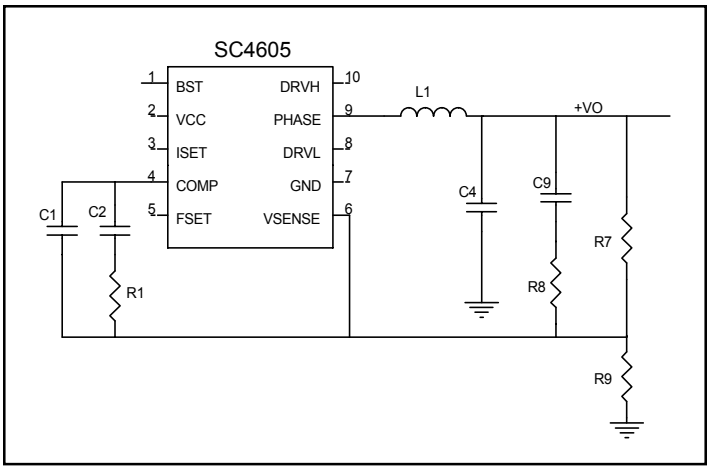


Figure 3. Compensation network provides 3 poles and 2 zeros.

For voltage mode step down applications as shown in Figure 3, the power stage transfer function is:

$$G_{VD}(s) = V_I \frac{1 + \frac{s}{\frac{1}{R_C \cdot C_4}}}{1 + s\frac{L_1}{R} + s^2 L_1 C_4}$$

Where:
R = load resistance and
R_C = C_4's ESR.

The compensation network will have the characteristic as follows:

$$G_{COMP}(s) = \frac{\omega_I}{s} \cdot \frac{1 + \frac{s}{\omega_{Z1}}}{1 + \frac{s}{\omega_{P1}}} \cdot \frac{1 + \frac{s}{\omega_{Z2}}}{\cdot 1 + \frac{s}{\omega_{P2}}}$$

Where;

$$\omega_I = \frac{1}{R_7 \cdot (C_1 + C_2)}$$

$$\omega_{Z1} = \frac{1}{R_1 \cdot C_2}$$

$$\omega_{Z2} = \frac{1}{(R_7 + R_8) \cdot C_9}$$

$$\omega_{P1} = \frac{C_1 + C_2}{R_1 \cdot C_1 \cdot C_2}$$

$$\omega_{P2} = \frac{1}{R_8 \cdot C_9}$$

After the compensation, the converter will have the following loop gain:

$$T(s) = G_{PWM} \cdot G_{COMP}(s) \cdot G_{VD}(s) =$$

$$\frac{\frac{1}{V_M} \cdot \omega_I \cdot V_I}{s} \cdot \frac{1 + \frac{s}{\omega_{Z1}}}{1 + \frac{s}{\omega_{P1}}} \cdot \frac{1 + \frac{s}{\omega_{Z2}}}{\cdot 1 + \frac{s}{\omega_{P2}}} \cdot \frac{1 + \frac{s}{\frac{1}{R_C \cdot C_4}}}{1 + s\frac{L}{R} + s^2 LC}$$

Where:
G_{PWM} = PWM gain
V_M = 1.5V, ramp peak to valley voltage of SC4605

Applications Information (Cont.)

The design guidelines for the SC4605 applications are as following:

1. Set the loop gain crossover corner frequency ω_c for given switching corner frequency $\omega_s = 2\pi f_s$,
2. Place an integrator at the origin to increase DC and low frequency gains,
3. Select ω_{z1} and ω_{z2} such that they are placed near ω_0 to damp the peaking and the loop gain has a -20dB/dec rate to go across the 0dB line for obtaining a wide bandwidth,
4. Cancel the zero from C_4's ESR by a compensator pole ω_{P1} ($\omega_{P1} = \omega_{ESR} = 1/(R_C C_4)$),
5. Place a high frequency compensator pole ωp_2 ($\omega p_2 = \pi f_s$) to get the maximum attenuation of the switching ripple and high frequency noise with the adequate phase lag at ω_c.

The compensated loop gain will be as given in Figure 4:

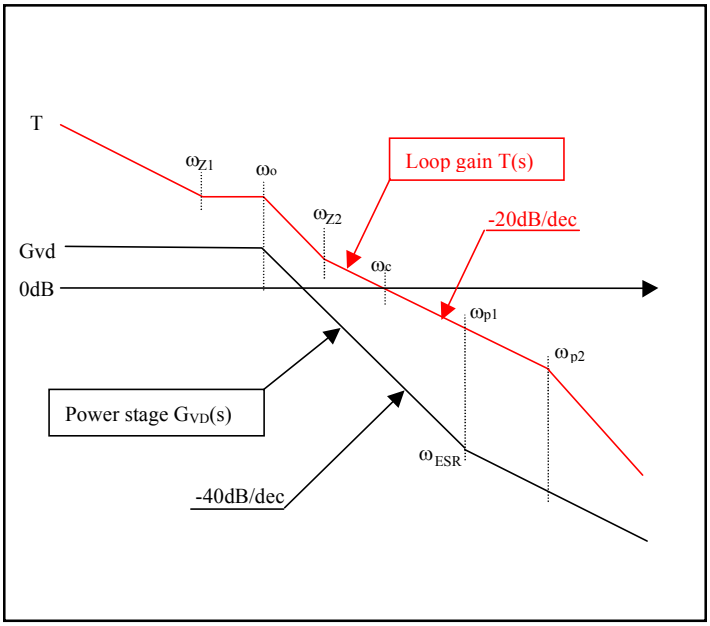


Figure 4. Asymptotic diagrams of power stage and its loop gain

Layout Guideline

In order to achieve optimal electrical, thermal and noise performance for high frequency converters, special attention must be paid to the PCB layouts. The goal of layout optimization is to identify the high di/dt loops and minimize them. The following guideline should be used to ensure proper functions of the converters.

1. A ground plane is recommended to minimize noises and copper losses, and maximize heat dissipation.
2. Start the PCB layout by placing the power components first. Arrange the power circuit to achieve a clean power flow route. Put all the connections on one side of the PCB with wide copper filled areas if possible.
3. The Vcc bypass capacitor should be placed next to the Vcc and GND pins.
4. The trace connecting the feedback resistors to the output should be short, direct and far away from the noise sources such as switching node and switching components.
5. Minimize the traces between DRVH/DRVL and the gates of the MOSFETs to reduce their impedance to drive the MOSFETs.
6. Minimize the loop including input capacitors, top/bottom MOSFETs. This loop passes high di/dt current. Make sure the trace width is wide enough to reduce copper losses in this loop.
7. ISET and PHASE connections to the top MOSFET for current sensing must use Kelvin connections.
8. Maximize the trace width of the loop connecting the inductor, bottom MOSFET and the output capacitors.
9. Connect the ground of the feedback divider and the compensation components directly to the GND pin of the SC4605 by using a separate ground trace. Then connect this pin to the ground of the output capacitor as close as possible.

Design Example 1: 3.3V to 1.5V @ 12A application with SC4605 (NH020 footprint)

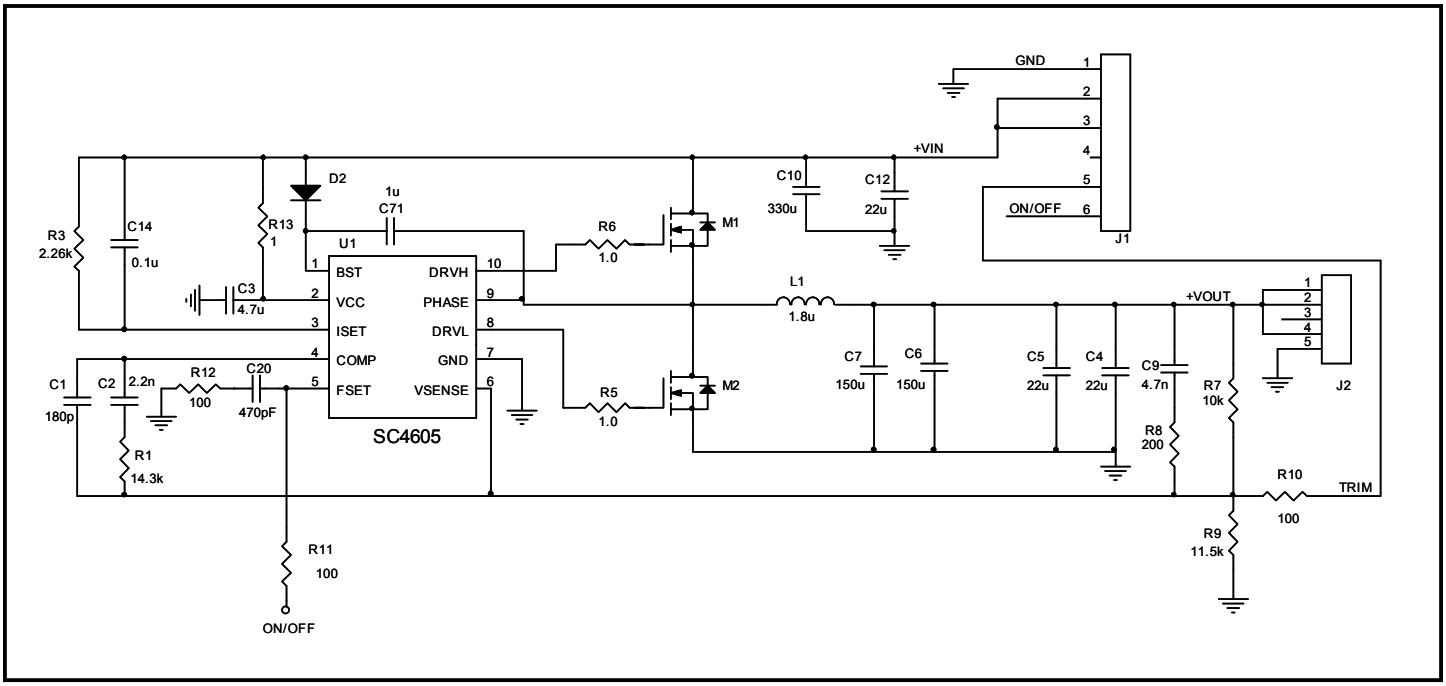


Figure 5. Schematic for 3.3V/1.5V@12A with SC4605 application

Design Example 2: 5V to 1.5V @ 12A application with SC4605 (NH020 footprint)

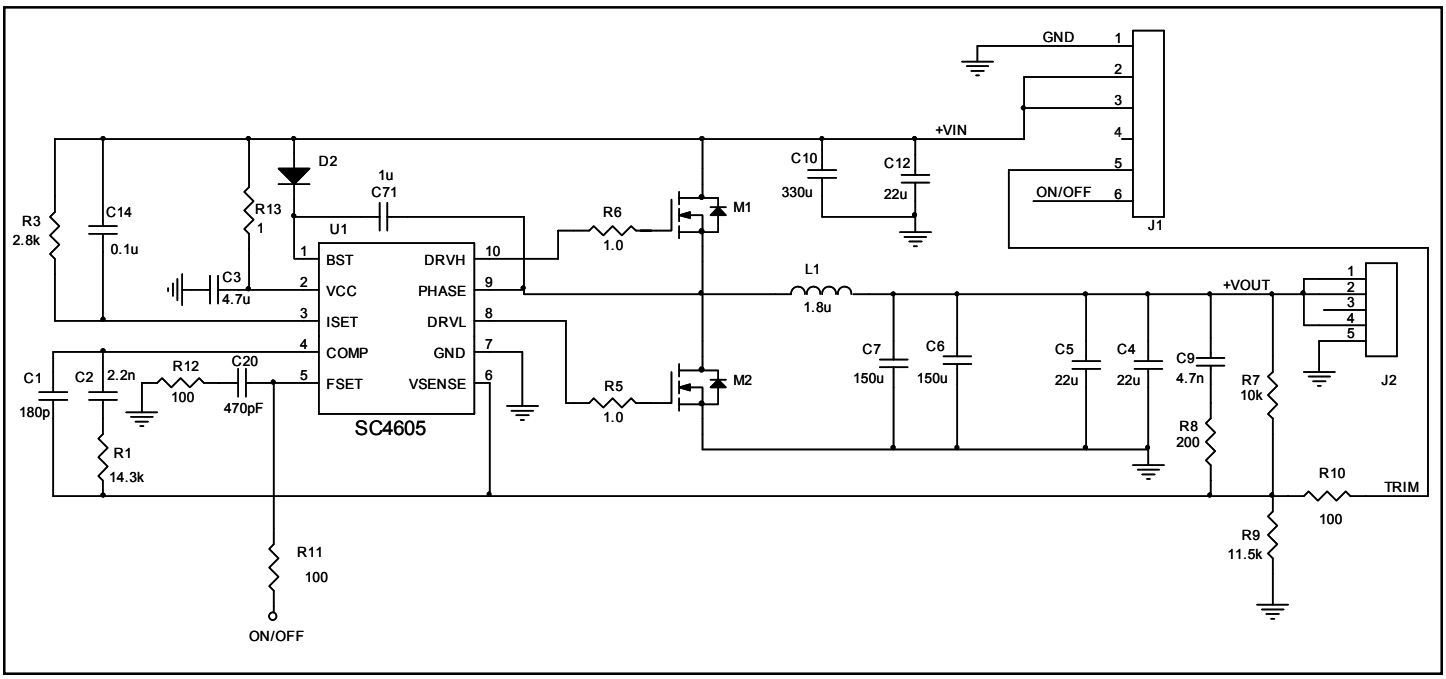


Figure 6. Schematic for 5V/1.5V@12A with SC4605 application

Design Example 3: 3.3V to 1.5V @ 15A application with SC4605 and its typical efficiency characteristics.

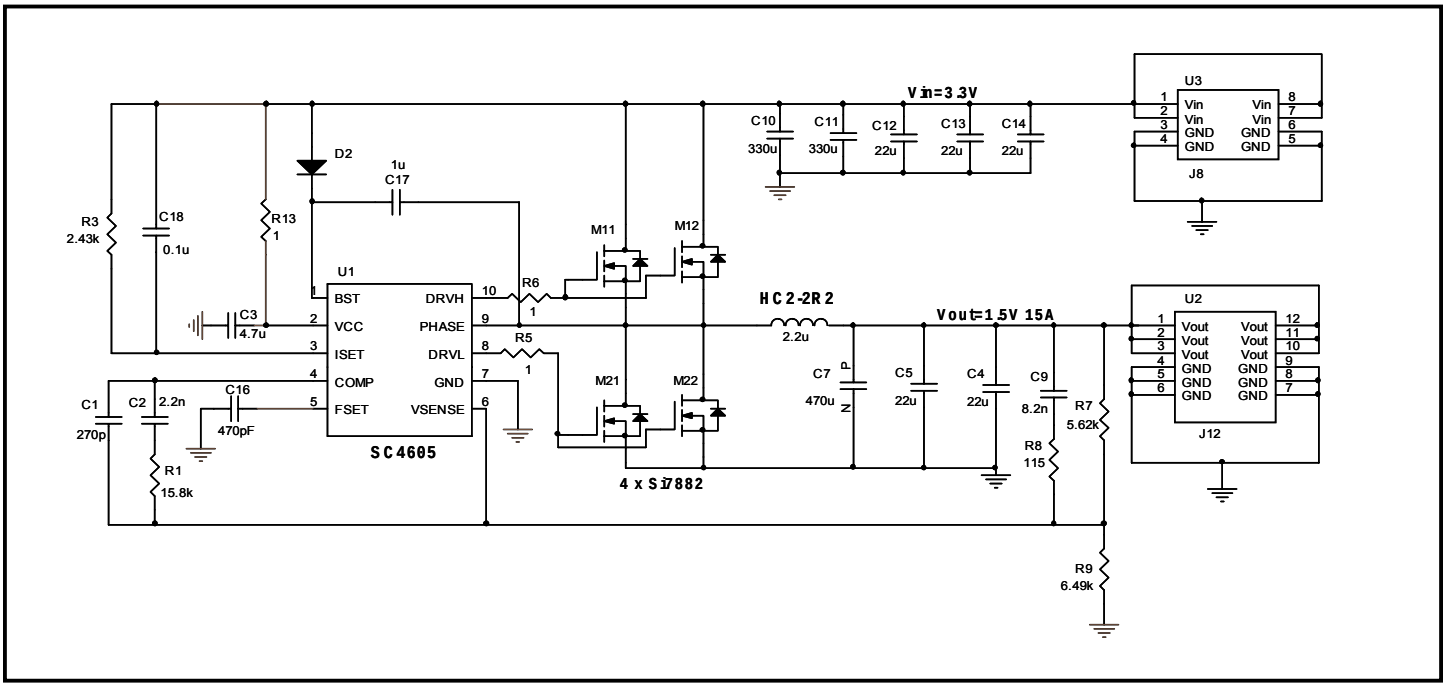
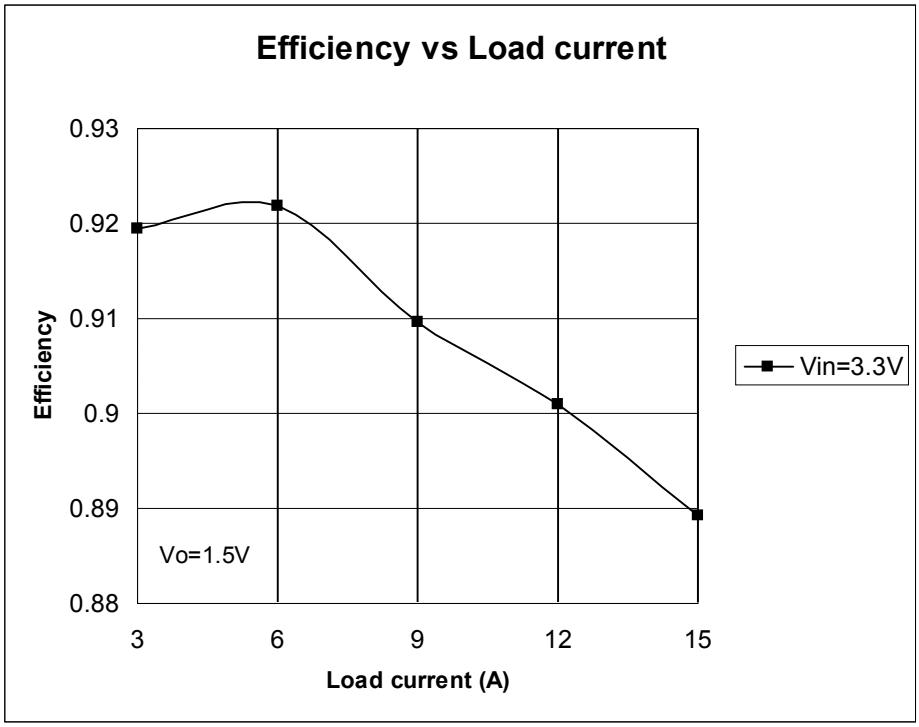


Figure 7. Schematic for 3.3V/1.5V @ 15A with SC4605 application



Applications Information (Cont.)

Design Example 4: 5V to 3.3V @ 5A application with SC4605 and its typical efficiency characteristics.

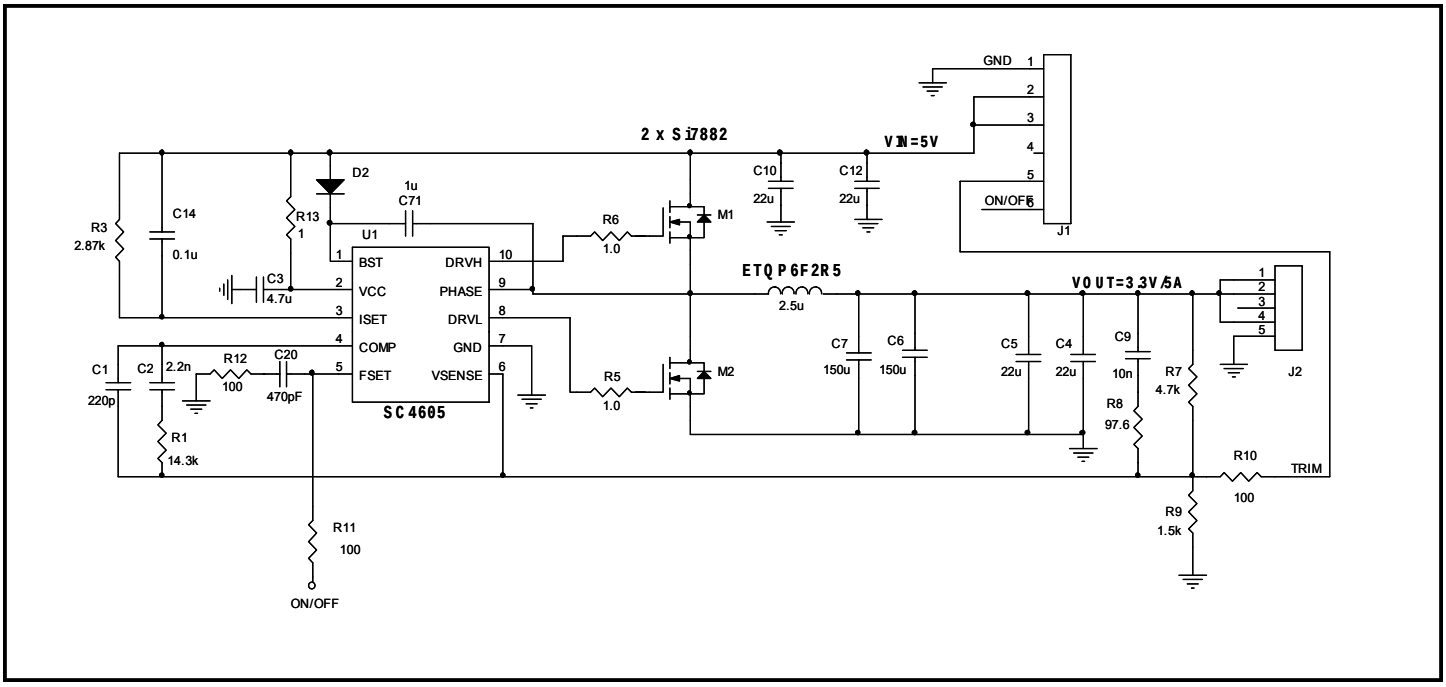
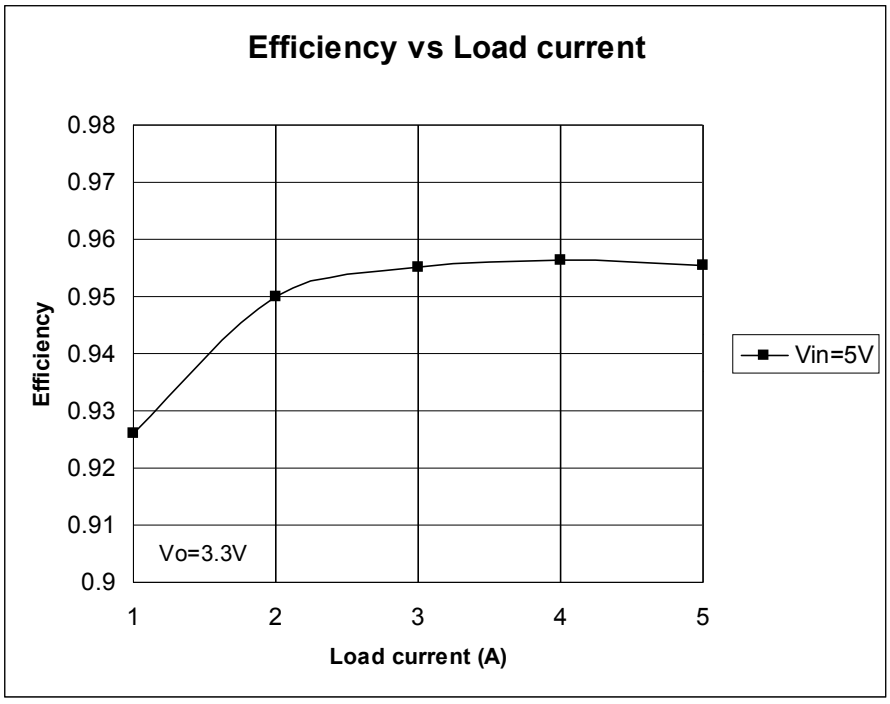


Figure 8. Schematic for 5V/3.3V@ 5A with SC4605 application



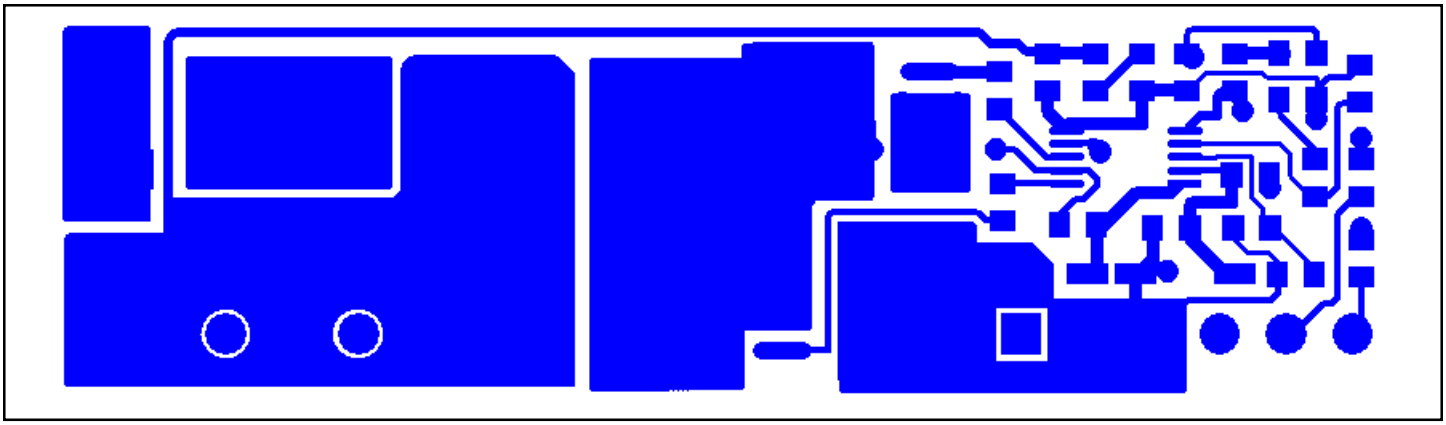
Bill of Materials - 3.3V to 1.5V @ 12A

Item	Qty	Reference	Value	Part No./Manufacturer
1	1	C1	180pF	
2	1	C2	2.2nF	
3	1	C3	4.7uF, 0805	
4	1	C71	1uF	
5	3	C4, C5, C12	22uF, 1210	TDK P/N: C3225X5R0J226M
6	2	C6, C7	150uF, 2870	Sanyo P/N: 4TPB150ML
7	1	C9	4.7nF	
8	1	C10	330uF, 2870	Sanyo P/N: 6TPB330ML
9	1	C14	0.1uF	
10	1	C20	470pF	
11	1	D2	MBR0520LT1, SOD-123	ON Semiconductor
14	1	L1	Inductor, 1.8uF	Panasonic. P/N: ETQP6F1R8BFR
15	2	M1, M2	Powerpack, SO-8	Vishay P/N: Si7858DP
16	1	R1	14.3k	
17	1	R3	2.32k	
18	2	R5, R6	1.0	
19	1	R7	10k	
20	1	R8	200	
21	1	R9	11.5k	
22	3	R10, R11, R12	100	
23	1	R13	1	
24	1	U1	SC4605	Semtech P/N: SC4605IMSTR

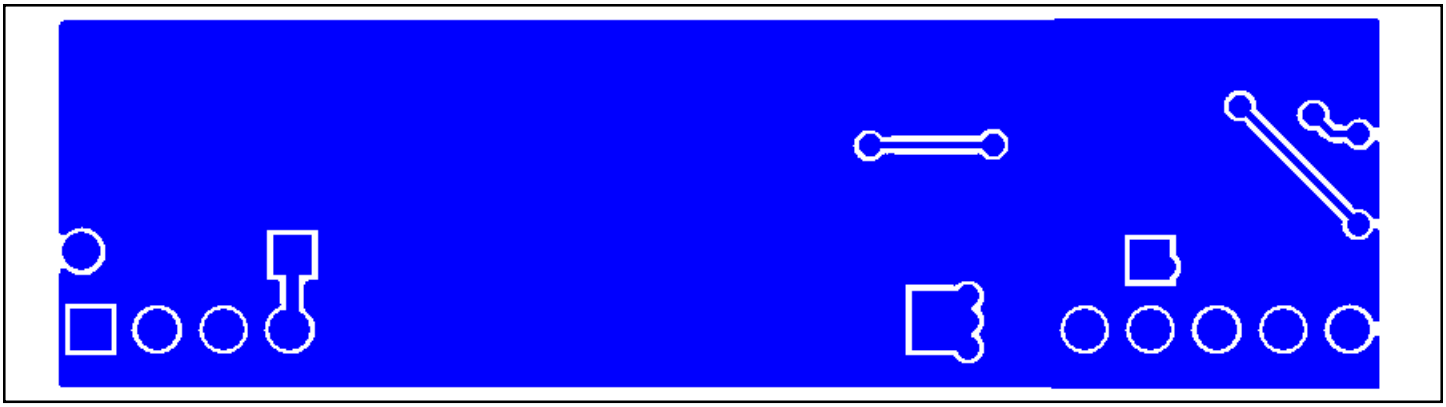
Unless specified, all resistors have 1% precision with 0603 package.
Capacitors will have 20% percision with 0603 package.
For R9, there are 3 kinds of values for different output cases.

PCB Layout - 3.3V to 1.5V @ 12A

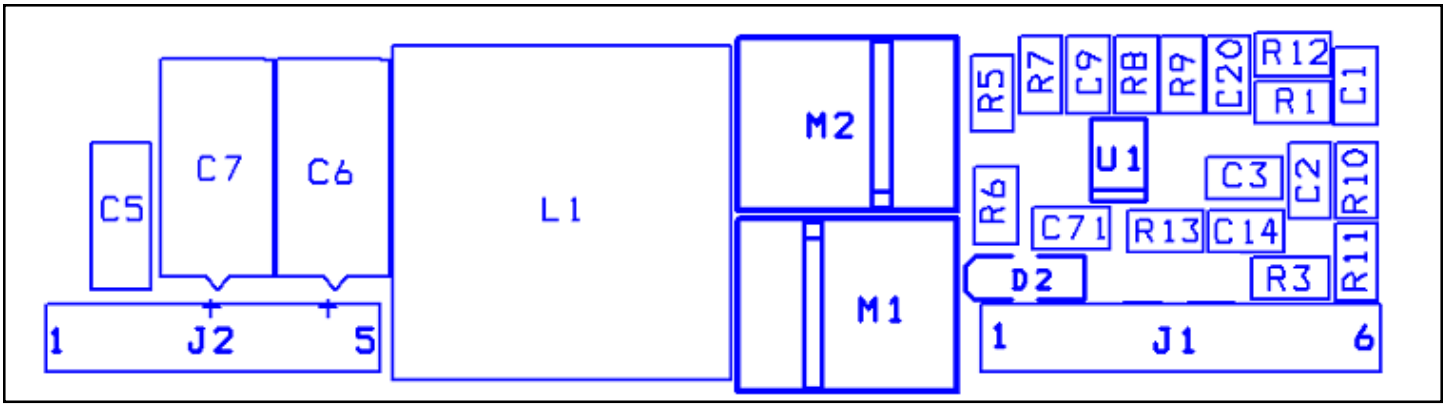
Top



Bottom



Top



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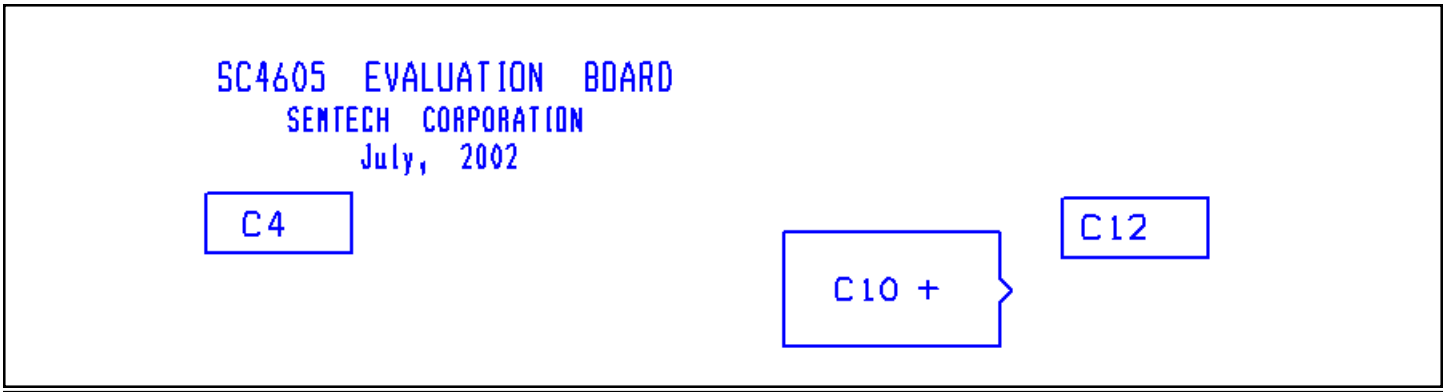
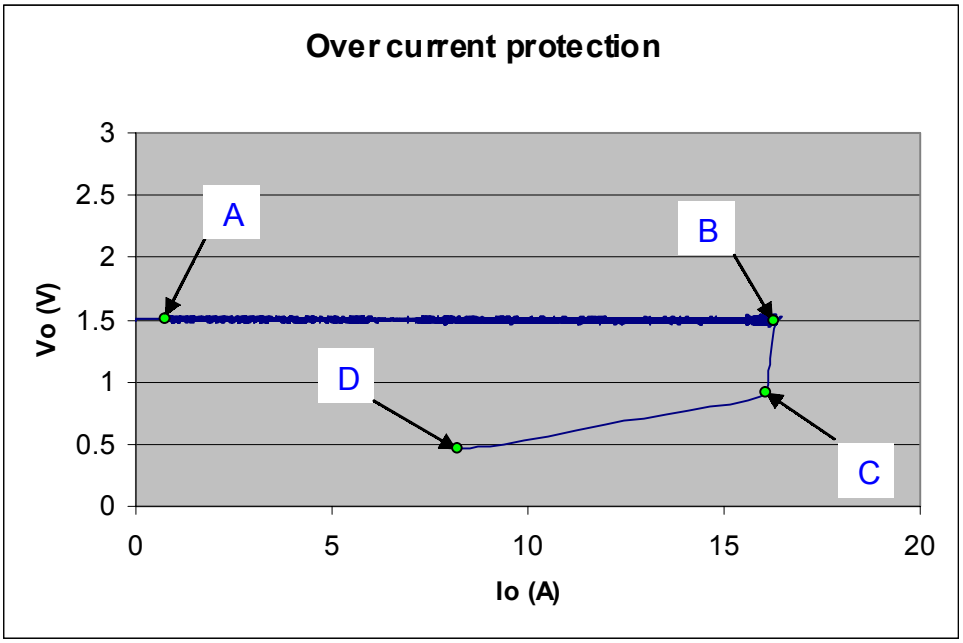


Applications Information (Cont.)

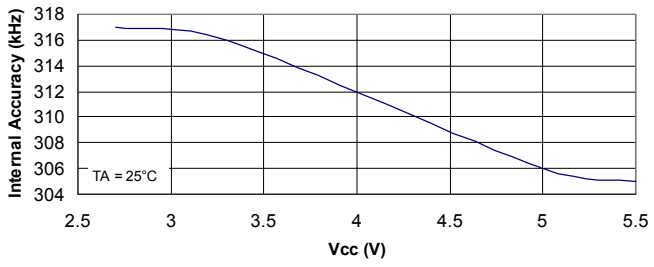
Over current protection characteristic of SC4605 for 3.3V to 1.5V @12A application

The over current protection curve below is obtained by applying a gradually increased load while the load current and the output voltage are monitored and measured. When the load current is increased from 0 to 16.2A (over current trigger point), the output voltage is 1.5V, corresponding from Point A to Point B. As the load current increases further from 16.2A to 16.3A, the output voltage drops significantly from 1.5V (Point B) to 0.88V (Point C). Because an over current and a lower output voltage (0.88V<68.75%*1.5V=1.03V) are present at Point C, the SC4605 enters its HICCUP mode. Then the locus of the output current and the output voltage follows Line CD as shown in the curve. Due to the over current applied, the HICCUP protection will go back and forth on Line CD. This prevents excess power dissipation in the TOP MOSFET during a short output condition.

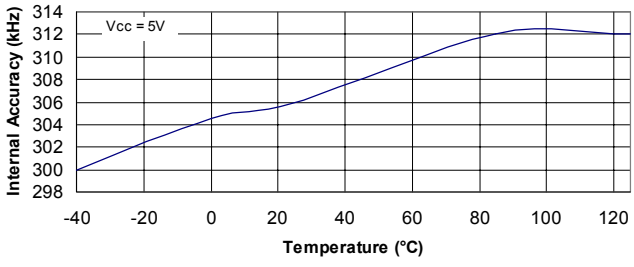


Typical Characteristics

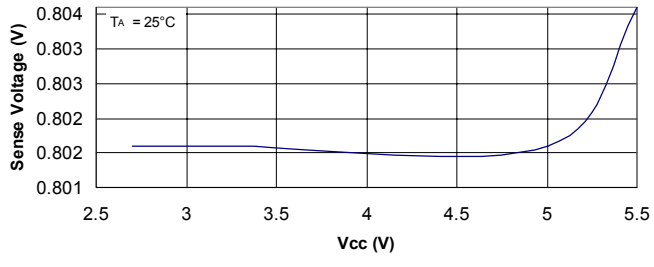
Oscillator Internal Accuracy vs Input Voltage



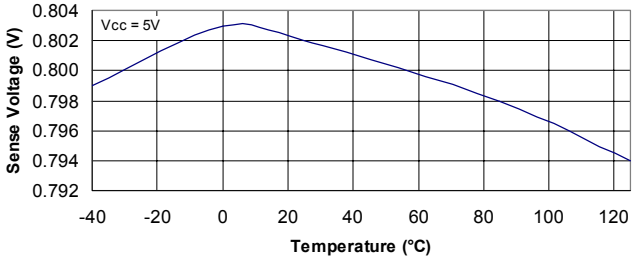
Oscillator Internal Accuracy vs Temperature



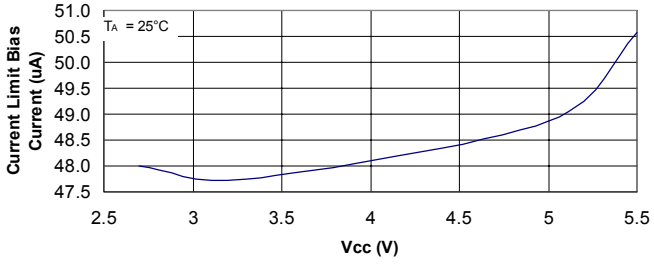
Sense Voltage vs Input Voltage



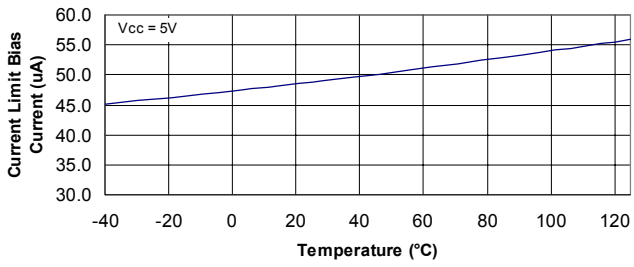
Sense Voltage vs Temperature



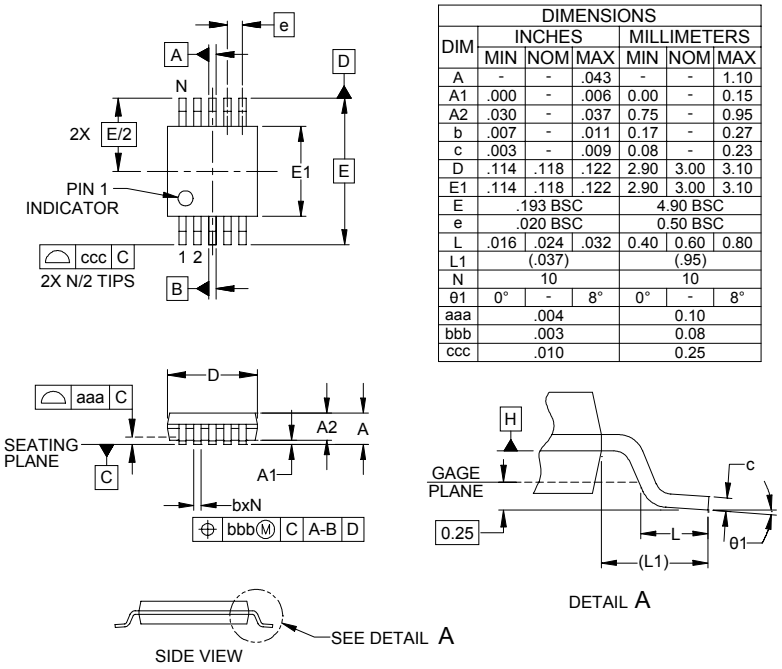
Current Limit Bias Current vs Input Voltage



Current Limit Bias Current vs Temperature



Outline Drawing - MSOP-10

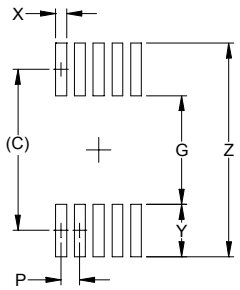


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.043	-	-	1.10
A1	.000	-	.006	0.00	-	0.15
A2	.030	-	.037	0.75	-	0.95
b	.007	-	.011	0.17	-	0.27
c	.003	-	.009	0.08	-	0.23
D	.114	.118	.122	2.90	3.00	3.10
E1	.114	.118	.122	2.90	3.00	3.10
E	.193 BSC			4.90 BSC		
e	.020 BSC			0.50 BSC		
L	.016	.024	.032	0.40	0.60	0.80
L1	(.037)			(.95)		
N	10			10		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.003			0.08		
ccc	.010			0.25		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-187, VARIATION BA.

Land Pattern - MSOP-10



DIM	INCHES	MILLIMETERS
C	(.161)	(4.10)
G	.098	2.50
P	.020	0.50
X	.011	0.30
Y	.063	1.60
Z	.224	5.70

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Contact Information

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