EPC2019 – Enhancement Mode Power Transistor

V_{DSS} , 200 V

$R_{DS(on)}$, 50 mΩ

I_D , 8.5 A

EPC

EFFICIENT POWER CONVERSION

RoHS | Halogen-Free
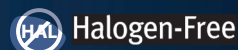
Gallium Nitride is grown on Silicon Wafers and processed using standard CMOS equipment leveraging the infrastructure that has been developed over the last 55 years. GaN's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

EPC2019 eGaN® FETs are supplied only in passivated die form with solder bars

Applications
- High Speed DC-DC conversion
- Class-D Audio
- High Frequency Hard-Switching and Soft-Switching Circuits

Benefits
- Ultra High Efficiency
- Ultra Low $R_{DS(on)}$
- Ultra low Q_G
- Ultra small footprint

www.epc-co.com/epc/Products/eGaNFETs/EPC2019.aspx

Maximum Ratings			
V_{DS}	Drain-to-Source Voltage (Continuous)	200	V
I_D	Continuous (T_A = 25°C, $R_{θJA}$ = 18 °C/W)	8.5	A
	Pulsed (25°C, T_{Pulse} = 300 µs)	42	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

Static Characteristics (T_J= 25°C unless otherwise stated)						
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 125 µA	200			V
I_{DSS}	Drain Source Leakage	V_{DS} = 160 V, V_{GS} = 0 V		20	100	µA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.8	2.5	mA
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		20	100	µA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1.5 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 7 A		36	50	mΩ
V_{SD}	Source-Drain Forward Voltage	I_S = 0.5 A, V_{GS} = 0 V		1.8		V

All measurements were done with substrate shorted to source.

Thermal Characteristics		TYP	UNIT
$R_{θJC}$	Thermal Resistance, Junction to Case	2.7	°C/W
$R_{θJB}$	Thermal Resistance, Junction to Board	7.5	°C/W
$R_{θJA}$	Thermal Resistance, Junction to Ambient (Note 1)	72	°C/W

Note 1: $R_{θJA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Dynamic Characteristics (T$_J$= 25°C unless otherwise stated)						
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C$_{ISS}$	Input Capacitance	V$_{DS}$ = 100 V, V$_{GS}$ = 0 V		200	270	pF
C$_{OSS}$	Output Capacitance			110	150	
C$_{RSS}$	Reverse Transfer Capacitance			0.7	1	
R$_G$	Gate Resistance			0.4		Ω
Q$_G$	Total Gate Charge	V$_{DS}$ = 100 V, V$_{GS}$ = 5 V, I$_D$ = 7 A		1.8	2.5	nC
Q$_{GS}$	Gate-to-Source Charge	V$_{DS}$ = 100 V, I$_D$ = 7 A		0.6		
Q$_{GD}$	Gate-to-Drain Charge			0.35	0.6	
Q$_{G(TH)}$	Gate Charge at Threshold			0.4		
Q$_{OSS}$	Output Charge	V$_{DS}$ = 100 V, V$_{GS}$ = 0 V		18	23	
Q$_{RR}$	Source-Drain Recovery Charge			0		

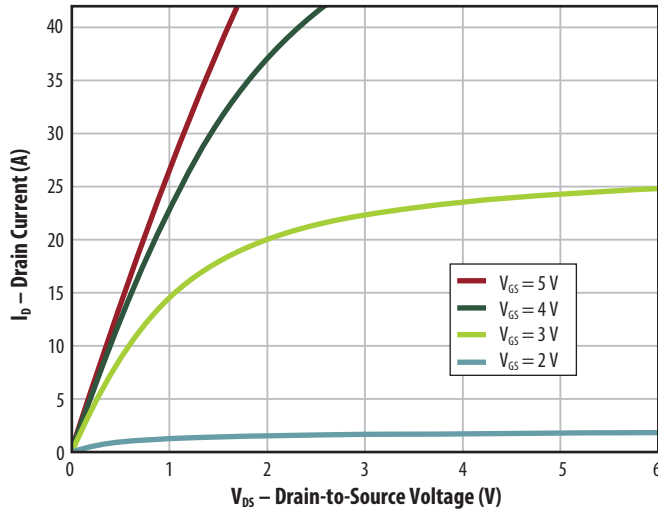All measurements were done with substrate shorted to source.

Figure 1: Typical Output Characteristics at 25°C
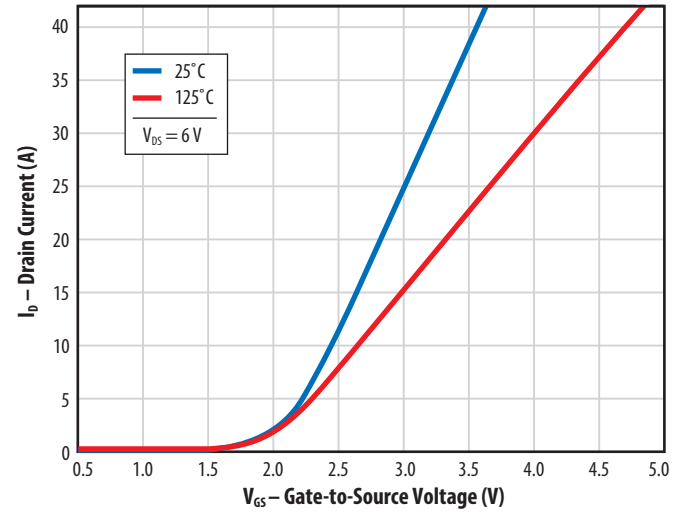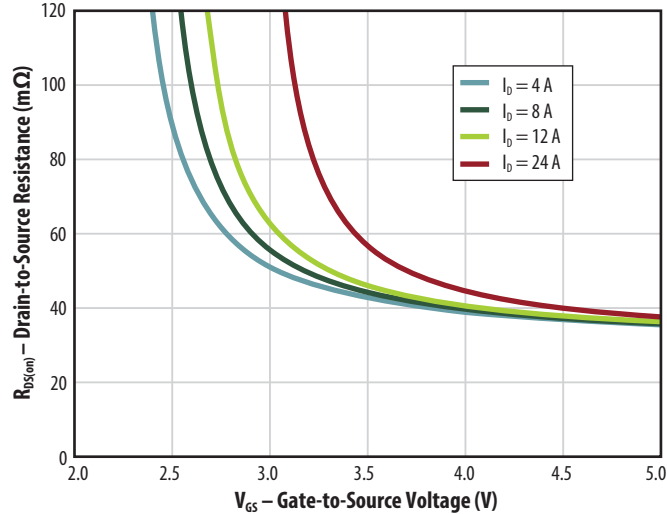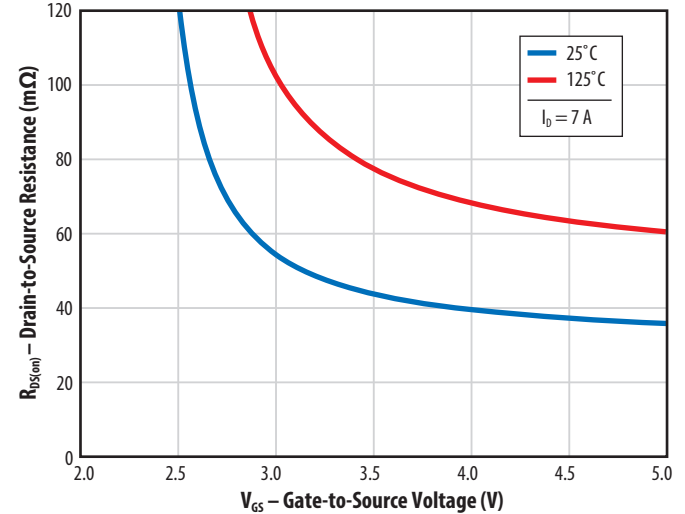

Figure 2: Transfer Characteristics

Figure 3: R$_{DS(on)}$ vs. V$_{GS}$ for Various Drain Currents

Figure 4: R$_{DS(on)}$ vs. V$_{GS}$ for Various Temperatures
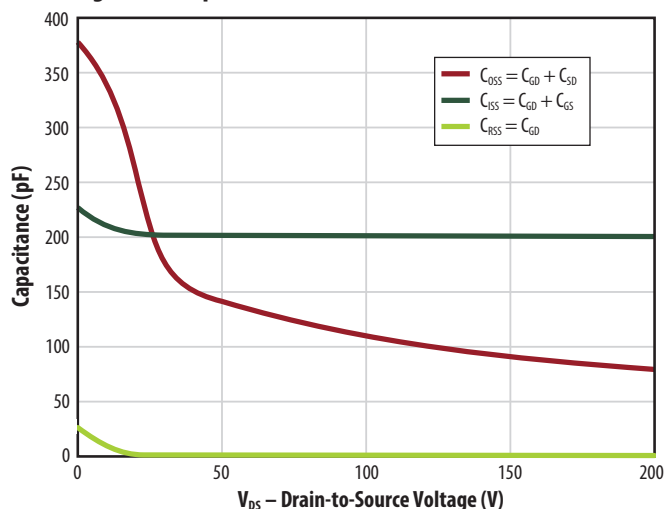
Figure 5a: Capacitance (Linear Scale)

Legend:
- $C_{OSS} = C_{GD} + C_{SD}$
- $C_{ISS} = C_{GD} + C_{GS}$
- $C_{RSS} = C_{GD}$

Y-axis: Capacitance (pF)
X-axis: V_{DS} – Drain-to-Source Voltage (V)

Figure 5b: Capacitance (Log Scale)

Legend:
- $C_{OSS} = C_{GD} + C_{SD}$
- $C_{ISS} = C_{GD} + C_{GS}$
- $C_{RSS} = C_{GD}$

Y-axis: Capacitance (pF)
X-axis: V_{DS} – Drain-to-Source Voltage (V)

Figure 6: Gate Charge

$I_D = 7$ A
$V_{DS} = 100$ V

Y-axis: V_{GS} – Gate-to-Source Voltage (V)
X-axis: Q_G – Gate Charge (nC)
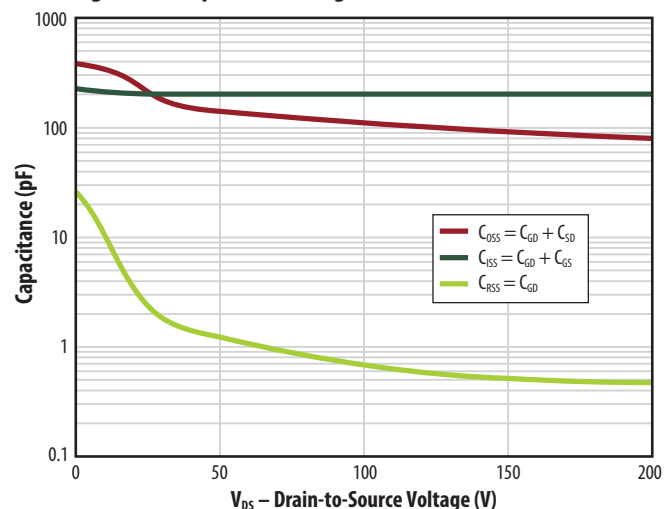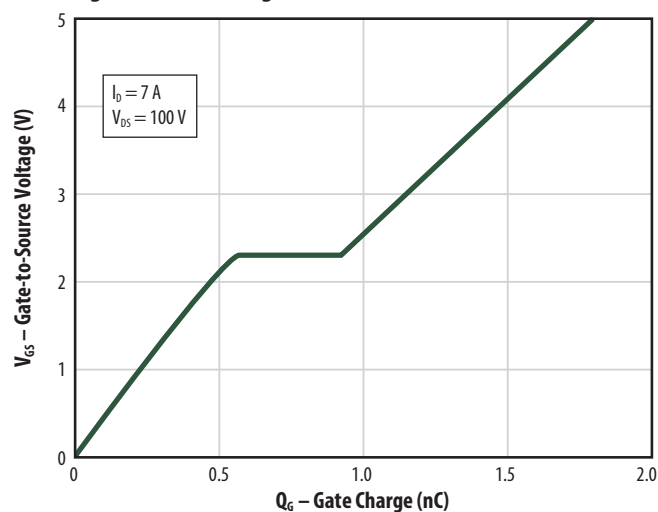
Figure 7: Reverse Drain-Source Characteristics

Legend:
- 25°C
- 125°C

Y-axis: I_{SD} – Source-to-Drain Current (A)
X-axis: V_{SD} – Source-to-Drain Voltage (V)
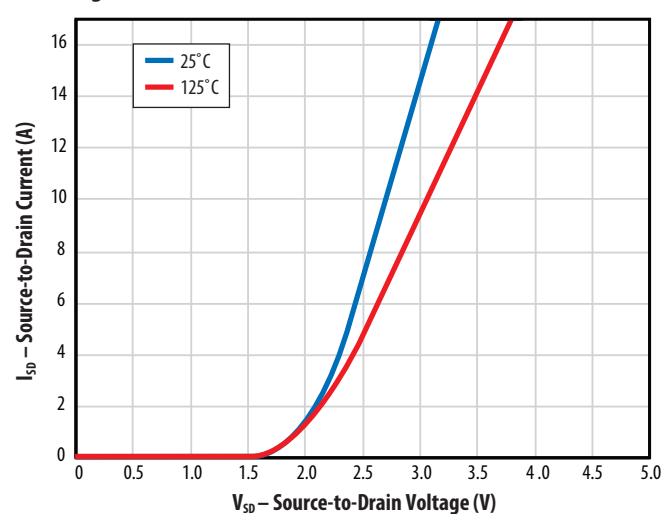
Figure 8: Normalized On-State Resistance vs. Temperature

$I_D = 7$ A
$V_{GS} = 5$ V

Y-axis: Normalized On-State Resistance $R_{DS(on)}$
X-axis: T_J – Junction Temperature (°C)
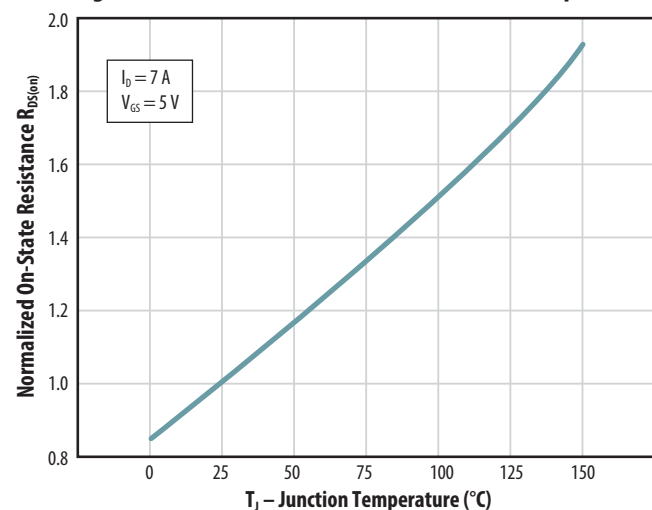
Figure 9: Normalized Threshold Voltage vs. Temperature

$I_D = 1.5$ mA

Y-axis: Normalized Threshold Voltage (V)
X-axis: T_J – Junction Temperature (°C)
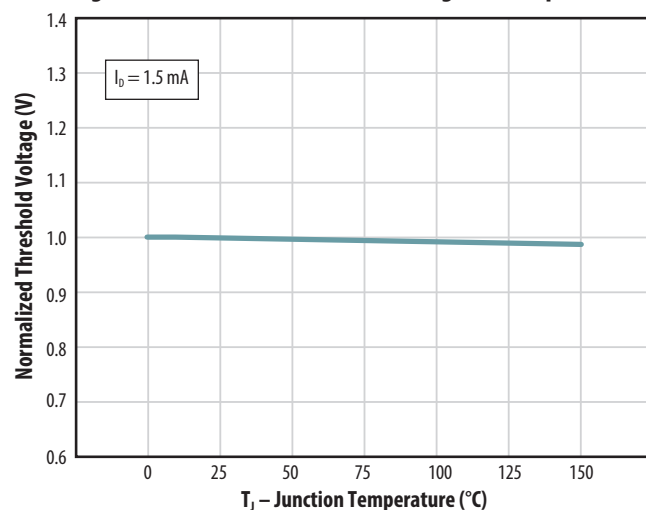
All measurements were done with substrate shortened to source.

Figure 10: Gate Leakage Current
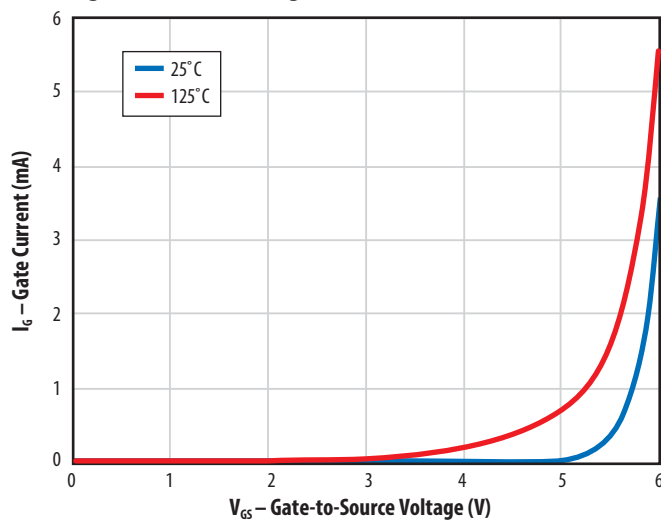
Figure 11: Transient Thermal Response Curves
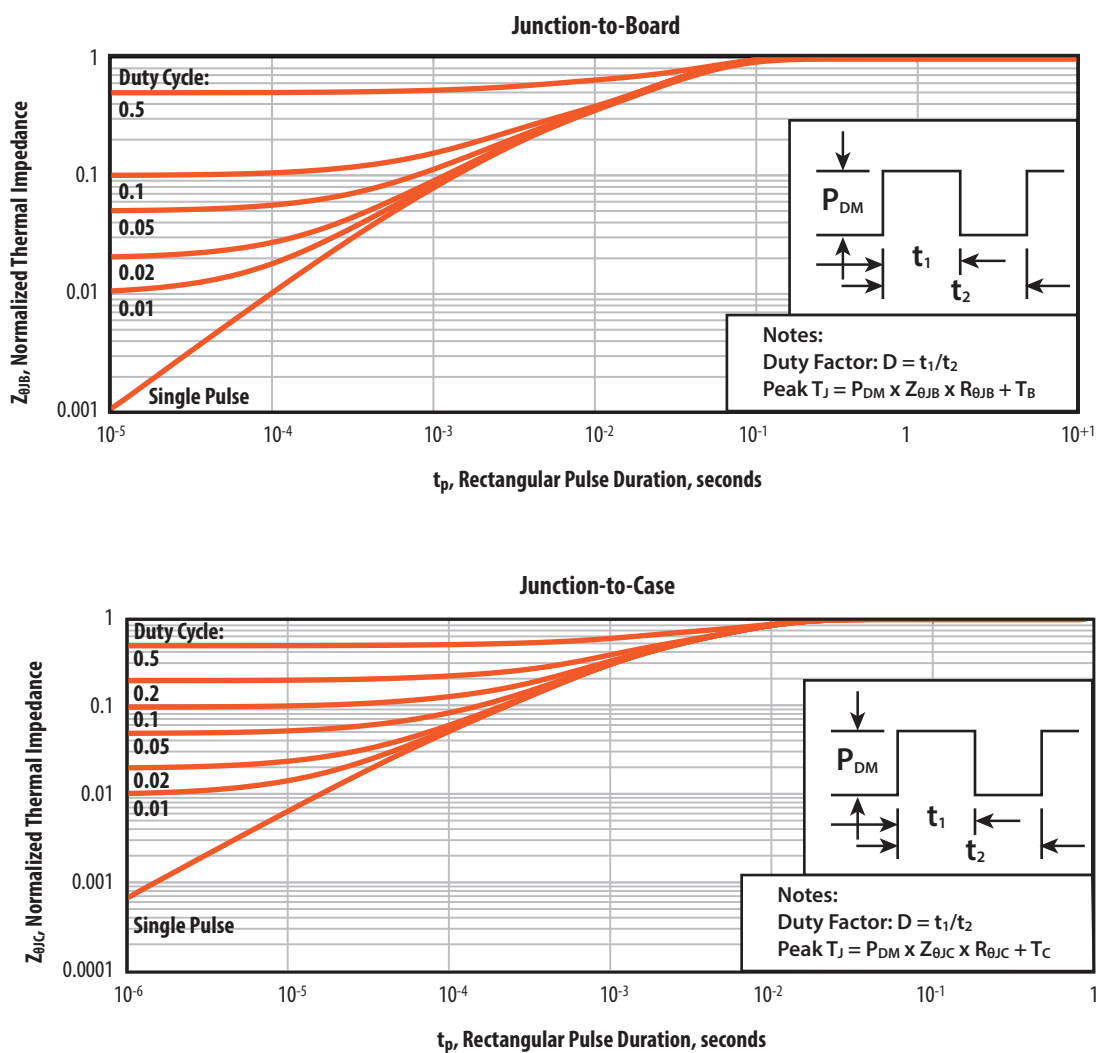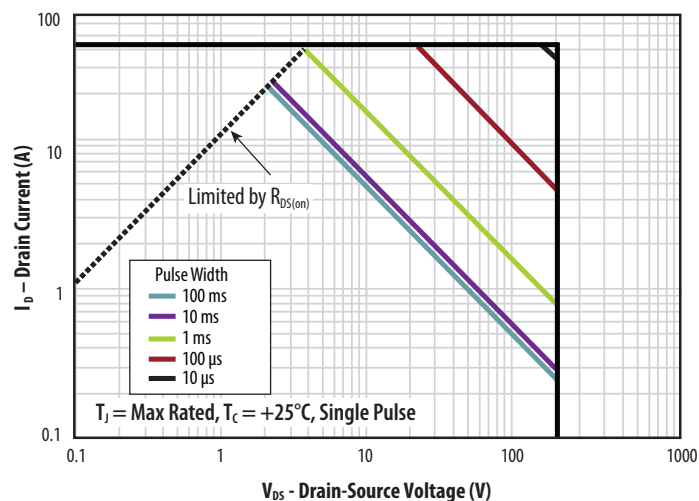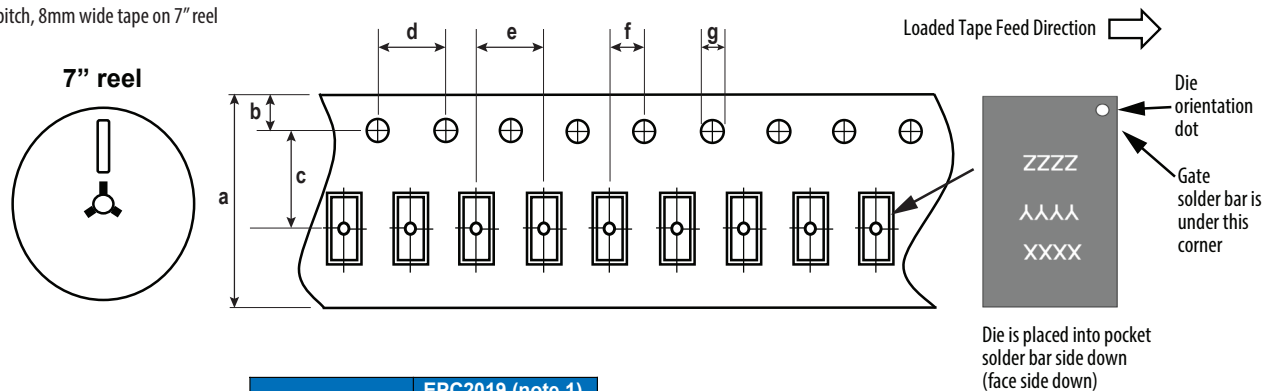
Junction-to-Board

Notes:
Duty Factor: $D = t_1/t_2$
Peak $T_J = P_{DM} \times Z_{\theta JB} \times R_{\theta JB} + T_B$

t_p, Rectangular Pulse Duration, seconds

Junction-to-Case

Notes:
Duty Factor: $D = t_1/t_2$
Peak $T_J = P_{DM} \times Z_{\theta JC} \times R_{\theta JC} + T_C$

t_p, Rectangular Pulse Duration, seconds

Figure 12: Safe Operating Area

**TAPE AND REEL CONFIGURATION**

4mm pitch, 8mm wide tape on 7" reel

Loaded Tape Feed Direction

Die orientation dot

Gate solder bar is under this corner

Die is placed into pocket solder bar side down (face side down)

EPC2019 (note 1)			
Dimension (mm)	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.
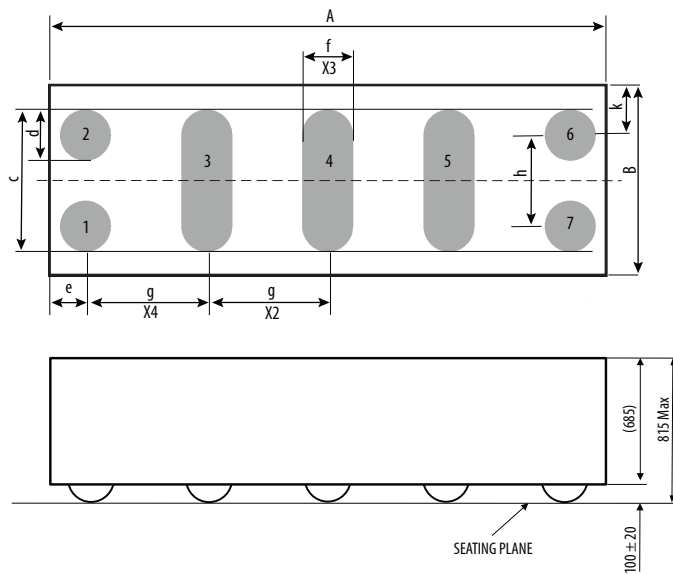
DIE MARKINGS

Die orientation dot

Gate Pad bump is under this corner
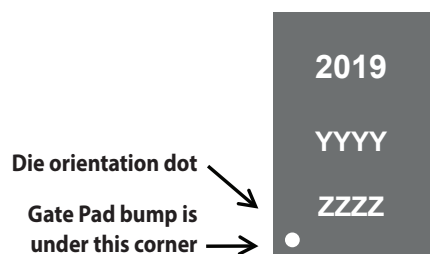
Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking line 2	Lot_Date Code Marking Line 3
EPC2019	2019	YYYY	ZZZZ

DIE OUTLINE

Solder Bar View

Side View

DIM	MICROMETERS		
	MIN	Nominal	MAX
A	2736	2766	2796
B	920	950	980
c	697	700	703
d	247	250	253
e	168	183	198
f	245	250	255
g	600	600	600
h	450	450	450
i	235	250	265

Pad no.1 is Gate

Pad no. 3, 5 are Drain

Pad no. 2, 4, 6 are Source

Pad no. 7 is Substrate

SEATING PLANE

Recommended Land Pattern

(Units in μm)

Pad no. 1 is Gate

Pad no. 3, 5 are Drain
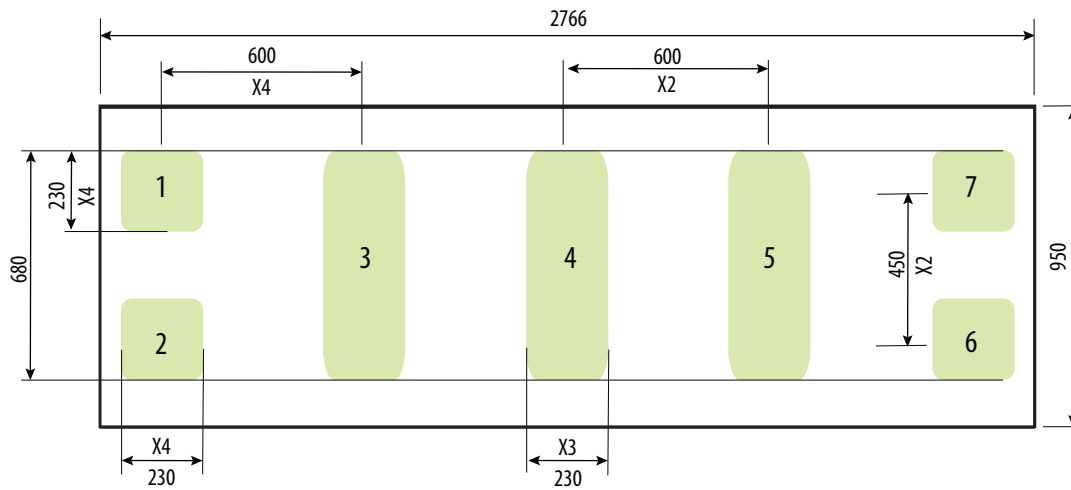
Pad no. 2, 4, 6 are Source

Pad no. 7 is Substrate
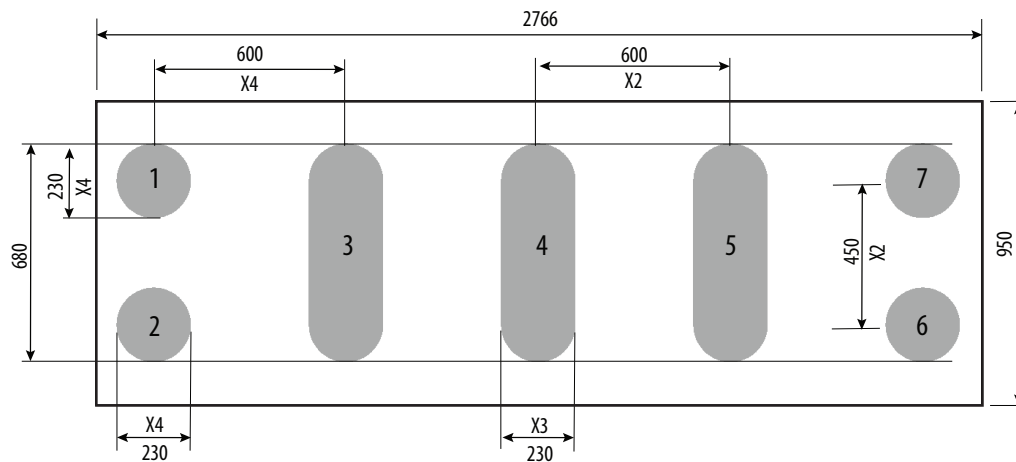
The land pattern shown is solder mask defined. Copper is larger than the solder mask opening. The solder mask is 10um smaller per side than the bump.

RECOMMENDED STENCIL

(Units in µm)

Pad no.1 is Gate

Pad no. 3, 5 are Drain

Pad no. 2, 4, 6 are Source

Pad no. 7 is Substrate

Recommended stencil should be 4mil (100µm) thick, must be laser cut, openings per drawing.

The solder stencil is 10µm smaller per side than the bump. The corner has a radius of R60

For assembly recommendations please visit http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

Information subject to change without notice. revised September, 2015