DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4060B
MSI
14-stage ripple-carry binary counter/divider and oscillator

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

DESCRIPTION

The HEF4060B is a 14-stage ripple-carry binary counter/divider and oscillator with three oscillator terminals (RS, R_{TC} and C_{TC}), ten buffered outputs (O_3 to O_9 and O_{11} to O_{13}) and an overriding asynchronous master reset input (MR). The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may be replaced by an external clock signal at input RS. The counter advances on the negative-going transition of RS. A HIGH level on MR resets the counter (O_3 to O_9 and O_{11} to O_{13} = LOW), independent of other input conditions.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

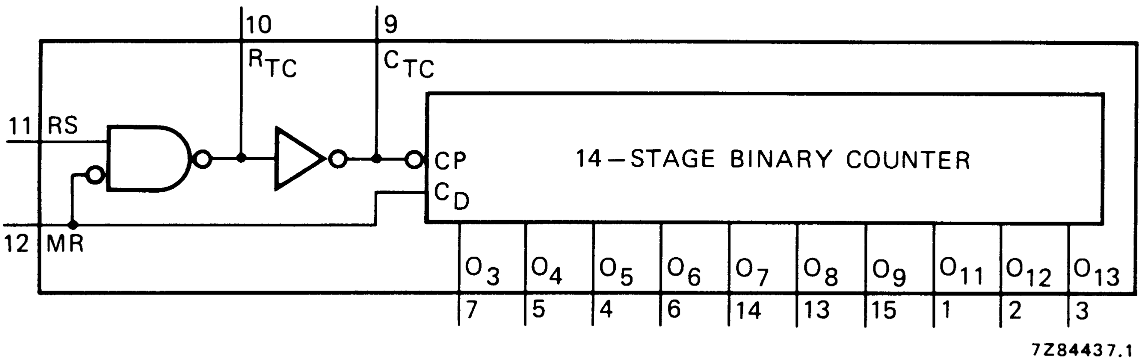


Fig.1 Functional diagram.

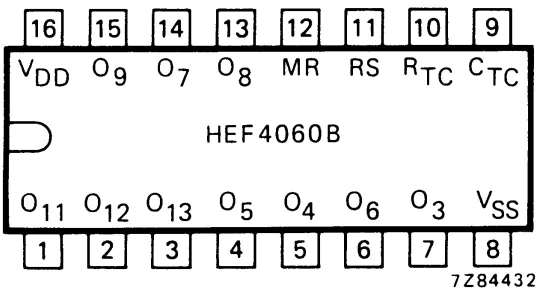


Fig.2 Pinning diagram.

PINNING

MR	master reset
RS	clock input/oscillator pin
R_{TC}	oscillator pin
C_{TC}	external capacitor connection
O_3 to O_9	counter outputs
O_{11} to O_{13}	counter outputs

HEF4060BP(N): 16-lead DIL; plastic (SOT38-1)

HEF4060BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)

HEF4060BT(D): 16-lead SO; plastic (SOT109-1)

( ): Package Designator North America

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

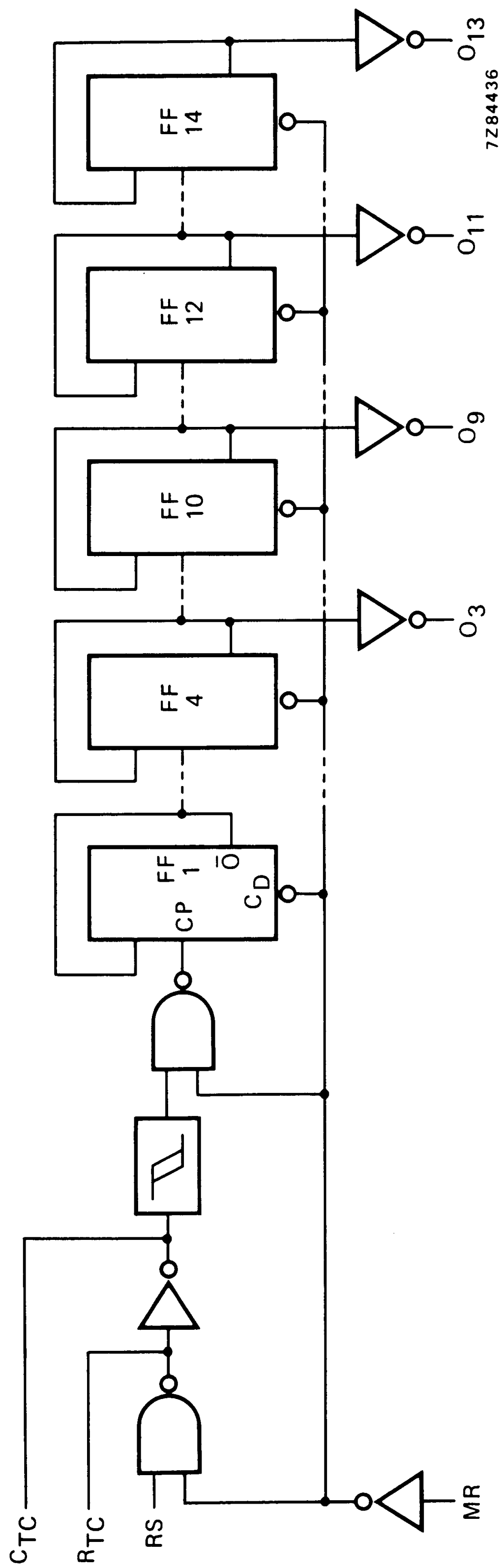


Fig.3 Logic diagram.

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays							
RS → O_3	5			210	420	ns	183 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		80	160	ns	69 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
	5			210	420	ns	183 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		80	160	ns	69 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
O_n → O_{n+1}	5			25	50	ns	
HIGH to LOW	10	t_{PHL}		10	20	ns	
	15			6	12	ns	
	5			25	50	ns	
LOW to HIGH	10	t_{PLH}		10	20	ns	
	15			6	12	ns	
MR → O_n	5			100	200	ns	73 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
Output transition	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
times	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
HIGH to LOW	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
Minimum clock pulse	5		120	60		ns	
width input RS	10	t_{WRSH}	50	25		ns	
HIGH	15		30	15		ns	
Minimum MR pulse	5		50	25		ns	
width; HIGH	10	t_{WMRH}	30	15		ns	
	15		20	10		ns	
Recovery time	5		160	80		ns	
for MR	10	t_{RMR}	80	40		ns	
	15		60	30		ns	
Maximum clock pulse	5		4	8		MHz	
frequency input RS	10	f_{max}	10	20		MHz	
	15		15	30		MHz	

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V_{DD} V	TYPICAL FORMULA FOR P (μW)[1]
Dynamic power dissipation per package (P)	5	$700\ f_i + f_oC_LV_{DD}^2$
	10	$3\ 300\ f_i + f_oC_LV_{DD}^2$
	15	$8\ 900\ f_i + f_oC_LV_{DD}^2$
Total power dissipation when using the on-chip oscillator (P)	5	$700\ f_{osc} + f_oC_LV_{DD}^2 + 2C_tV_{DD}^2f_{osc} + 690\ V_{DD}$
	10	$3\ 300\ f_{osc} + f_oC_LV_{DD}^2 + 2C_tV_{DD}^2f_{osc} + 6\ 900\ V_{DD}$
	15	$8\ 900\ f_{osc} + f_oC_LV_{DD}^2 + 2C_tV_{DD}^2f_{osc} + 22\ 000\ V_{DD}$

Notes

1. where:

   f_i = input frequency (MHz)

   f_o = output frequency (MHz)

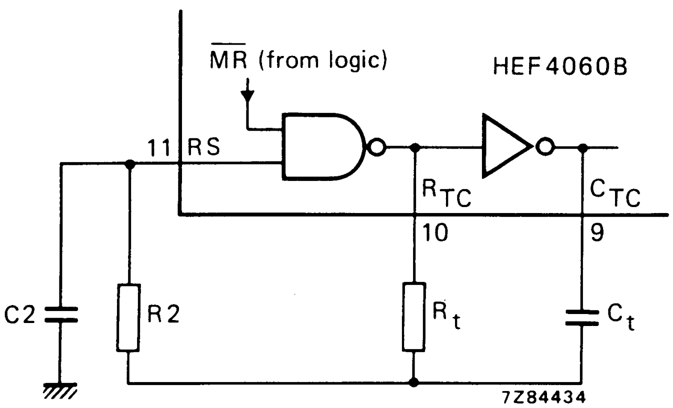
   C_L = load capacitance (pF)

   V_{DD} = supply voltage (V)

   C_t = timing capacitance (pF)

   f_{osc} = oscillator frequency (MHz)

RC oscillator



Typical formula for oscillator frequency:

$$f_{osc} = \frac{1}{2{,}3 \times R_t \times C_t}$$

Fig.4 External component connection for RC oscillator.

Timing component limitations

The oscillator frequency is mainly determined by R_tC_t, provided R_t << R2 and R2C2 << R_tC_t. The function of R2 is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C2 should be kept as small as possible. In consideration of accuracy, C_t must be larger than the inherent stray capacitance. R_t must be larger than the LOCMOS 'ON' resistance in series with it, which typically is 500 Ω at V_{DD} = 5 V, 300 Ω at V_{DD} = 10 V and 200 Ω at V_{DD} = 15 V.

The recommended values for these components to maintain agreement with the typical oscillation formula are:

$C_t \geq 100$ pF, up to any practical value,
10 kΩ ≤ R_t ≤ 1 MΩ.

Typical crystal oscillator circuit

In Fig.5, R2 is the power limiting resistor. For starting and maintaining oscillation a minimum transconductance is necessary.

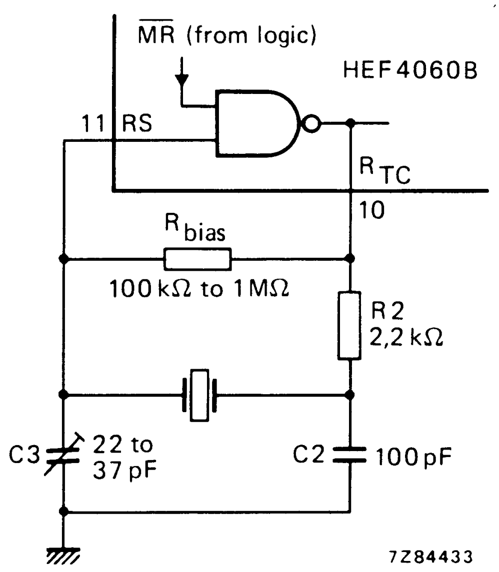


Fig.5 External component connection for crystal oscillator.

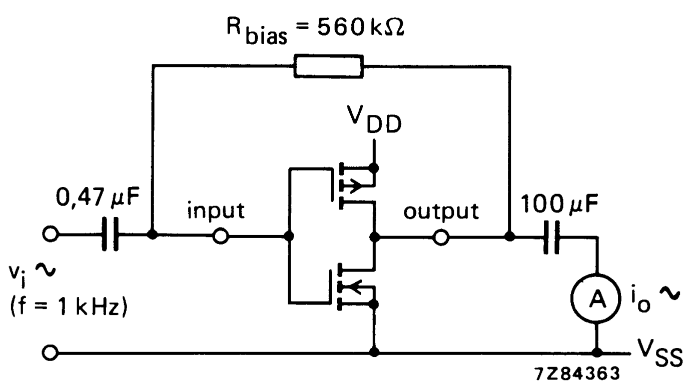
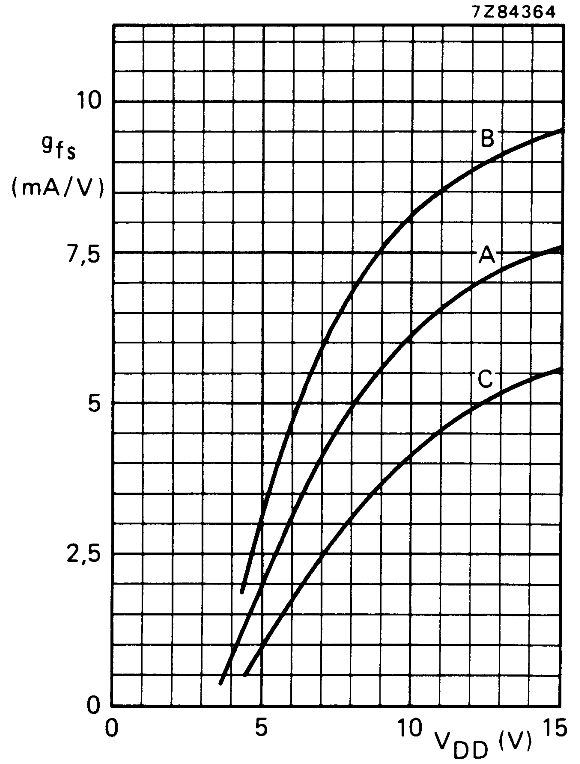


Fig.6 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig.7); MR = LOW.

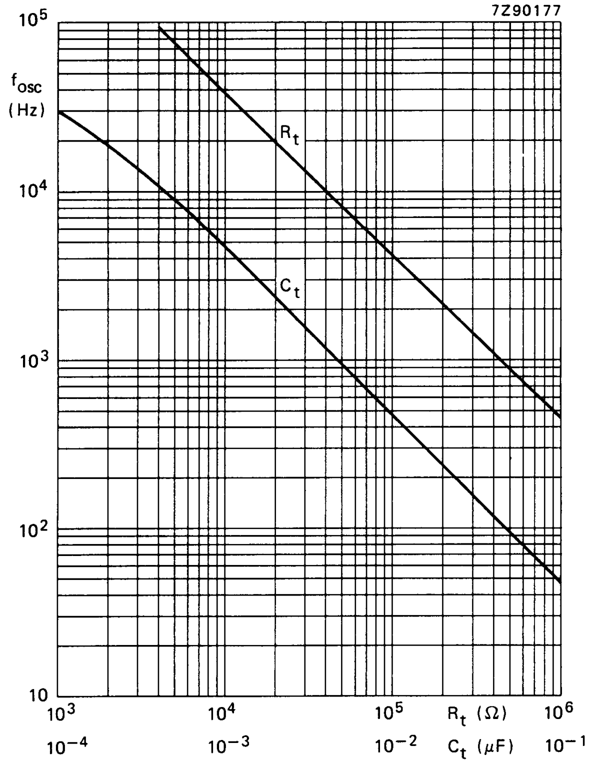


A: average

B: average + 2 s,

C: average – 2 s, where ‘s’ is the observed standard deviation.

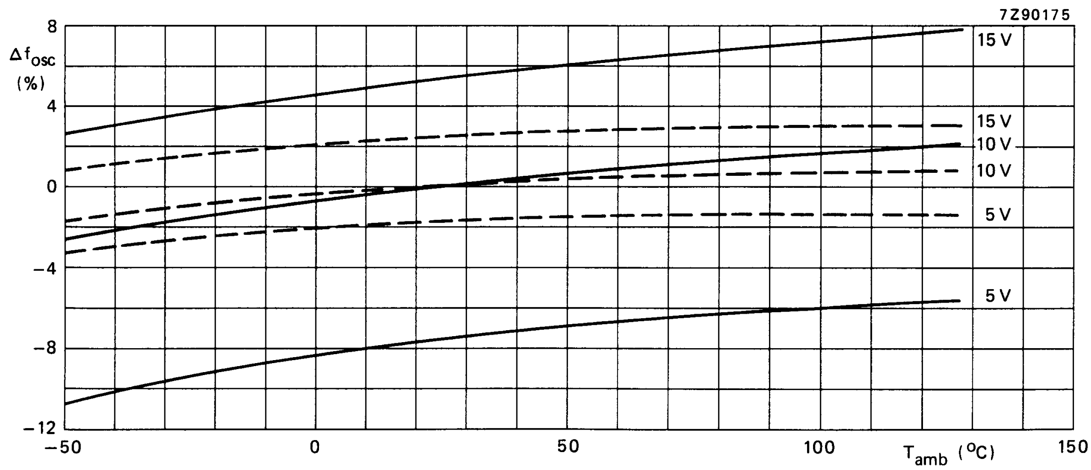
Fig.7 Typical forward transconductance g_{fs} as a function of the supply voltage at T_{amb} = 25 °C.



C_t curve at R_t = 100 kΩ; R2 = 470 kΩ.

R_t curve at C_t = 1 nF; R2 = 5 R_t.

Fig.8 RC oscillator frequency as a function of R_t and C_t at V_{DD} = 5 to 15 V; T_{amb} = 25 °C.



___ R_t = 100 kΩ; C_t = 1 nF; R2 = 0.

- - - R_t = 100 kΩ; C_t = 1 nF; R2 = 300 kΩ.

Fig.9 Oscillator frequency deviation (Δf_{osc}) as a function of ambient temperature; referenced at: f_{osc} at T_{amb} = 25 °C and V_{DD} = 10 V.