BATTERY PROTECTION IC FOR SERIES CONNECTION OF 1 TO 4 CELLS (SECONDARY PROTECTION) S-8244 Series

The S-8244 Series is used for secondary protection of lithium-ion batteries with from one to four cells, and incorporates a high-precision voltage detector circuit and a delay circuit. Short-circuits between cells accommodate series connection of one to four cells.

■ Features

- Internal high-precision voltage detector circuit

  1) Overcharge detection voltage range:

3.70 to 4.50 V:	Accuracy of ± 25 mV (at +25°C)
(at a 5 mV/step)	Accuracy of ± 50 mV (at -40 to +85°C)

  2) Hysteresis: 5 optional models available and selectable:

  0.38±0.1 V, 0.25±0.07 V, 0.13±0.04 V, 0.045±0.02 V, None

- High withstand voltage device (absolute maximum rating: 26 V)
- Wide operating voltage range: 3.6V to 24 V (refers to the range in which the delay circuit can operate normally after overvoltage is detected)
- Delay time during detection: Can be set by an external capacitor.
- Low current consumption

  At 3.5 V for each cell: 3.0 μA max. (+25°C)

  At 2.3 V for each cell: 2.4 μA max. (+25°C)

- Small package: 8-pin MSOP
- Output logic and form - 4 types:

  CMOS output active “H”

  CMOS output active “L”

  Pch open drain output active “L”

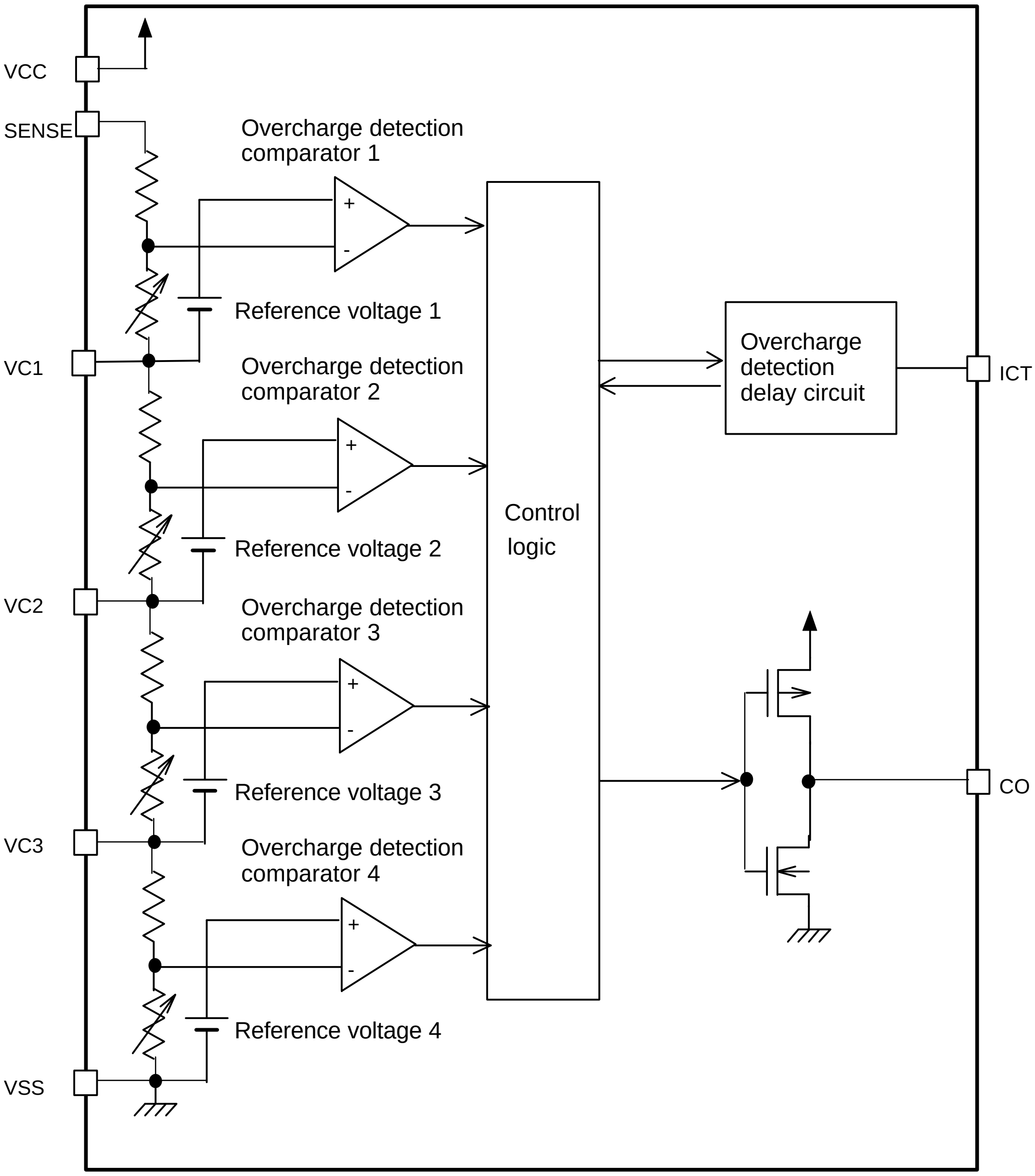
  Nch open drain output active “H”

  (only CMOS output for 0.045 V hysteresis models)

■ Applications

- Secondary protection of lithium ion rechargeable batteries

■ Block Diagram



Note: In the case of Nch open-drain output, only the Nch transistor will be connected to the CO pin. In the case of Pch open-drain output, only the Pch transistor will be connected to the CO pin.

Figure 1 Block Diagram

■ Selection Guide

Table 1 Selection Guide

Model No./Item	Overcharge detection voltage [V]	Overcharge hysteresis voltage [V]	Output form
S-8244AAAFN-CEA-T2	4.45 ± 0.025	0.38 ± 0.1	CMOS output active "H"
S-8244AABFN-CEB-T2	4.2 ± 0.025	0	Nch open drain active "H"
S-8244AACFN-CEC-T2	4.115 ± 0.025	0.13 ± 0.04	CMOS output active "H"
S-8244AADFN-CED-T2	4.2 ± 0.025	0	Pch open drain active "L"
S-8244AAEFN-CEE-T2	4.225 ± 0.025	0	Nch open drain active "H"
S-8244AAFFN-CEF-T2	4.35 ± 0.025	0.045 ± 0.02	CMOS output active "H"
S-8244AAGFN-CEG-T2	4.45 ± 0.025	0.045 ± 0.02	CMOS output active "H"
S-8244AAHFN-CEH-T2	4.30 ± 0.025	0.25 ± 0.07	CMOS output active "H"

For any changes to the detection voltage or other parameters, contact Sales Representative at SII Sales Department.

■ Pin Assignment

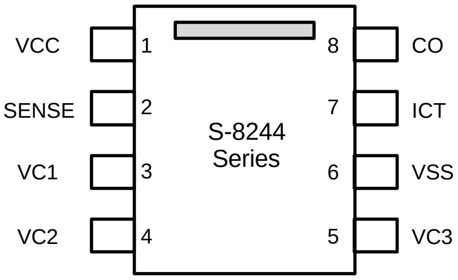


Figure 2 Pin Assignment

■ Pin Description

Table 2 Pin Description

Pin No.	Symbol	Description
1	VCC	Positive power input pin
2	SENSE	Positive voltage connection pin of Battery 1
3	VC1	Negative voltage connection pin of Battery 1; Positive voltage connection pin of Battery 2
4	VC2	Negative voltage connection pin of Battery 2; Positive voltage connection pin of Battery 3
5	VC3	Negative voltage connection pin of Battery 3; Positive voltage connection pin of Battery 4
6	VSS	Negative power input pin; Negative voltage connection pin of Battery 4
7	ICT	Capacitor connection pin for overcharge detection delay
8	CO	FET gate connection pin for charge control

■ Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings (Ta = 25°C unless otherwise specified)

Item	Symbol	Applicable pin	Rating	Unit
Input voltage between VCC and VSS	VDS	VCC	-0.3 to 26	V
Delay capacitor connection pin voltage	VICT	ICT	VSS -0.3 to VCC +0.3	V
Input pin voltage	VIN	SENSE, VC1, VC2, VC3	VSS -0.3 to VCC +0.3	V
CO output pin voltage	VCO	CO	VSS -0.3 to VCC +0.3 (CMOS output)	V
			VSS -0.3 to 26 (Nch open drain output)	
			VCC -26 to VCC +0.3 (Pch open drain output)	
Power dissipation	PD		150	mW
Operating temperature range	Topr		-40 to +85	°C
Storing temperature range	Tstg		-40 to +125	°C

This IC has a protection circuit against static electricity. DO NOT apply high static electricity or high voltage that exceeds the performance of the protection circuit to the IC.

■ Electrical Characteristics

Table 4 Electrical Characteristics (Ta = 25°C unless otherwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Measure-ment conditions	Measure-ment circuit
DETECTION VOLTAGE								
Overcharge detection voltage 1 (*3)	VCU1	3.7 to 4.5 V Adjustment	VCU1 -0.025	VCU1	VCU1 +0.025	V	1	1
Overcharge detection voltage 2 (*3)	VCU2	3.7 to 4.5 V Adjustment	VCU2 -0.025	VCU2	VCU2 +0.025	V	2	1
Overcharge detection voltage 3 (*3)	VCU3	3.7 to 4.5 V Adjustment	VCU3 -0.025	VCU3	VCU3 +0.025	V	3	1
Overcharge detection voltage 4 (*3)	VCU4	3.7 to 4.5 V Adjustment	VCU4 -0.025	VCU4	VCU4 +0.025	V	4	1
Overcharge hysteresis voltage 1 (*5)	VCD1		0.28	0.38	0.48	V	1	1
Overcharge hysteresis voltage 2 (*5)	VCD2		0.28	0.38	0.48	V	2	1
Overcharge hysteresis voltage 3 (*5)	VCD3		0.28	0.38	0.48	V	3	1
Overcharge hysteresis voltage 4 (*5)	VCD4		0.28	0.38	0.48	V	4	1
Detection voltage temperature coefficient (*1)	TCOE	Ta=-40 to 85°C	-0.4	0.0	+0.4	mV/°C	—	—
DELAY TIME								
Overcharge detection delay time	tCU	C=0.1 μF	1.0	1.5	2.0	s	5	2
OPERATING VOLTAGE								
Operating voltage between VCC and VSS (*2)	VDSOP		3.6	—	24	V	—	—
CURRENT CONSUMPTION								
Current consumption during normal operation	I OPE	V1=V2=V3=V4=3.5V	—	1.5	3.0	μA	6	3
Current consumption at power down	I PDN	V1=V2=V3=V4=2.3V	—	1.2	2.4	μA	6	3
VC1 sink current	IVC1	V1=V2=V3=V4=3.5V	-0.3	—	0.3	μA	6	3
VC2 sink current	IVC2	V1=V2=V3=V4=3.5V	-0.3	—	0.3	μA	6	3
VC3 sink current	IVC3	V1=V2=V3=V4=3.5V	-0.3	—	0.3	μA	6	3
OUTPUT VOLTAGE(*4)								
CO “H” voltage	VCO(H)	at I_{OUT} = 10 μA	VCC-0.05	—	—	V	7	4
CO “L” voltage	VCO(L)	at I_{OUT} = 10 μA	—	—	VSS+0.05	V	7	4

Note (*1) : Overcharge detection voltage or overcharge hysteresis voltage.

Note (*2) : Operating voltage indicates that the delay circuit operates normally after an overcharge is detected.

Note (*3) : ±50 mV when Ta = -40 to +85°C.

Note (*4) : Output logic and CMOS or open drain output can be selected.

Note (*5) : 0.25 V ± 0.07 V, 0.13 V ± 0.04 V, 0.045 V ± 0.02 V except for 0.38 V hysteresis models.

■ Measurement Circuits

(1) Measurement Condition 1, Measurement Circuit 1

Conditions:

- Set switches 1 and 2 to OFF for CMOS output models.
- Set switch 1 to ON and switch 2 to OFF for Nch open drain models.
- Set switch 1 to OFF and switch 2 to ON for Pch open drain models.

Definitions:

- Set V1, V2, V3 and V4 to 3.5 V and gradually increase V1:
  Overcharge detection voltage 1 (VCU1) is defined as V1 voltage when CO is turned to “H” (for CMOS output active “H” or Nch open drain) or “L” (for CMOS output active “L” or Pch open drain).
- Next, gradually decrease V1:
  Overcharge hysteresis voltage VCD1 is defined as a difference between VCU1 and V1 when CO is turned to “L” (for CMOS output active “H” or Nch open drain) or “H” (for CMOS output active “L” or Pch open drain).

(2) Measurement Condition 2, Measurement Circuit 1

Conditions:

- Set switches 1 and 2 to OFF for CMOS output models.
- Set switch 1 to ON and switch 2 to OFF for Nch open drain models.
- Set switch 1 to OFF and switch 2 to ON for Pch open drain models.

Definitions:

- Set V1, V2, V3 and V4 to 3.5 V and gradually increase V2.
  Overcharge detection voltage 2 (VCU2) is defined as V2 voltage when CO is turned to “H” (for CMOS output active “H” or Nch open drain) or “L” (for CMOS output active “L” or Pch open drain).
- Next, gradually decrease V2.
  Overcharge hysteresis voltage VCD2 is defined as a difference between VCU2 and V2 when CO is turned to “L” (for CMOS output active “H” or Nch open drain) or “H” (for CMOS output active “L” or Pch open drain).

(3) Measurement Condition 3, Measurement Circuit 1

Conditions:

- Set switches 1 and 2 to OFF for CMOS output models.
- Set switch 1 to ON and switch 2 to OFF for Nch open drain models.
- Set switch 1 to OFF and switch 2 to ON for Pch open drain models.

Definitions:

- Set V1, V2, V3 and V4 to 3.5 V and gradually increase V3.
  Overcharge detection voltage 3 (VCU3) is defined as V3 voltage when CO is turned to “H” (for CMOS output active “H” or Nch open drain) or “L” (for CMOS output active “L” or Pch open drain).
- Next gradually decrease V3.
  Overcharge hysteresis voltage VCD3 is defined as a difference between VCU3 and V3 when CO is turned to “L” (for CMOS output active “H” or Nch open drain) or “H” (for CMOS output active “L” or Pch open drain).

(4) Measurement Condition 4, Measurement Circuit 1

Conditions:

- Set switches 1 and 2 to OFF for CMOS output models.
- Set switch 1 to ON and switch 2 to OFF for Nch open drain models.
- Set switch 1 to OFF and switch 2 to ON for Pch open drain models.

Definitions:

- Set V1, V2, V3 and V4 to 3.5 V and gradually increase V4.
  Overcharge detection voltage 4 (VCU4) is defined as V4 voltage when CO is turned to “H” (for CMOS output active “H” or Nch open drain) or “L” (for CMOS output active “L” or Pch open drain).
- Next, gradually decrease V4.
  Overcharge hysteresis voltage VCD4 is defined as a difference between VCU4 and V4 when CO is turned to “L” (for CMOS output active “H” or Nch open drain) or “H” (for CMOS output active “L” or Pch open drain).

(5) Measurement Condition 5, Measurement Circuit 2

Conditions:

- Set switches 1 and 2 to OFF for CMOS output models.
- Set switch 1 to ON and switch 2 to OFF for Nch open drain models.
- Set switch 1 to OFF and switch 2 to ON for Pch open drain models.

Definition:

- Set V1, V2, V3 and V4 to 3.5 V and momentarily rise V1 to 4.7 V within10 µs.
  Overcharge detection delay time (tCU) is the period from when V1 goes 4.7 V to when CO is turned to “H” (for CMOS output active “H” or Nch open drain) or “L” (for CMOS output active “L” or Pch open drain).

(6) Measurement Condition 6, Measurement Circuit 3

Conditions:

- Set V1, V2, V3 and V4 to 2.3 V.
- Measure current consumption (I1).

Definition:

- The current consumption (I1) is defined as current consumption at power down (IPDN).

Conditions:

- Set V1, V2, V3 and V4 to 3.5 V.
- Measure current consumption I1, I2, I3, and I4.

Definition:

- The current consumption (I1) is defined as current consumption during normal operation (IOPE), the current consumption (I2) as VC1 sink current (IVC1), the current consumption (I3) as VC2 sink current(IVC2), and the current consumption (I4) as VC3 sink current (IVC3), respectively.

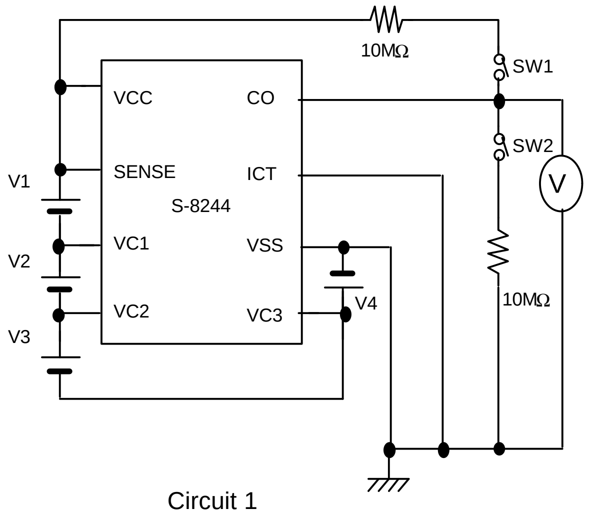
(7) Measurement Condition 7, Measurement Circuit 4

Conditions:

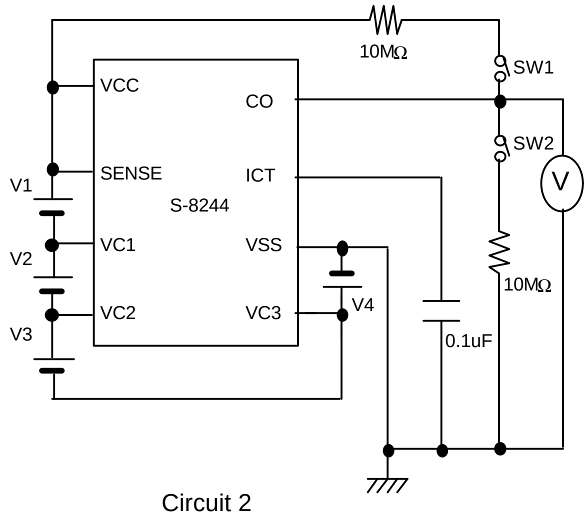
- Set switch 1 to ON and switch 2 to OFF for CMOS output active “H” or Nch open drain models.
- Set switch 1 to OFF and switch 2 to ON for Pch open drain models.

Definitions:

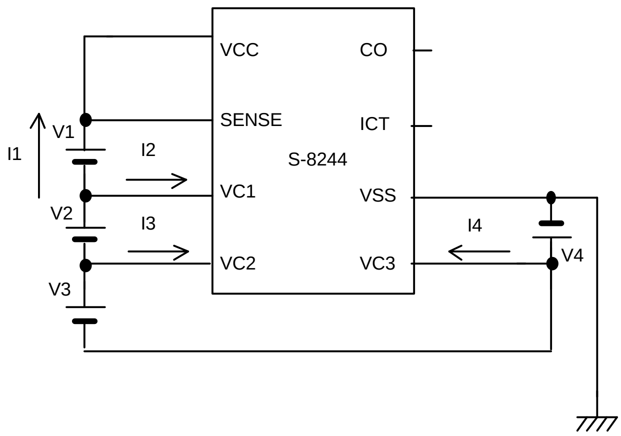
- Set V1, V2, V3 and V4 to 3.5 V and gradually increase V5 from 0V (for CMOS output active “H” or Nch open drain models).
  V5 voltage is defined as VCO (H) when I1 (= 10 µA) flows.
- Set V1, V2, V3 and V4 to 3.5 V and gradually increase V6 from 0 V (for CMOS output active “L” or Pch open drain models).
  V6 voltage is defined as VCO (L) when I2 (= 10 µA) flows.



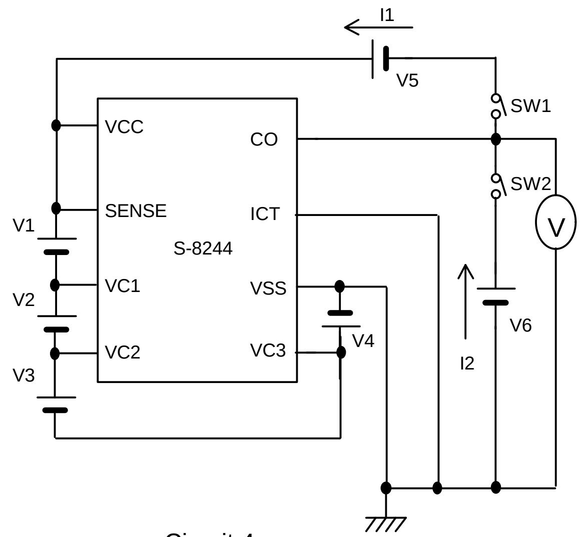
Circuit 1



Circuit 2



Circuit 3



Circuit 4

■ Description of Operation

Overcharge Detection

CO is turned to “H” (for CMOS output active “H” or Nch open drain models) or “L” (for CMOS output active “L” or Pch open drain models) when the voltage of one of the batteries exceeds the overcharge detection voltage (VCU) during charging under normal conditions beyond the overcharge detection delay time (tCU). This state is called “overcharge.” Attaching FET to the CO pin provides charge control and a second protection. At that time, the overcharge state is maintained until the voltage of all batteries decreases from the overcharge detection voltage (VCU) by the equivalent to the overcharge hysteresis voltage (VCD).

Delay Circuit

The delay circuit rapidly charges the capacitor connected to the delay capacitor connection pin up to a specified voltage when the voltage of one of the batteries exceeds the overcharge detection voltage (VCU). Then, the delay circuit gradually discharges the capacitor at 100 nA and inverts the CO output when the voltage at the delay capacitor connection pin goes below a specified level. Overcharge detection delay time (tCU) varies depending upon the external capacitor.

Each delay time is calculated using the following equation (Ta= -40 to +85°C).

	Min.	Typ.	Max.	
tCU[s] = Delay Coefficient	(10,	15,	20)	x CICT [μF]

Because the delay capacitor is rapidly charged, the smaller the capacitance, the larger the difference between the maximum voltage and the specified value of delay capacitor pin (ICT pin). This will cause a deviation between the calculated delay time and the resultant delay time. Also, delay time is internally set in this IC to prevent the CO output from inverting until the charge to delay capacitor pin is reached to the specified voltage. If large capacitance is used, output may be enabled without delay time because charge is disabled within the internal delay time.

Please note that the maximum capacitance connected to the delay capacitor pin (ICT pin) is 1 μF.

■ Operation Timing Chart

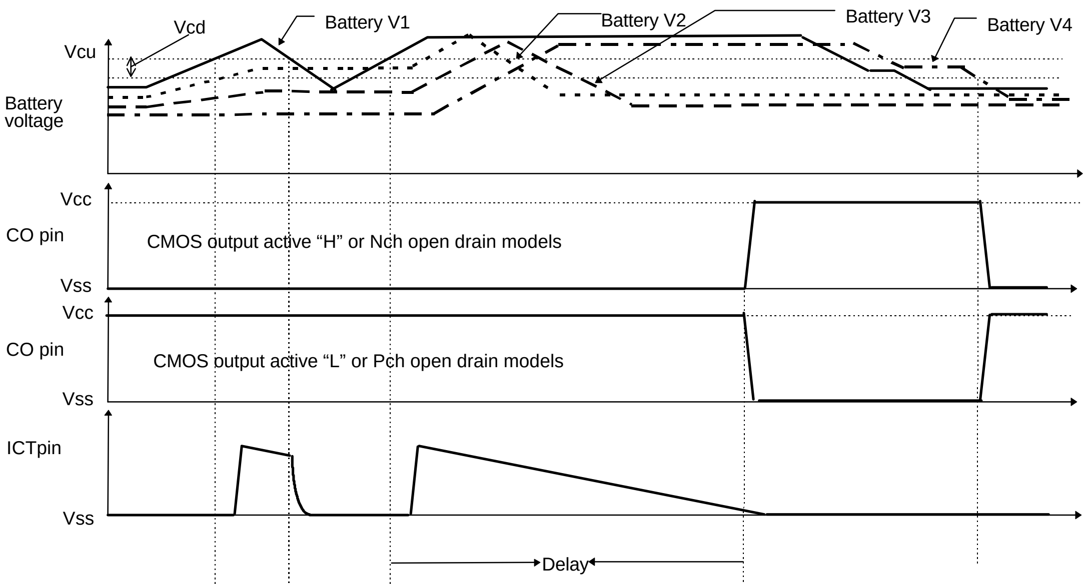


Figure 3 Operation Timing Chart

■ Battery Protection IC Connection Example 1

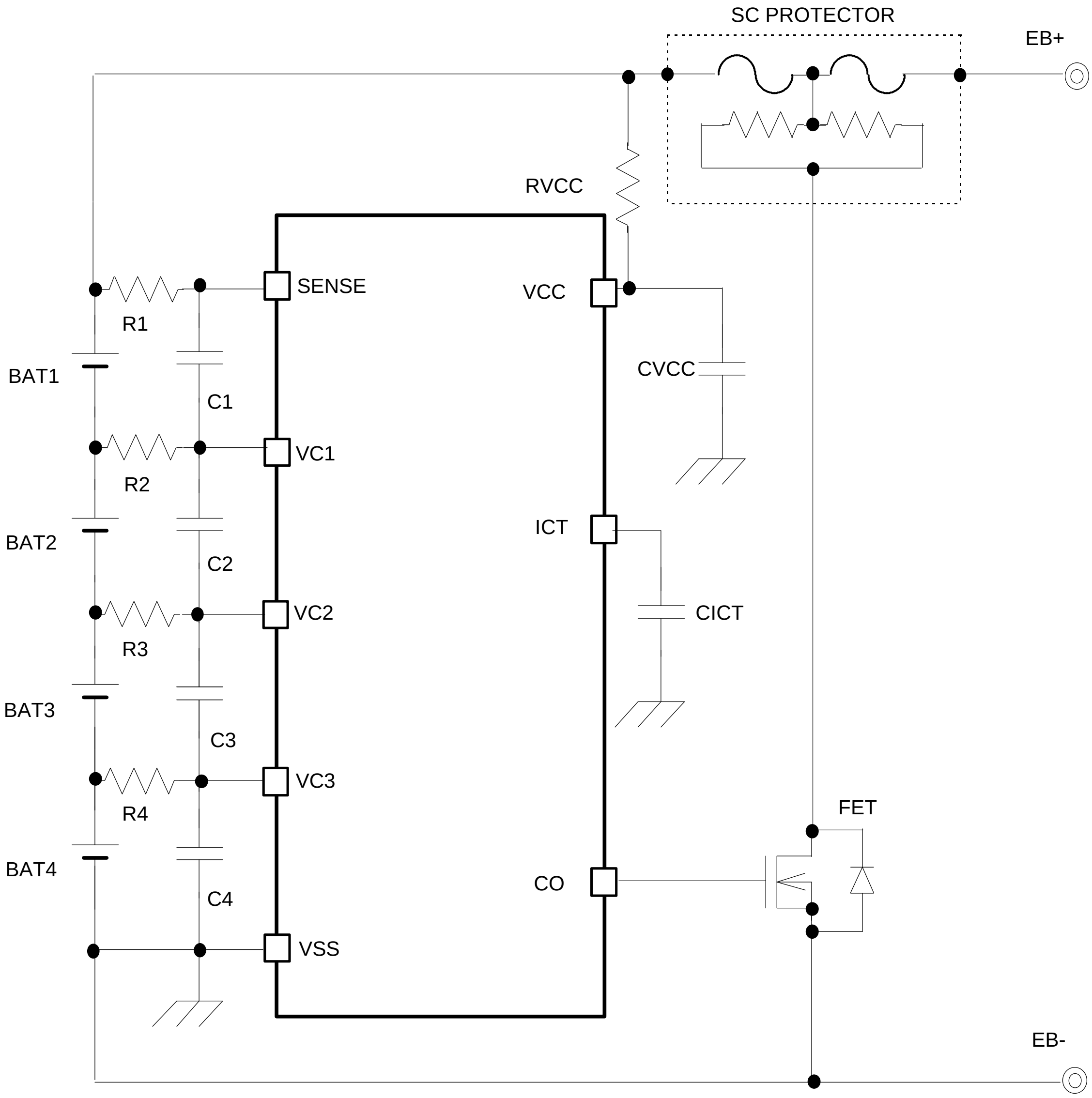


Figure 4 Battery Protection IC Connection Example 1

Table 5 Constants

Symbol	Min.	Recommended Value	Max.	Unit
R1 to R4	0	1 k	10 k	Ω
C1 to C4	0	0.1	1	μF
RVCC	0	100	1 k	Ω
CVCC	0	0.1	1	μF
CICT	0	0.1	1	μF

For SC PROTECTOR, contact

Sony Chemicals Corporation

Bonding & Materials Division

1-6-3 Nihombashi-Muromachi, Chuo-ku, Tokyo, 103-8312 Japan

TEL: 03-3279-0448 FAX: 03-5255-8448

■ Battery Protection IC Connection Example 2

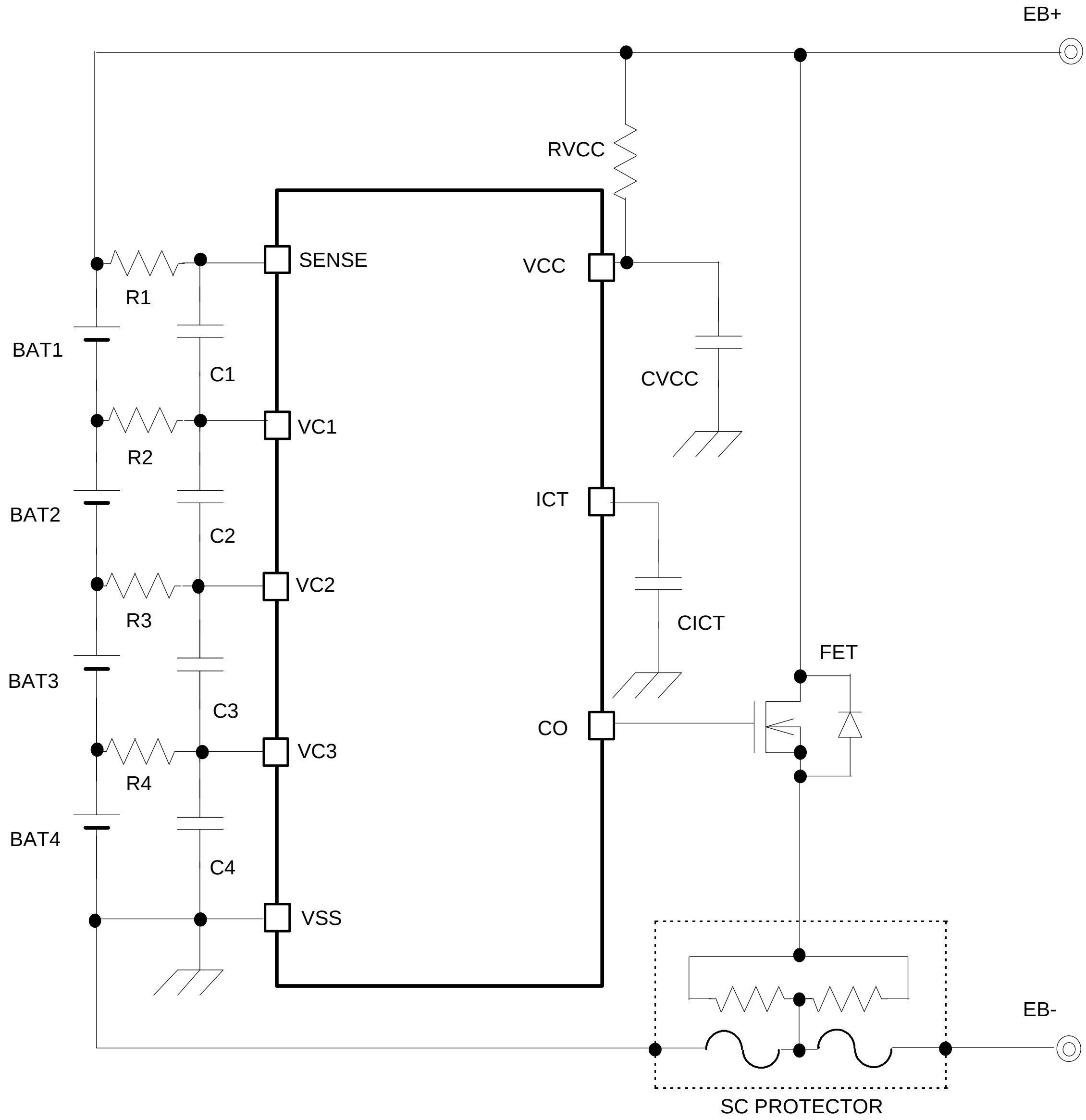


Figure 5 Battery Protection IC Connection Example 2

Table 6 Constants

	Min.	Recommended Value	Max.	Unit
R1 to R4	0	1 k	10 k	Ω
C1 to C4	0	0.1	1	μF
RVCC	0	100	1 k	Ω
CVCC	0	0.1	1	μF
CICT	0	0.1	1	μF

■ Battery Protection IC Connection Example 3 (for three cells)

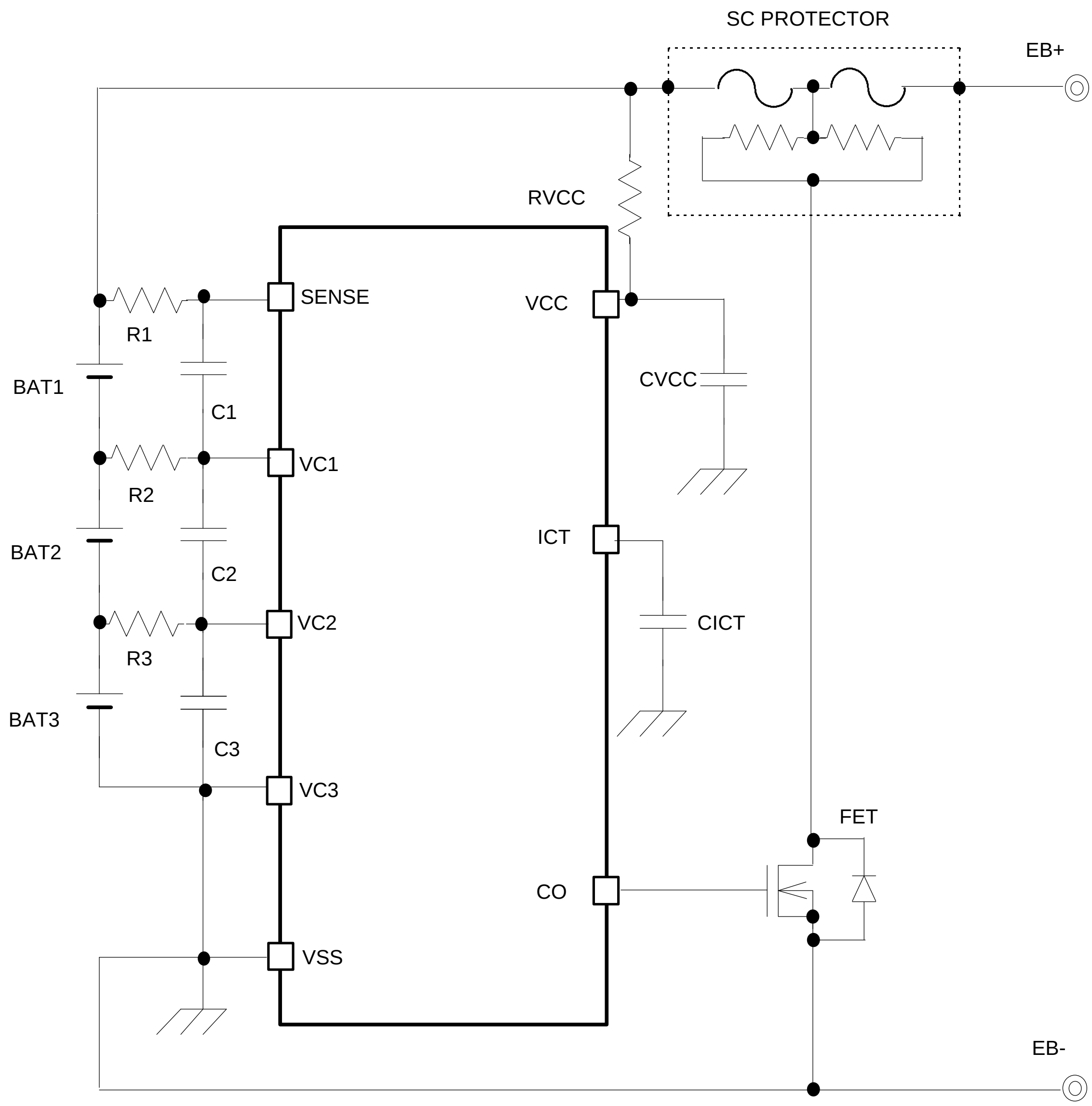


Figure 6 Battery Protection IC Connection Example 3

Table 7 Constants

Symbol	Min.	Recommended Value	Max.	Unit
R1 to R3	0	1 k	10 k	Ω
C1 to C3	0	0.1	1	μF
RVCC	0	100	1 k	Ω
CVCC	0	0.1	1	μF
CICT	0	0.1	1	μF

■ Battery Protection IC Connection Example 4 (for two cells)

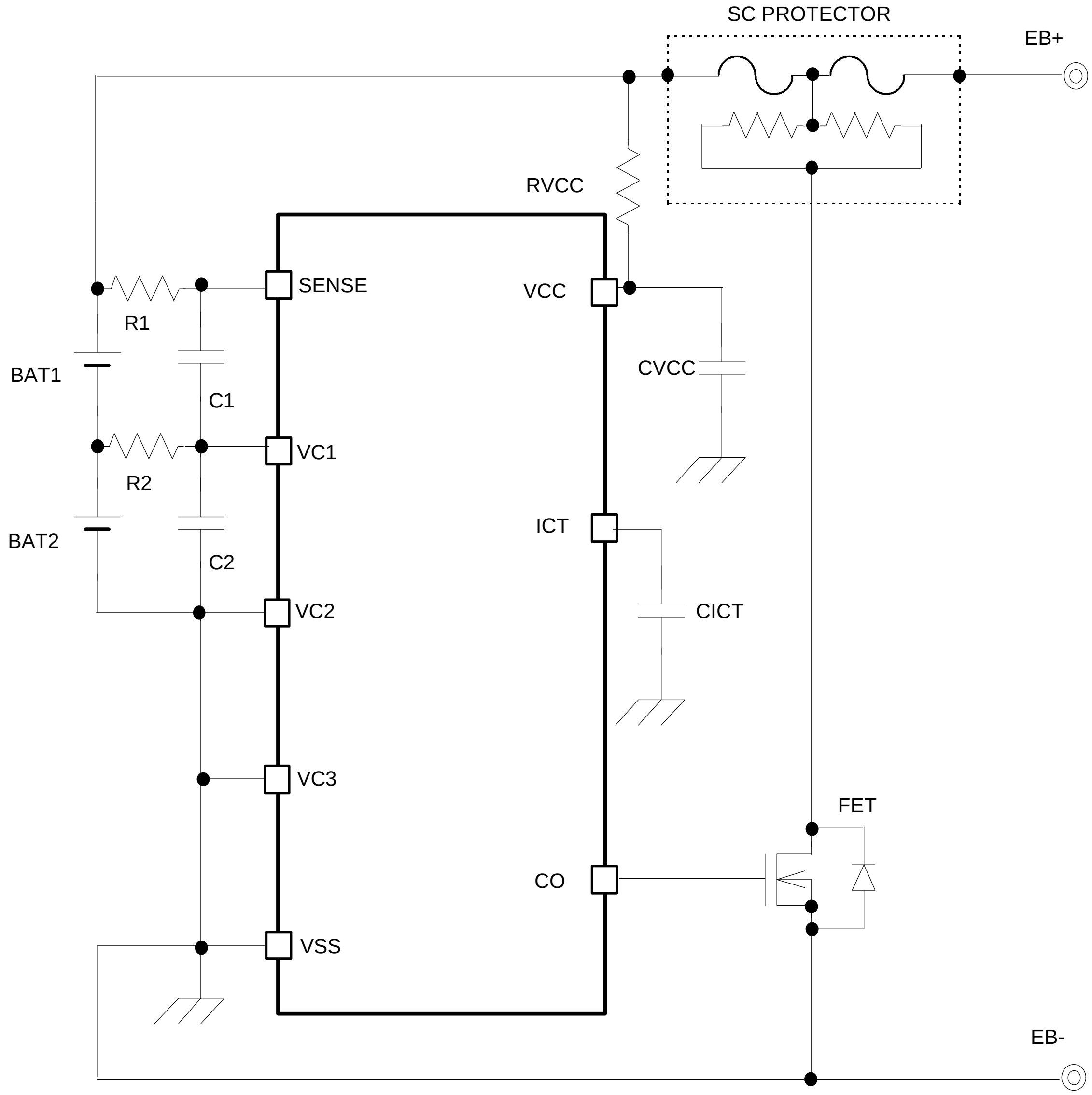


Figure 7 Battery Protection IC Connection Example 4

Table 8 Constants

Symbol	Min.	Recommended Value	Max.	Unit
R1, R2	0	1 k	10 k	Ω
C1, C2	0	0.1	1	µF
RVCC	0	100	1 k	Ω
CVCC	0	0.1	1	µF
CICT	0	0.1	1	µF

■ Battery Protection IC Connection Example 5 (for one cell)

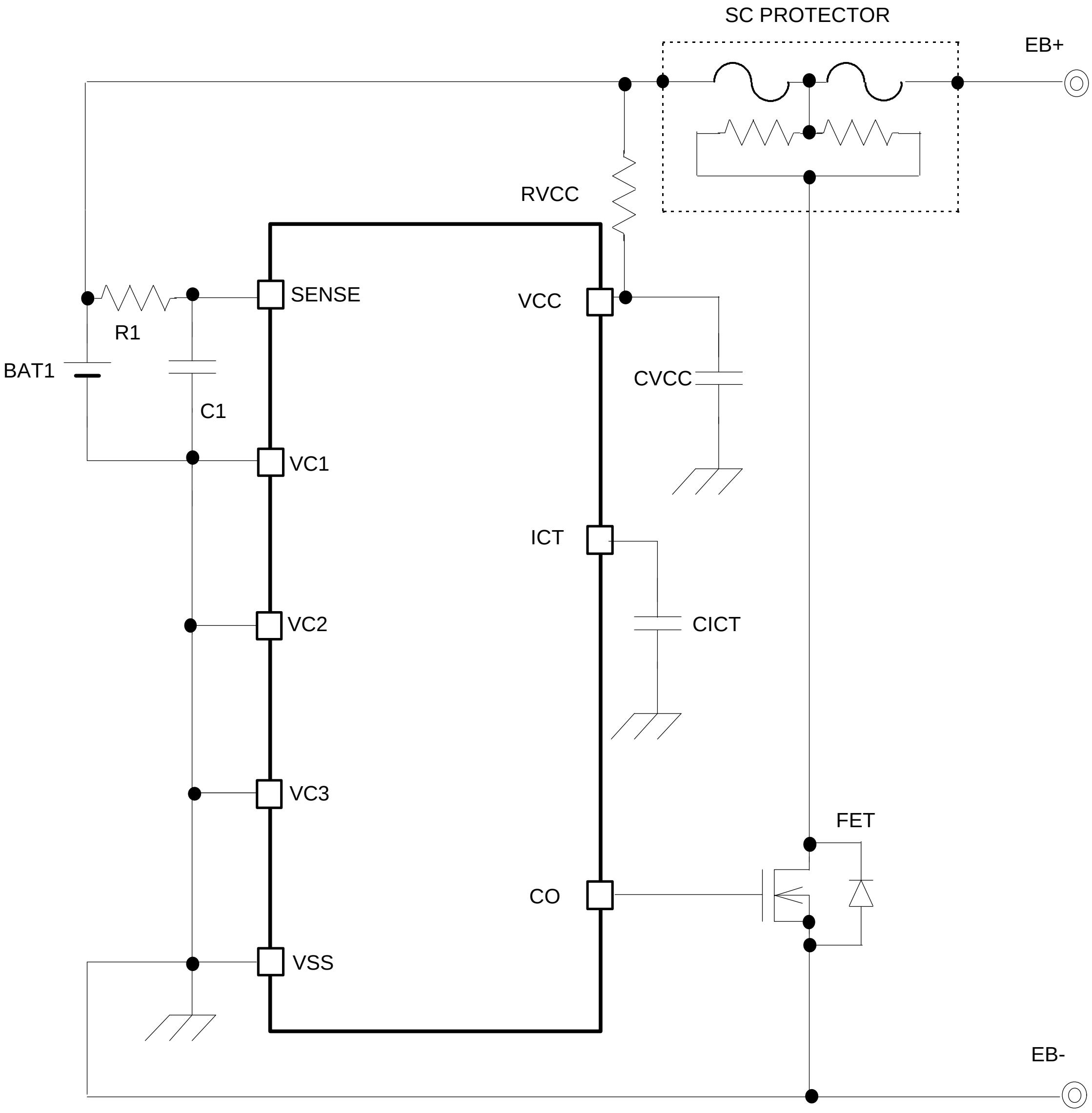


Figure 8 Battery Protection IC Connection Example 5

Table 9 Constants

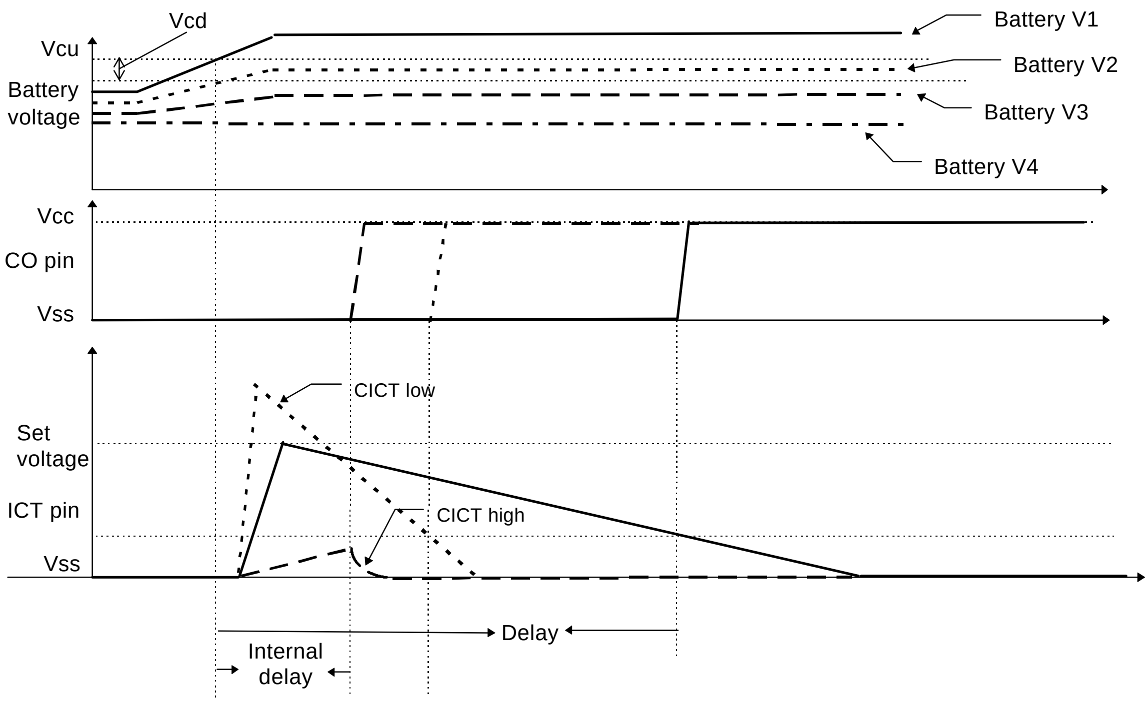
Symbol	Min.	Recommended Value	Max.	Unit
R1	0	1 k	10 k	Ω
C1	0	0.1	1	μF
RVCC	0	100	1 k	Ω
CVCC	0	0.1	1	μF
CICT	0	0.1	1	μF

■ Application Notes

- This IC charges the delay capacitor through the delay capacitor pin (ICT) immediately when the voltage of one of batteries V1 to V4 reaches the overcharge voltage. Therefore, setting the resistor connected to the VCC pin to any value greater than the recommended level causes a reduction in the IC power supply voltage because of charge current of the delay capacitor. This may lead to a malfunction. DO NOT set the resistor to above the recommended value. If you change the resistance, please consult us.

- DO NOT connect any of overcharged batteries. Even if only one overcharged battery is connected to this IC, the IC detects overcharge, then charge current flows to the delay capacitor through the parasitic diode between pins where the battery is not connected yet. This may lead to a malfunction. The battery connecting order is free. There is no problem even when a 0-V battery is connected.

For CMOS Output Active "H" and Nch Open Drain Models



- In this IC, the output logic of the CO pin is inverted after several milliseconds of internal delay if this IC is under the overcharge condition even ICT pin is either "VSS-shortcircuit," "VDD-shortcircuit" or "Open" status. If a delay time is not needed, connect the delay capacitor pin to VSS whenever possible.

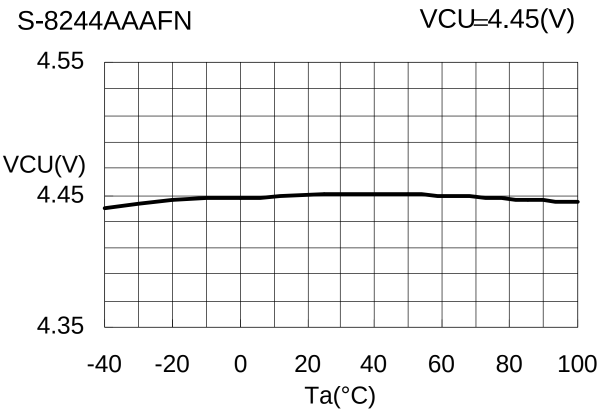
- Any position from V1 to V4 can be used when applying this IC for a one to three-cell battery. However, be sure to shortcircuit between pins not in use (SENSE-VC1, VC1-VC2, VC2-VC3, or VC3-VSS).

- SII claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.

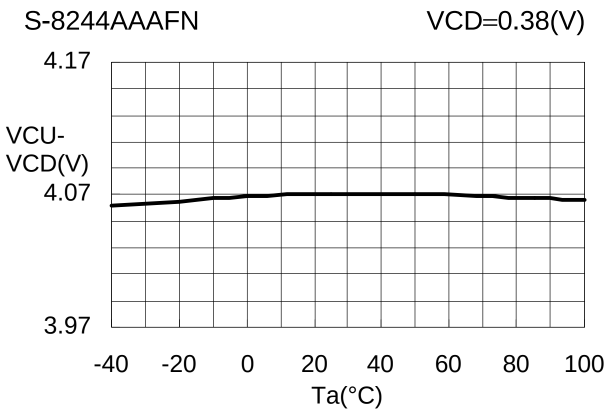
■ Typical Characteristic Data

1. Detection Voltage vs Temperature

Overcharge Detection Voltage vs Temperature

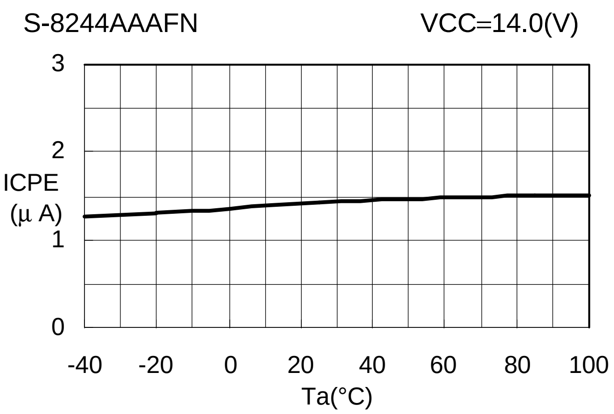


Overcharge Release Voltage vs Temperature

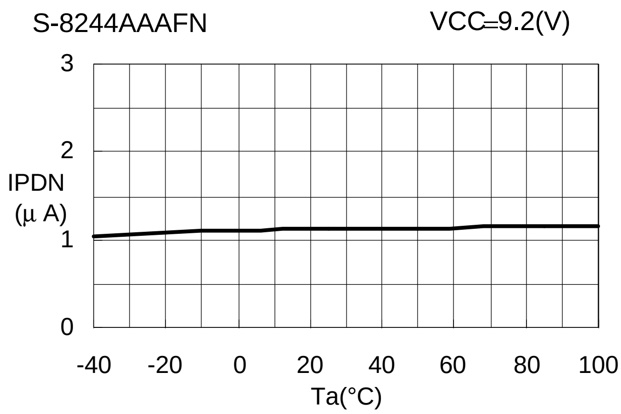


2. Current Consumption vs Temperature

Current Consumption during Normal Operation vs Temperature

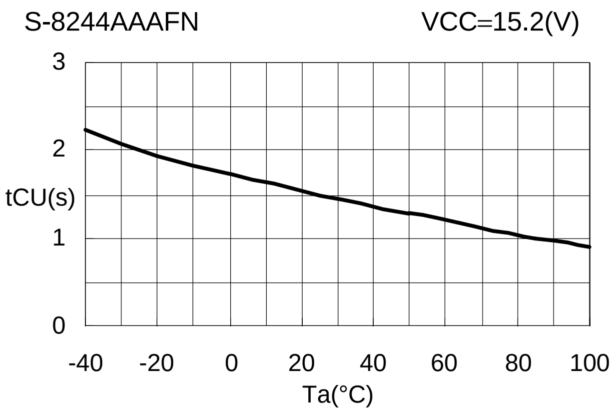


Current Consumption at Power Down vs Temperature



3. Delay Time vs Temperature

Overcharge Detection Delay Time vs Temperature



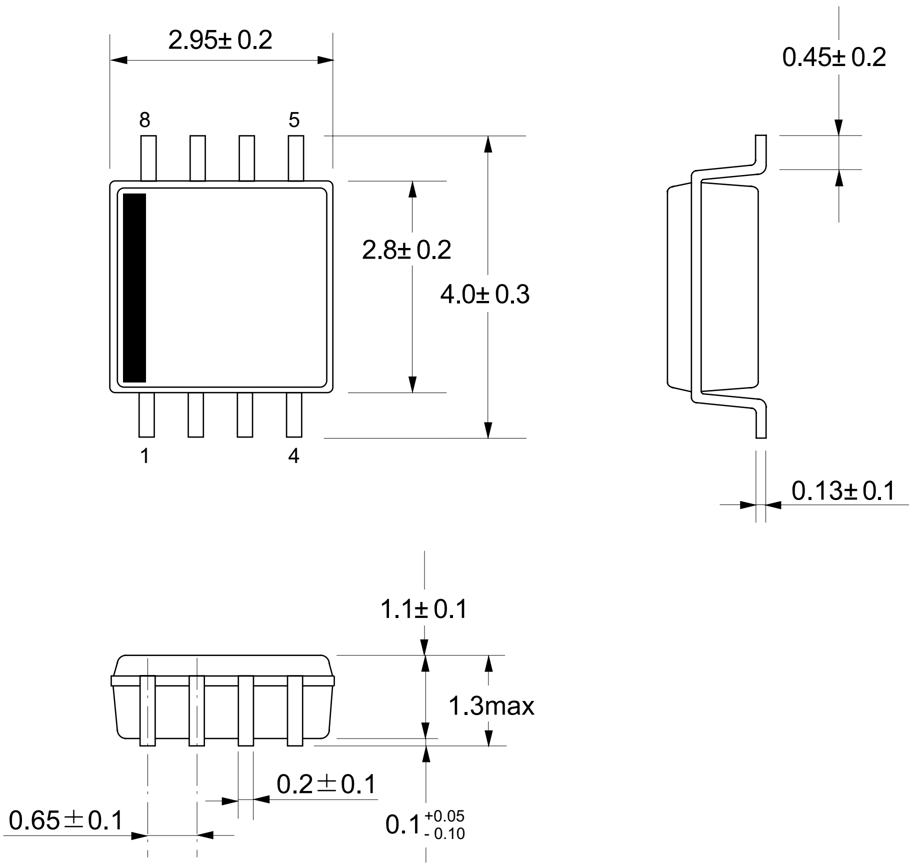
Please design all applications of the S-8244 Series with safety in mind.

■ 8-pin MSOP

FN008-A 990531

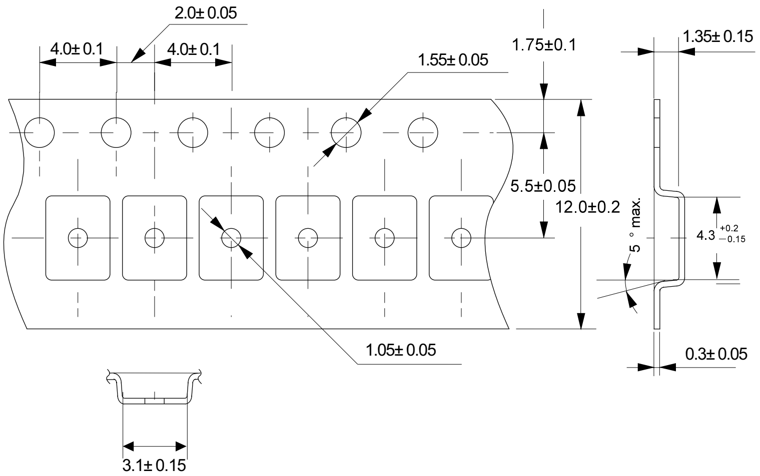
●Dimensions

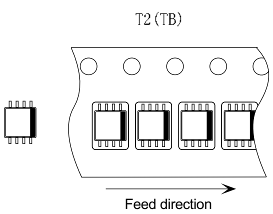
Unit:mm



No. : FN008-A-P-SD-1.0

●Taping Specifications

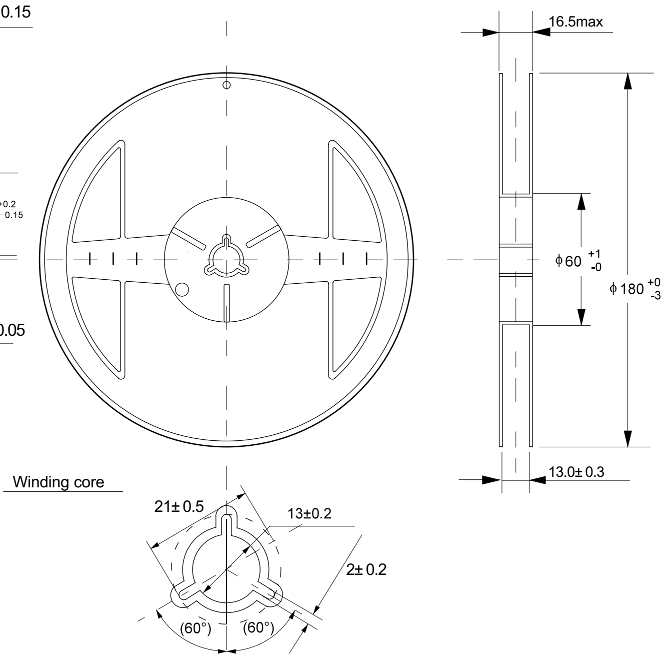




No. : FN008-A-C-SD-1.0

●Reel Specifications

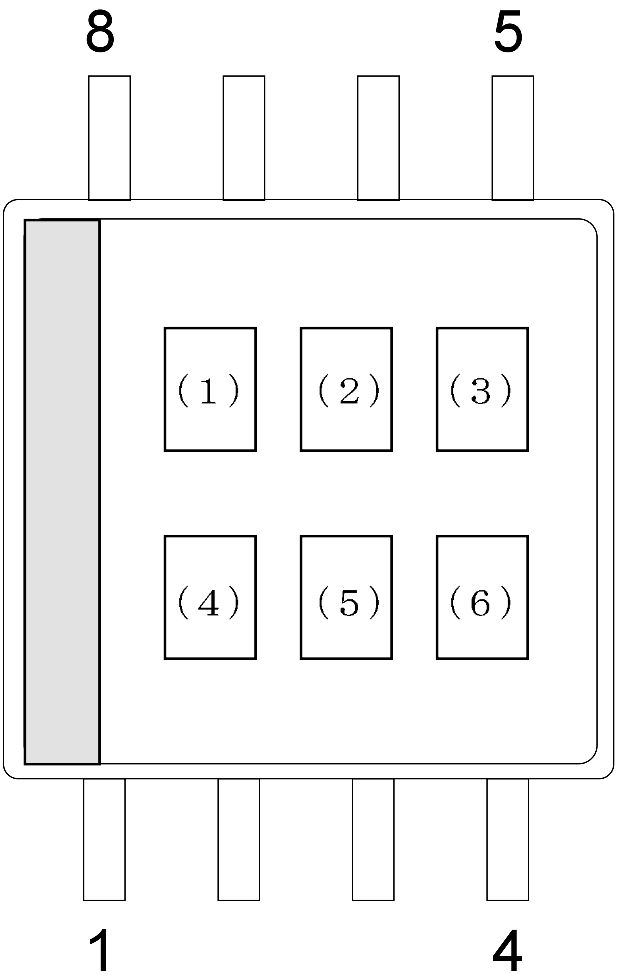
1 reel holds 3000 ICs.



No. : FN008-A-R-SD-1.0

■Markings

● **8-pin MSOP**



(1) to (3) : Product name (abbreviation)

(4) : Year of assembly

(5) : Month of assembly

(6) : Week of assembly