



# TDA1566

**I<sup>2</sup>C-bus controlled dual channel 46 W/2  $\Omega$ , single channel 92 W/1  $\Omega$  amplifier with load diagnostic features**

Rev. 02 — 20 August 2007

Product data sheet

## 1. General description

The TDA1566 is a car audio power amplifier with a complementary output stage realized in BCDMOS. The TDA1566 has two Bridge Tied Load (BTL) output stages and comes in a HSOP24 or DBS27P package.

The TDA1566 can be controlled with or without I<sup>2</sup>C-bus. With I<sup>2</sup>C-bus control gain settings per channel and diagnostic trigger levels can be selected. Failure conditions as well as load identification can be read with I<sup>2</sup>C-bus. The load identification detects whether the outputs of a BTL channel are connected with a DC or AC load and discriminates between a speaker load, a line driver load and an open (unconnected) load.

The TDA1566 can be configured in a single BTL mode and drive a 1  $\Omega$  load. For the single BTL mode it is necessary to connect on the Printed-Circuit Board (PCB) the outputs of both BTL channels in parallel.

## 2. Features

- Operates in I<sup>2</sup>C-bus mode and non-I<sup>2</sup>C-bus mode
- TH version: four I<sup>2</sup>C-bus addresses controlled by two pins; J version: two I<sup>2</sup>C-bus addresses controlled by one pin
- Two 4  $\Omega$  or 2  $\Omega$  capable BTL channels or one 1  $\Omega$  capable BTL channel
- Low offset
- Pop free off/standby/mute/operating mode transitions
- Speaker fault detection
- Selectable gain (26 dB and 16 dB)
- In I<sup>2</sup>C-bus mode:
  - ◆ DC load detection: open, short and speaker or line driver present
  - ◆ AC load (tweeter) detection
  - ◆ Programmable trigger levels for DC and AC load detection
  - ◆ Per channel programmable gain (26 dB and 16 dB, selectable per channel)
  - ◆ Selectable diagnostic levels for clip detection and thermal pre-warning
  - ◆ Selectable information on the DIAG pin for clip information of each channel separately and independent enabling of thermal-, offset- or load fault
- Independent short-circuit protection per channel
- Loss of ground and open  $V_P$  safe
- All outputs short-circuit proof to  $V_P$ , GND and across the load
- All pins short-circuit proof to ground
- Temperature controlled gain reduction at high junction temperatures

- Fault condition diagnosis per channel: short to ground, short to supply, shorted lead and speaker fault (wrongly connected)
- Low battery voltage detection
- TH version: pin compatible with the TDA8566TH1

3. Ordering information

Table 1. Ordering information

Type number	Package		Version
	Name	Description	
TDA1566TH	HSOP24	plastic, heatsink small outline package; 24 leads; low stand-off height	SOT566-3
TDA1566J	DBS27P	plastic DIL-bent-SIL (special bent) power package; 27 leads (lead length 6.8 mm)	SOT827-1

4. Block diagram

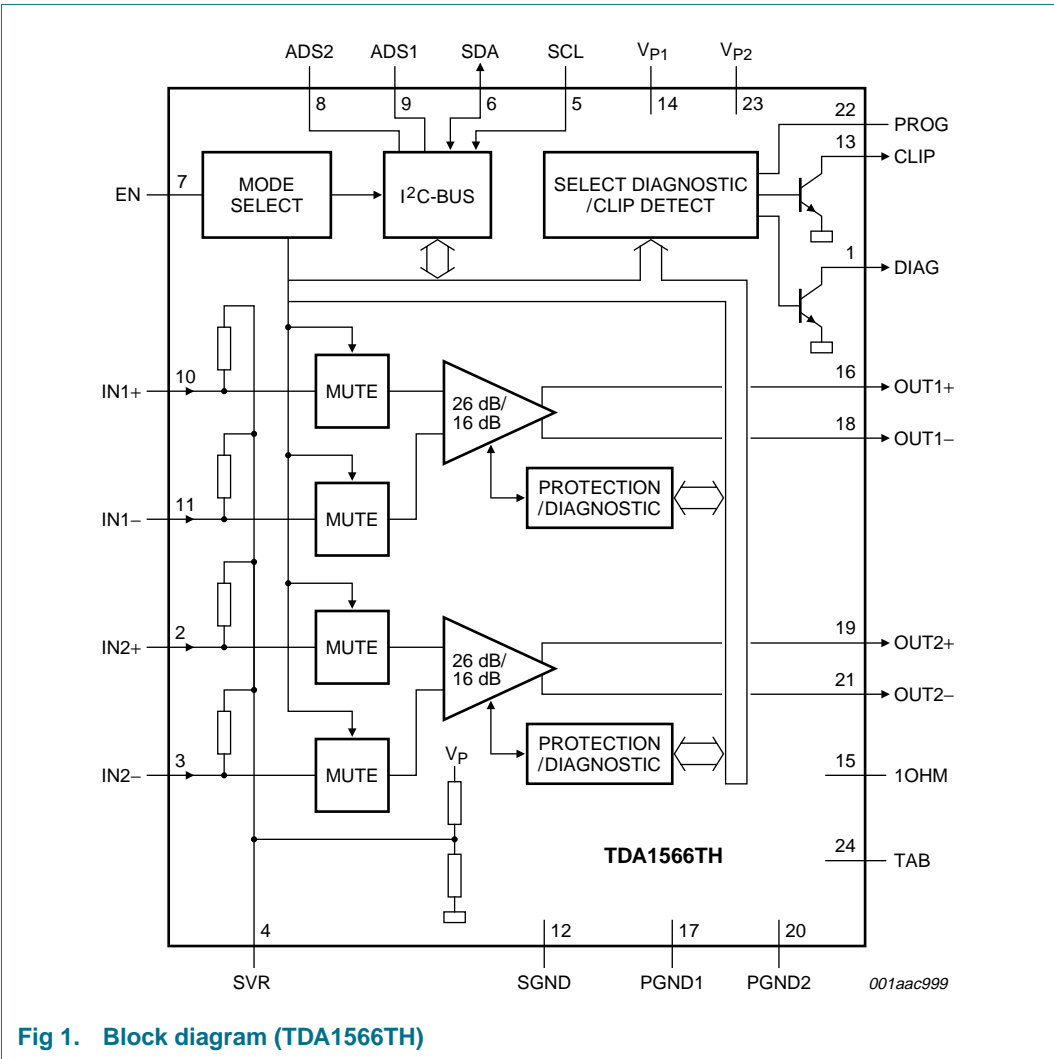
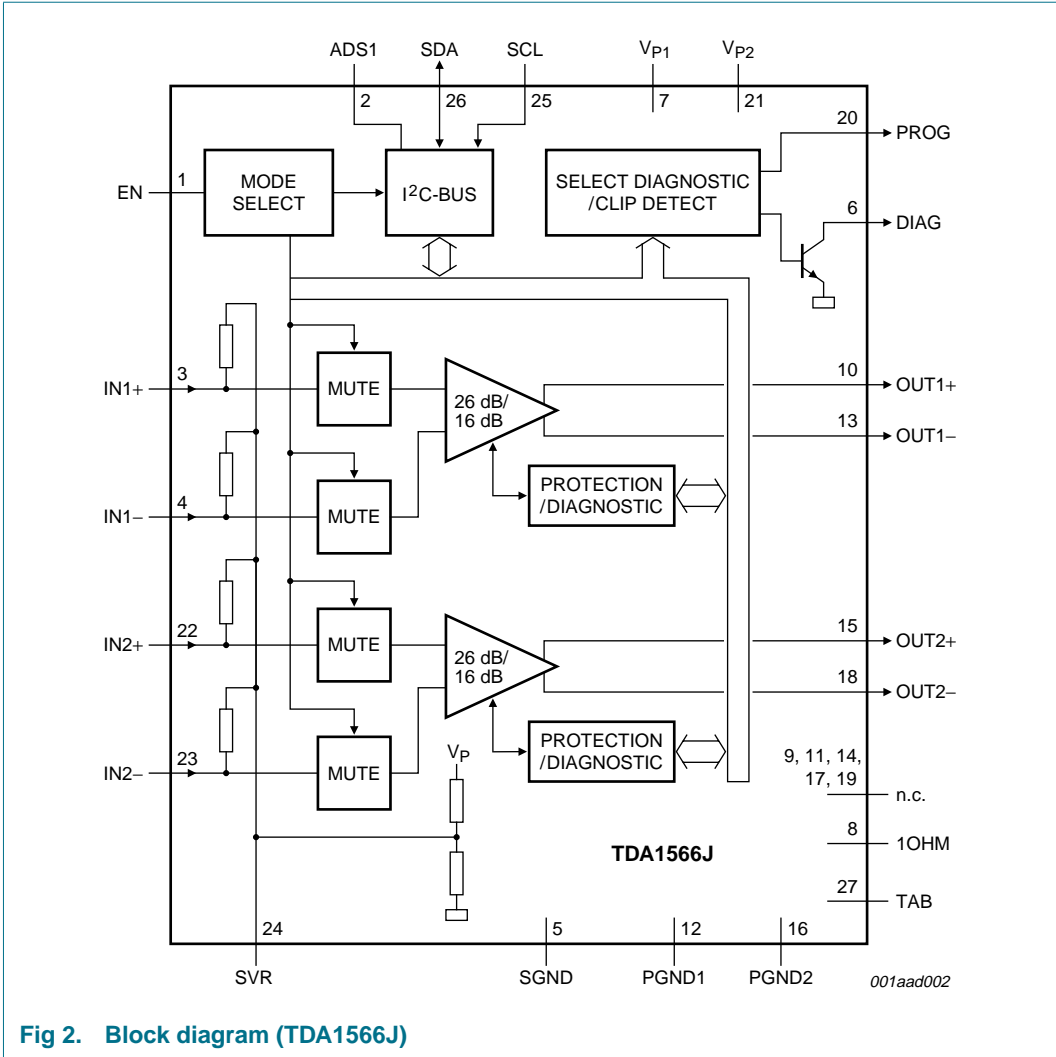
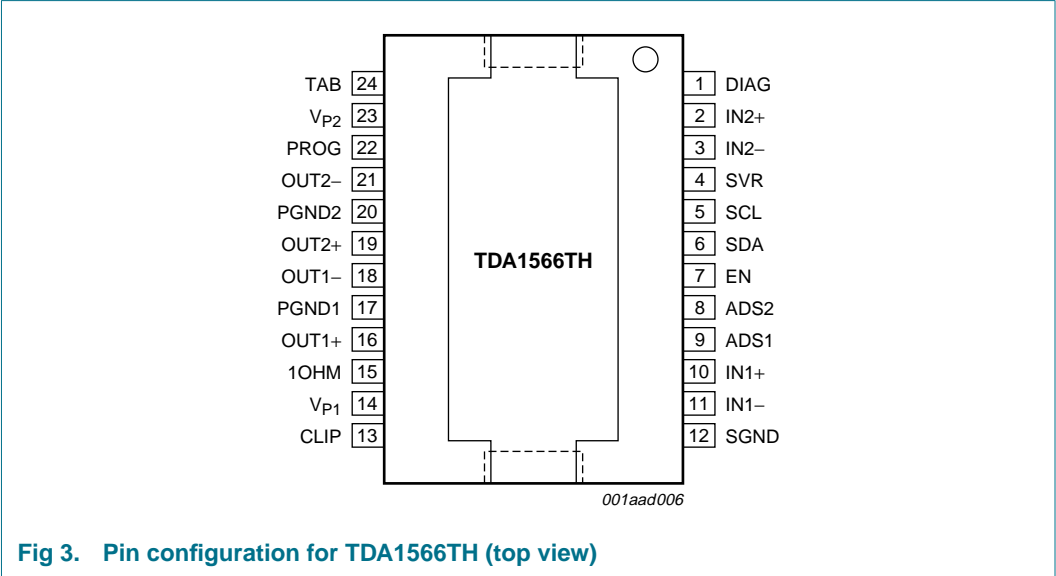


Fig 1. Block diagram (TDA1566TH)



5. Pinning information

5.1 Pinning



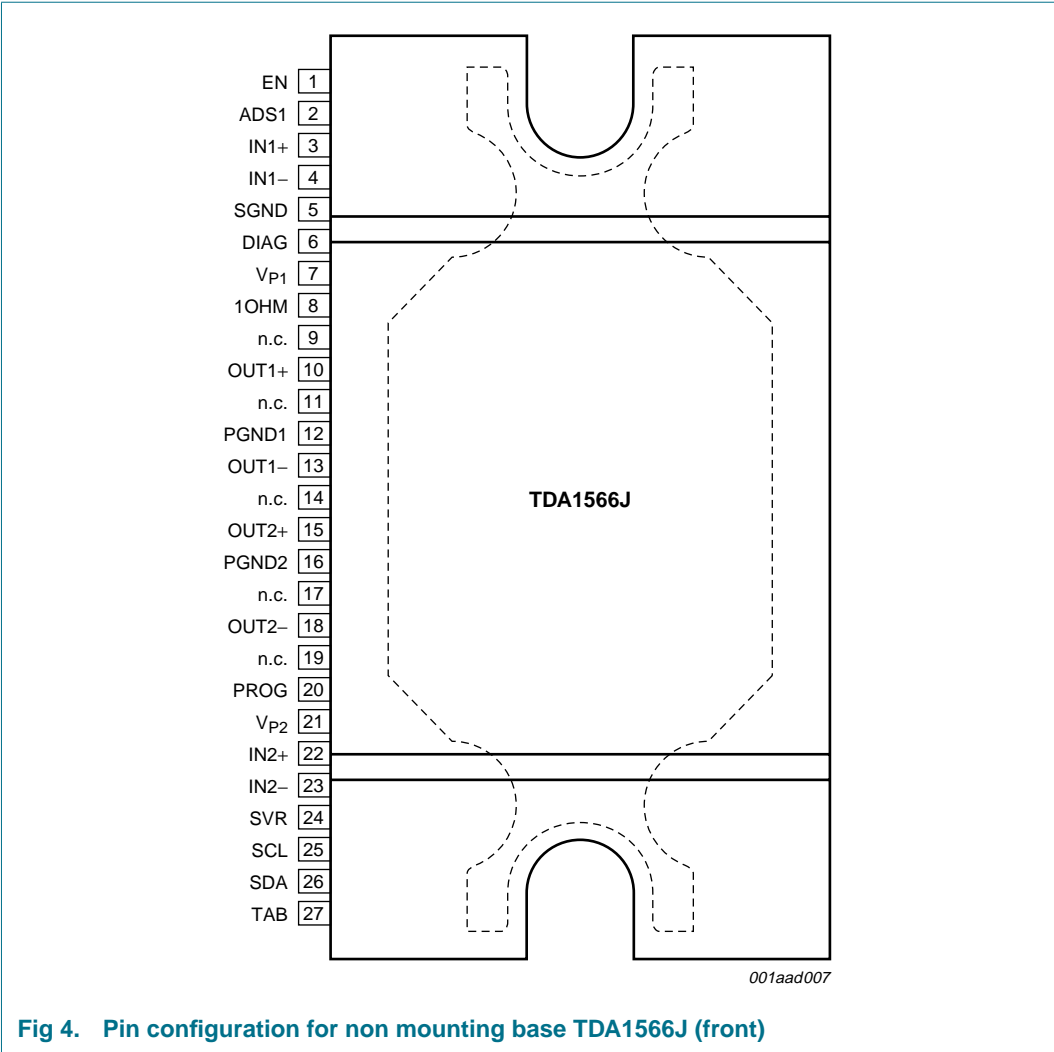


Fig 4. Pin configuration for non mounting base TDA1566J (front)

5.2 Pin description

Table 2. Pin description TDA1566TH

Symbol	Pin	Description
DIAG	1	diagnostic output
IN2+	2	positive input channel 2
IN2-	3	negative input channel 2
SVR	4	supply voltage ripple decoupling
SCL	5	I <sup>2</sup> C-bus clock input
SDA	6	I <sup>2</sup> C-bus data input/output
EN	7	enable input
ADS2	8	I <sup>2</sup> C-bus address select bit 2
ADS1	9	I <sup>2</sup> C-bus address select bit 1
IN1+	10	positive input channel 1
IN1-	11	negative input channel 1
SGND	12	signal ground

**Table 2.** Pin description TDA1566TH ...continued

Symbol	Pin	Description
CLIP	13	clip detect and temperature pre-warning output
V <sub>P1</sub>	14	supply voltage channel 1
1OHM	15	1 $\Omega$ select pin
OUT1+	16	positive output channel 1
PGND1	17	power ground channel 1
OUT1–	18	negative output channel 1
OUT2+	19	positive output channel 2
PGND2	20	power ground channel 2
OUT2–	21	negative output channel 2
PROG	22	program input/output
V <sub>P2</sub>	23	supply voltage channel 2
TAB	24	connect to PGND

**Table 3.** Pin description TDA1566J

Symbol	Pin	Description
EN	1	enable input
ADS1	2	I <sup>2</sup> C-bus address select bit 1
IN1+	3	positive input channel 1
IN1–	4	negative input channel 1
SGND	5	signal ground
DIAG	6	diagnostic output
V <sub>P1</sub>	7	supply voltage channel 1
1OHM	8	1 $\Omega$ select pin
n.c.	9	not connected
OUT1+	10	positive output channel 1
n.c.	11	not connected
PGND1	12	power ground channel 1
OUT1–	13	negative output channel 1
n.c.	14	not connected
OUT2+	15	positive output channel 2
PGND2	16	power ground channel 2
n.c.	17	not connected
OUT2–	18	negative output channel 2
n.c.	19	not connected
PROG	20	program input/output
V <sub>P2</sub>	21	supply voltage channel 2
IN2+	22	positive input channel 2
IN2–	23	negative input channel 2
SVR	24	supply voltage ripple decoupling

Table 3. Pin description TDA1566J ...continued

Symbol	Pin	Description
SCL	25	I <sup>2</sup> C-bus clock input
SDA	26	I <sup>2</sup> C-bus data input/output
TAB	27	connect to PGND

## 6. Functional description

### 6.1 General

Naming conventions used in this document:

- Reference to bits in instruction bytes: IBx[Dy] refers to bit Dy of instruction byte x
- Reference to bits in data bytes: DBx[Dy] refers to bit Dy of data byte x

#### 6.1.1 Mode selection

The ADS1 pin selects the I<sup>2</sup>C-bus or non-I<sup>2</sup>C-bus mode operation as listed in [Table 4](#). See [Section 6.1.6](#) and [Section 6.4.3](#) for the ADS1 pin functionality.

Table 4. Mode selection with the ADS1 pin

Pin	Non-I <sup>2</sup> C-bus mode	I <sup>2</sup> C-bus mode
ADS1	GND	open or via 33 kΩ to GND

[Table 5](#) lists the control for the I<sup>2</sup>C-bus mode operation. In I<sup>2</sup>C-bus mode the EN pin operates at CMOS compatible LOW and HIGH logic levels. With the EN pin LOW the TDA1566 is switched off and the quiescent current is at its lowest value. With the enable pin HIGH the operation mode of the TDA1566 is selected with IB1[D0] and IB1[D1]. The I<sup>2</sup>C-bus instruction and data bytes are described in [Section 6.4.2](#) and [Section 6.4.3](#).

Table 5. I<sup>2</sup>C-bus mode operation

EN pin	IB1[D0]	IB2[D0]	Operation mode
HIGH (> 2.6 V)	1	0	operating
	1	1	mute
	0	don't care	standby
LOW (< 1.0 V)	don't care	don't care	off

In non-I<sup>2</sup>C-bus mode the TDA1566 has 3 operation modes: off/mute/operation. The operation mode is selected with the EN pin. [Figure 5](#) displays the required voltage levels at the EN pin in I<sup>2</sup>C-bus and non-I<sup>2</sup>C-bus mode. For the voltage levels see [Section 9 "Characteristics"](#).

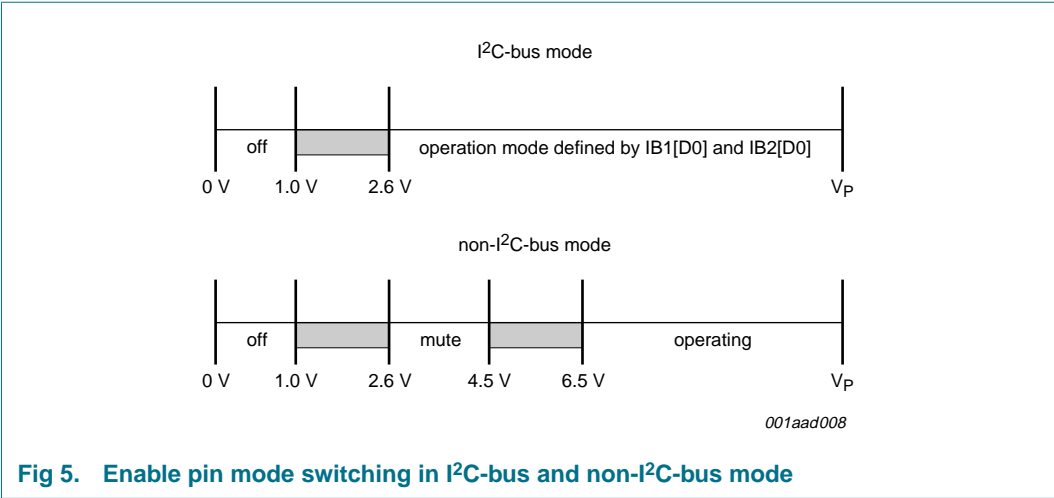


Fig 5. Enable pin mode switching in I<sup>2</sup>C-bus and non-I<sup>2</sup>C-bus mode

6.1.2 Gain selection

The TDA1566 features a 16 dB and a 26 dB gain setting. The 16 dB setting is referred to as line driver mode, the 26 dB setting is referred to as amplifier mode. Table 6 shows how the gain is selected.

Table 6. Gain select in I<sup>2</sup>C-bus and non-I<sup>2</sup>C-bus mode

Gain select	16 dB	26 dB
I <sup>2</sup> C-bus	IB3[D6] = 1	IB3[D6] = 0 <sup>[1]</sup>
	IB3[D5] = 1	IB3[D5] = 0 <sup>[2]</sup>
Non-I <sup>2</sup> C-bus	PROG connected with 1.5 kΩ to GND	PROG open <sup>[3]</sup>

- [1] Channel 1.
- [2] Channel 2.
- [3] Both channels.

6.1.2.1 I<sup>2</sup>C-bus mode

The gain is selected with IB3[D6] for channel 1 and IB3[D5] for channel 2. If the gain select is performed when the amplifier is muted, the gain select will be pop free. See Section 6.4.2 for the definition of the instruction bytes.

If DC load detection is used, IB1[D1] = 1, auto gain select is activated. Detection of an open load (see Section 6.2.1) will result in a line driver mode setting. If the load detection data is invalid, IB3[D5] and IB3[D6] will define the gain setting.

6.1.2.2 Non-I<sup>2</sup>C-bus mode

The gain for channel 1 and channel 2 is selected with the PROG pin. Leaving the pin unconnected selects 26 dB gain and connecting a resistor of 1500 Ω between the PROG pin and GND selects 16 dB gain.

When the amplifier is used in line driver mode loads of 2 Ω and 4 Ω can be driven. With a load larger than 25 Ω a Zobel network of 33 nF in series with 22 Ω should be connected between the amplifier output terminals. The Zobel network should be placed close to the output pins. To prevent instability in 1 Ω mode the amplifier must not be used in line driver mode with a load larger than 25 Ω.



### 6.1.3 Balanced and unbalanced input sources

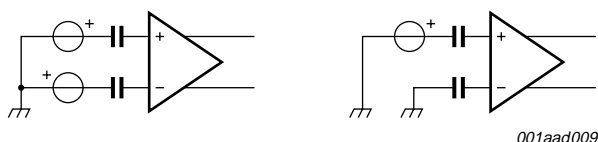
The TDA1566 accepts balanced as well as unbalanced input signals. [Table 7](#) and [Table 8](#) show the required hard or software setting and [Figure 6](#) shows the input source connection. Note that the unbalanced input source should be connected to the positive BTL channel input. Note that the J version accepts in non-I<sup>2</sup>C-bus mode only a balanced input source.

**Table 7. Balanced and unbalanced input source setting TDA1566TH**

Source	Balanced input source	Unbalanced input source
I <sup>2</sup> C-bus mode	IB3[D1] = 0	IB3[D1] = 1
Non-I <sup>2</sup> C-bus mode	ADS2 pin connected to GND	ADS2 pin unconnected

**Table 8. Balanced and unbalanced input source setting TDA1566J**

Source	Balanced input source	Unbalanced input source
I <sup>2</sup> C-bus mode	IB3[D1] = 0	IB3[D1] = 1
Non-I <sup>2</sup> C-bus mode	default	not selectable



**Fig 6. Balanced (left) and unbalanced (right) input source**

### 6.1.4 Single channel 1 $\Omega$ operation

The input and output pins for single channel 1  $\Omega$  operation are listed in [Table 9](#). The 1  $\Omega$  operation requires that on the PCB the output pins are shorted as indicated in [Table 9](#). In the 1  $\Omega$  operation the input signal is taken from channel 1.

To prevent instability in 1  $\Omega$  operation the amplifier must not be used in line driver mode with a load larger than 25  $\Omega$ .

**Table 9. Pinning for the single channel 1  $\Omega$  mode; TDA1566TH and TDA1566J**

Symbol	Pin (TDA1566TH)	Pin (TDA1566J)	Description single channel operation	Description dual channel operation
IN2+	2	22	disabled: connect IN2+ with 470 nF to SGND	positive input channel 2
IN2–	3	23	disabled: connect IN2+ with 470 nF to SGND	negative input channel 2
IN1+	10	3	positive input channel 1	positive input channel 1
IN1–	11	4	negative input channel 1	negative input channel 1
1OHM	15	8	1 $\Omega$ select pin connected to V <sub>P</sub>	1 $\Omega$ select pin connected to GND
OUT1+	16	10	positive output channel 1	positive output channel 1
OUT1–	18	13	negative output channel 1	negative output channel 1
OUT2+	19	15	shorted on board to OUT1–	positive output channel 2
OUT2–	21	18	shorted on board to OUT1+	negative output channel 2

### 6.1.5 Mute speed setting

In I<sup>2</sup>C-bus mode the amplifier can be muted slow (20 ms) or fast (0.1 ms). The mute speed is selected with IB2[D2].

See [Section 6.4.2](#) for the definition of the instruction bytes. [Table 10](#) lists the operation mode transitions where slow and fast mute are applied. The operation modes are described in [Section 6.1.1](#), [Table 5](#).

**Table 10. Mute speed setting**

Mode transition	I <sup>2</sup> C-bus mode	Non-I <sup>2</sup> C-bus mode
Mute to operating	slow mute	slow mute
Operating to mute	IB2[D2] = 0: slow mute IB2[D2] = 1: fast mute	slow mute
Operating to standby	slow mute	n.a.
Operating to off	fast mute	fast mute

### 6.1.6 Pins with double functions

**Table 11. Pins with double functions**

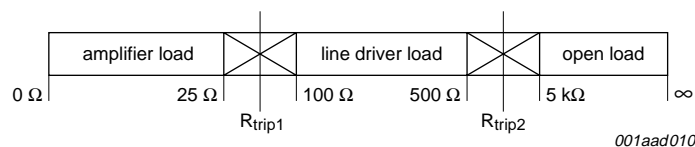
Pin	I <sup>2</sup> C-bus mode	Non-I <sup>2</sup> C-bus mode
PROG	load detection reference current programming, see <a href="#">Section 6.2.1</a> and <a href="#">6.2.2</a>	gain select, see <a href="#">Section 6.1.2</a>
ADS1	I <sup>2</sup> C-bus address select bit 1, see <a href="#">Section 6.4.1</a>	non-I <sup>2</sup> C-bus mode select, see <a href="#">Section 6.1.1</a>
ADS2 <sup>[1]</sup>	I <sup>2</sup> C-bus address select bit 2, see <a href="#">Section 6.4.1</a>	balanced/unbalanced input, see <a href="#">Section 3</a>
EN	chip enable, see <a href="#">Section 6.1.1</a>	mode select, see <a href="#">Section 6.1.1</a>

[1] TH version only.

## 6.2 Load identification (I<sup>2</sup>C-bus mode only)

### 6.2.1 DC load detection

The default setting IB1[D1] = 0 disables DC load detection. When the DC load detection is enabled with IB1[D1] = 1, an offset is slowly applied at the output of the amplifiers at the beginning of the start-up cycle. The DC load is measured and compared with  $R_{trip1}$  and  $R_{trip2}$  to distinguish between an amplifier load, line driver load or open load.  $R_{trip1}$  and  $R_{trip2}$  are set with resistor  $R_{PROG}$  (1 %) connected between the PROG pin and GND.



**Fig 7. DC load detection limits ( $R_{PROG} = 1500 \Omega/1\%$ )**

The relation between  $R_{PROG}$ ,  $R_{trip1}$  and  $R_{trip2}$  is approximated by (valid for  $R_{PROG}$  should be between 1.2 k $\Omega$  and 4 k $\Omega$ ):

$$R_{\text{trip1}} = 0.1 \times (R_{\text{PROG}} - 720) \, \Omega$$

$$R_{\text{trip2}} = 1.05 \times (R_{\text{PROG}} - 450) \, \Omega$$

$R_{\text{trip1}}$  and  $R_{\text{trip2}}$  levels presented refer to the advised value of 1500  $\Omega$ . Note that a shorted load will be interpreted as an amplifier load.

The result of the DC load detection is stored in DB1[D4] and DB1[D5] for channel 1 and in DB2[D4] and DB2[D5] for channel 2, see [Table 12](#).

**Table 12. Interpretation of DC load detection bits**

Open load bits DB1[D4] and DB2[D4]	Amplifier load bits DB1[D5] and DB2[D5]	DC load valid bit DB3[D3]	Description
0	0	1	amplifier load
0	1	1	line driver load
1	don't care	1	open load
Don't care	don't care	0	invalid DC load detection result

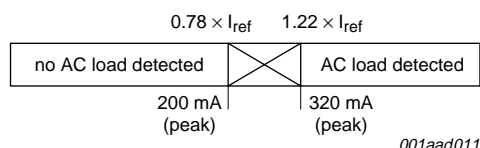
Note that the DC load bits are only valid if DB3[D3] = 1. The DC load detection valid bit is reset, DB3[D3] = 0, when the DC load detection is started with a not completely discharged SVR capacitor ( $V_{\text{SVR}} > 0.3 \text{ V}$ ) or when the DC load detection is interrupted by an engine start ( $V_P < 7.5 \text{ V}$  typical, see [Section 9](#)).

## 6.2.2 AC load detection

The AC load detection is used to detect if AC coupled speakers like tweeters are connected correctly during assembly. The detection starts when IB1[D2] changes from LOW to HIGH. A sine wave of a certain frequency (e.g. 19 kHz) needs to be applied to the inputs of the amplifier. The output voltage over the load impedance will cause an output current in the amplifier. Output currents larger than  $1.15 \times I_{\text{ref}}$  will set the AC load detection bit and no AC load is detected when the output current is less than  $0.85 \times I_{\text{ref}}$ , see [Figure 8](#). The reference current  $I_{\text{ref}}$  is set with an external resistor  $R_{\text{PROG}}$  (1 %) connected between the PROG pin and GND. The relation between  $R_{\text{PROG}}$  and  $I_{\text{ref}}$  is given by:

$$I_{\text{ref}} = 390 / R_{\text{PROG}} \text{ [A]} \text{ (valid for } R_{\text{PROG}} \text{ between } 1.2 \text{ k}\Omega \text{ and } 4 \text{ k}\Omega \text{)}.$$

To set the AC load detection bit the peak output current must pass the  $1.15 \times I_{\text{ref}}$  threshold three times. The three 'threshold cross' counter is used to prevent false AC load detection caused by switching the input signal on or off. To reset the slope counter, IB1[D2] needs to be reset. With  $R_{\text{PROG}} = 1500 \, \Omega$  the current thresholds are set to 200 mA and 320 mA.



**Fig 8. AC load detection limits**

The levels presented refer to the advised value of 1500  $\Omega$ .

For instance at an output voltage of 4 V peak the total impedance must be less than 10  $\Omega$  to detect the AC coupled load or more than 13.4  $\Omega$  to guarantee no connected AC load is detected. Values between 10  $\Omega$  and 13.4  $\Omega$  cannot be recognized. The result of the AC load detection is shown in DB1[D7] for channel 1 and DB2[D7] for channel 2.

When IB1[D2] = 1 the AC load detection is enabled. The AC load detection can only be performed after the amplifier has completed its start-up cycle and will not conflict with the DC load detection. The default setting of IB1[D2] = 0 disables AC load detection.

Note: in the 1  $\Omega$  mode  $I_{ref}$  is doubled, so  $I_{ref} = 2 \times 390 / R_{PROG}$  [A].

## 6.3 Diagnostic

### 6.3.1 Diagnostic table

The available diagnostic information is shown in [Table 13](#) and [Table 14](#). Refer to [Table 17](#) and [Table 18](#) for the bitmap of the instruction and data bytes.

DIAG and CLIP have an open-drain output, are active LOW and must have an external pull-up resistor to an external voltage.

DIAG shows fixed information and via the I<sup>2</sup>C-bus selectable information. This information will be seen on DIAG and CLIP as a logical OR. The temperature pre-warning diagnostic and clip information is available on the CLIP.

In case of a failure, DIAG will remain LOW and the microprocessor can read out the failure information via the I<sup>2</sup>C-bus. The I<sup>2</sup>C-bus bits are set on a failure and will be reset with the I<sup>2</sup>C-bus read command. Even when the failure is removed the microprocessor will know what was wrong by reading the I<sup>2</sup>C-bus. The consequence of this procedure is that during the I<sup>2</sup>C-bus read old information is read. Most actual information will be gathered with 2 read commands after each other.

DIAG will give actual diagnostic information (when selected). When a failure is removed, DIAG will be released instantly, independently of the I<sup>2</sup>C-bus latches.

**Table 13. Available diagnostic data TH version**

Diagnostic	I <sup>2</sup> C-bus mode		Non-I <sup>2</sup> C-bus mode	
	DIAG	CLIP	DIAG	CLIP
POR	yes	no	no	no
Low $V_P$ or load dump detection	yes	no	yes	no
Clip detection	selectable	yes	no	yes
Temperature pre-warning	selectable	yes	no	yes
Short	selectable	no	yes	no
Speaker protection	selectable	no	yes	no
Offset detection	selectable	no	yes	no
Maximum temperature protection	yes	no	yes	no
Load detection	no	no	no	no

Note that in the J version no CLIP pin is available.

**Table 14. Available diagnostic data J version**

Diagnostic	I <sup>2</sup> C-bus mode	Non-I <sup>2</sup> C-bus mode
	DIAG	DIAG
POR	yes	no
Low V <sub>P</sub> or load dump detection	yes	yes
Clip detection	selectable	yes
Temperature pre-warning	selectable	yes
Short	selectable	yes
Speaker protection	selectable	yes
Offset detection	selectable	no
Maximum temperature protection	yes	yes
Load detection	no	no

Following diagnostic information is only available via I<sup>2</sup>C-bus:

- DC and AC load detection results, see [Section 6.2](#)
- DB3[D4] is set when the DC settling of the amplifier has almost completed and the SVR voltage has risen to a value of V<sub>P</sub> / 2 or above, see [Section 6.5.1](#)

### 6.3.2 Diagnostic level settings

**Table 15. Clip and temperature pre-warning level setting**

Setting	I <sup>2</sup> C-bus mode	Non-I <sup>2</sup> C-bus mode
Clip detection level	IB2[D7] = 0 selects 3 %	3 %
	IB2[D7] = 1 selects 7 %	
Temperature pre-warning level	IB3[D4] = 0 selects 145 °C	145 °C
	IB3[D4] = 1 selects 122 °C	

### 6.3.3 Temperature pre-warning

If in I<sup>2</sup>C-bus mode the average junction temperature reaches a by I<sup>2</sup>C-bus selectable level, the pre-warning will be activated resulting in a LOW CLIP pin.

In non-I<sup>2</sup>C mode the thermal pre-warning is set on 145 °C.

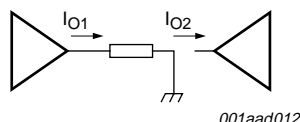
In the TH version the thermal pre-warning is available on the CLIP pin in I<sup>2</sup>C-bus mode and non-I<sup>2</sup>C mode.

In the J version the thermal pre-warning is available on the DIAG pin in non-I<sup>2</sup>C-bus mode. In I<sup>2</sup>C-bus mode the presence of the thermal pre-warning on the DIAG is selected with IB1[D4], see [Section 6.3.1](#) and [Section 6.4.2](#).

If the temperature increases above the pre-warning level, the temperature controlled gain reduction will be activated for both channels resulting in a lower output power. If this does not reduce the average junction temperature, both channels will be switched off at the absolute maximum temperature T<sub>off</sub>, typical 175 °C.

### 6.3.4 Speaker protection

To prevent damage of the speaker when one side of the speaker is connected to ground, see [Figure 9](#), a 'missing current protection' is implemented.



**Fig 9. Speaker protection condition**

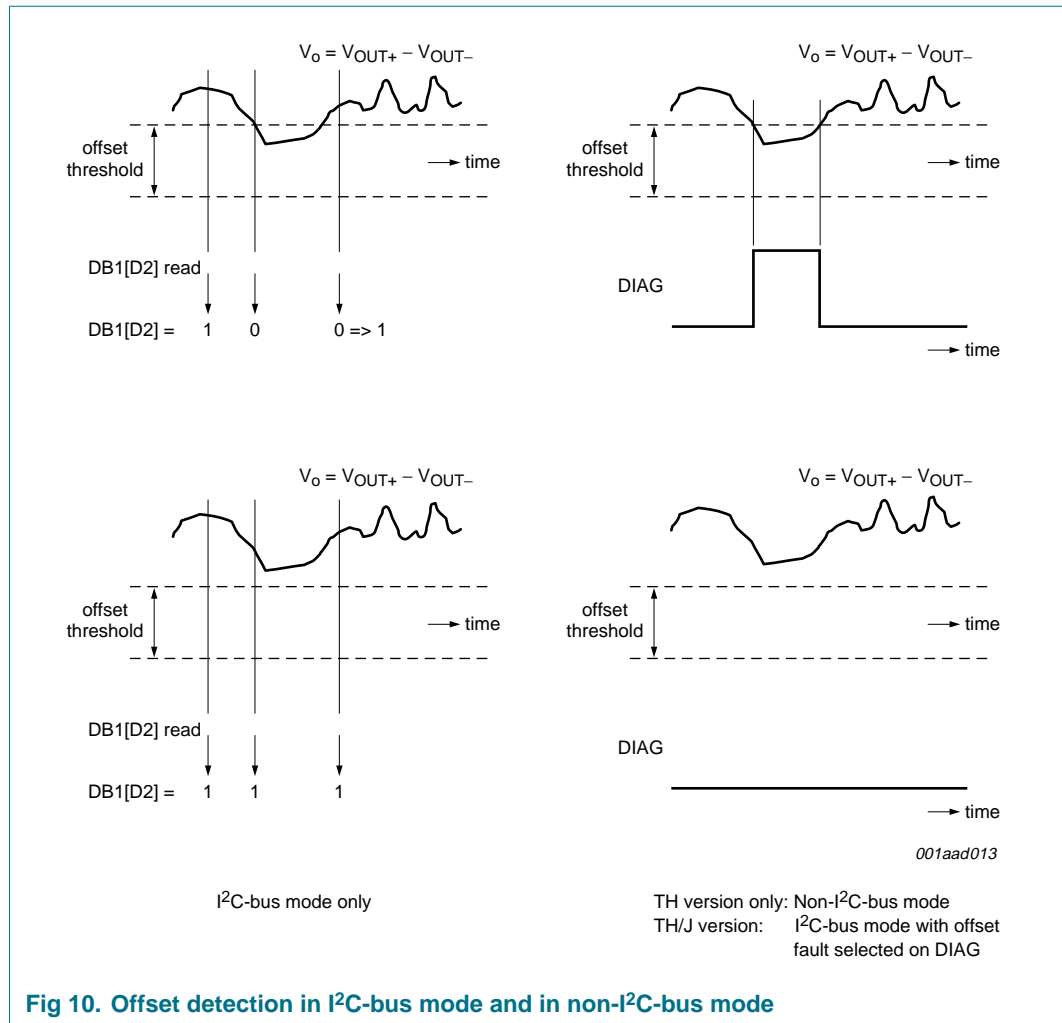
When in one BTL channel the absolute value of the current through the output terminals differ, so  $|I_{O1}| \neq |I_{O2}|$ , a fault condition is assumed, and the BTL channel will be switched off. The 'speaker protection active' diagnosis options for I<sup>2</sup>C-bus and non-I<sup>2</sup>C-bus mode are listed in [Table 13](#).

### 6.3.5 Offset detection

The offset detection can be performed with no input signal (for instance when the DSP is in mute after a start-up) or with input signal.

In I<sup>2</sup>C-bus mode the offset bits DB1[D2] and DB2[D2] are set by executing a read command. The offset bits will be reset when the BTL output voltage  $V_o = |V_{OUT1+} - V_{OUT1-}|$  enters the offset threshold window of 1.5 V. The offset bits are read with a 2nd read command.

In non-I<sup>2</sup>C-bus mode (or in I<sup>2</sup>C-bus mode with offset diagnostic selected on DIAG) DIAG will be pulled LOW if the BTL output voltage is more than 1.5 V.



## 6.4 I<sup>2</sup>C-bus operation

### 6.4.1 I<sup>2</sup>C-bus address with hardware address select

Table 16. I<sup>2</sup>C-bus address table TH version

ADS1	ADS2	A6	A5	A4	A3	A2	A1	A0	R/W <sup>[1]</sup>
open	open	1	1	0	1	0	0	0	1/0
	GND	1	1	0	1	0	0	1	1/0
33 kΩ to GND	open	1	1	0	1	0	1	0	1/0
	GND	1	1	0	1	0	1	1	1/0

[1] 0 = write to TDA1566TH; 1 = read from TDA1566TH.

Table 17. I<sup>2</sup>C-bus address table J version

ADS1	A6	A5	A4	A3	A2	A1	A0	R/W <sup>[1]</sup>
open	1	1	0	1	0	0	1	1/0
33 kΩ to GND	1	1	0	1	0	1	1	1/0

[1] 0 = write to TDA1566J; 1 = read from TDA1566J.

### 6.4.2 Instruction bytes

If R/W bit = 0, the TDA1566 expects 3 instruction bytes; IB1, IB2 and IB3. After a power-on reset, all instruction bits are set to zero. In 1  $\Omega$  mode the instruction bits of channel 1 are used. The instruction bits labelled 'reserved for test' should be set to zero.

**Table 18. Instruction bytes**

Bit	Instruction byte IB1		Instruction byte IB2		Instruction byte IB3	
D7	0	slow start enable	0	clip detect level on 3 %	reserved for test	
	1	slow start disable	1	clip detect level on 7 %		
D6	0	channel 1 no clip detect on DIAG	reserved for test		0	channel 1 26 dB gain
	1	channel 1 clip detect on DIAG			1	channel 1 16 dB gain
D5	0	channel 2 no clip detect on DIAG	reserved for test		0	channel 2 26 dB gain
	1	channel 2 clip detect on DIAG			1	channel 2 16 dB gain
D4	0	no temperature pre-warning on DIAG	0	speaker protection or short on DIAG	0	temperature pre-warning on 145 °C
	1	temperature pre-warning on DIAG	1	no speaker protection or short on DIAG	1	temperature pre-warning on 122 °C
D3	reserved for test		reserved for test		0	channel 1 enabled
					1	channel 1 disabled
D2	0	AC load detection disabled; detection slope counter reset	0	slow mute (20 ms)	0	channel 2 enabled
	1	AC load detection enabled	1	fast mute (0.1 ms)	1	channel 2 disabled
D1	0	DC load detection disabled	0	offset fault on DIAG	0	balanced input
	1	DC load detection enabled	1	no set fault on DIAG	1	unbalanced input
D0	0	TDA1566 in standby	0	channel 1 and channel 2 operating	reserved for test	
	1	TDA1566 in mute or operating (see IB2[D0])	1	channel 1 and channel 2 muted		

### 6.4.3 Data bytes

If R/W = 1, the TDA1566 will send 3 data bytes to the microprocessor: DB1, DB2, and DB3. All short diagnostic and offset detect bits are latched. All bits are reset after a read operation except DB1[D7], DB2[D7], DB1[D4], DB2[D4], DB1[D5] and DB2[D5]. DB1[D2] and DB2[D2] are set after a read operation, see [Section 6.3.5](#). DB1[D7] and DB2[D7] are reset when IB1[D2] is LOW. In 1  $\Omega$  mode the diagnostic information will be shown in DB1. The content of the bits 'reserved for test' should be ignored.



Table 19. Data bytes

Bit	Data byte DB1 channel 1		Data byte DB2 channel 2		Data byte DB3 both channels	
D7	0	no AC load detected	0	no AC load detected	0	TDA1566 in mute or operating (IB1[D0] = 1)
	1	AC load detected	1	AC load detected	1	power-on reset has occurred or TDA1566 in standby (IB1[D0] = 0)
D6	0	no speaker fault	0	no speaker fault	0	below maximum temperature
	1	speaker fault	1	speaker fault	1	maximum temperature protection activated
D5	0	amplifier load (D4 = 0) not valid (D4 = 1)	0	amplifier load (D4 = 0) not valid (D4 = 1)	0	no temperature warning
	1	line driver load (D4 = 0) open load (D4 = 1)	1	line driver load (D4 = 0) open load (D4 = 1)	1	temperature pre-warning active
D4	0	amplifier load (D5 = 0) line driver load (D5 = 1)	0	amplifier load (D5 = 0) line driver load (D5 = 1)	0	SVR below $V_P / 2$
	1	not valid (D5 = 0) open load (D5 = 1)	1	not valid (D5 = 0) open load (D5 = 1)	1	SVR above $V_P / 2$
D3	0	no shorted load	0	no shorted load	0	invalid DC load data
	1	shorted load	1	shorted load	1	valid DC load data
D2	0	no output offset	0	no output offset	reserved for test	
	1	output offset detected	1	output offset detected		
D1	0	no short to $V_P$	0	no short to $V_P$	reserved for test	
	1	short to $V_P$	1	short to $V_P$		
D0	0	no short to ground	0	no short to ground	reserved for test	
	1	short to ground	1	short to ground		

## 6.5 Timing waveforms

### 6.5.1 Start-up and shutdown

To prevent switch-on or switch-off pop noise, the capacitor on the SVR pin  $C_{SVR}$  is used for smooth start-up and shutdown. During start-up and shutdown the output voltage tracks the SVR voltage. With IB1[D7] = 0 the time constant made with the SVR capacitor can be increased to reduce turn on transients at the load. Consequently the start-up time  $t_{d(mute\_off)}$  increases with approximately 420 ms ( $V_P = 14.4$  V,  $C_{SVR} = 22$   $\mu$ F,  $T_{amb} = 25$  °C). Note that in non-I<sup>2</sup>C-bus mode the IB1[D7] = 0 setting will be used.

Increasing  $C_{SVR}$  results in a longer start-up and shutdown time. Note that a larger SVR capacitor value will also result in a longer DC load detection cycle.

For optimized pop performance it is recommended to keep the amplifier in mute until the SVR voltage has reached its final level.

When the amplifier is switched off by pulling the EN pin LOW the amplifier is muted (fast mute) and the capacitor on the SVR pin will be discharged. With an SVR capacitor of 22  $\mu$ F the off current is reached 2 s after the EN pin is switched to zero.

Start-up and shutdown in I<sup>2</sup>C-bus mode is shown in [Figure 11](#) and explained in [Table 20](#).

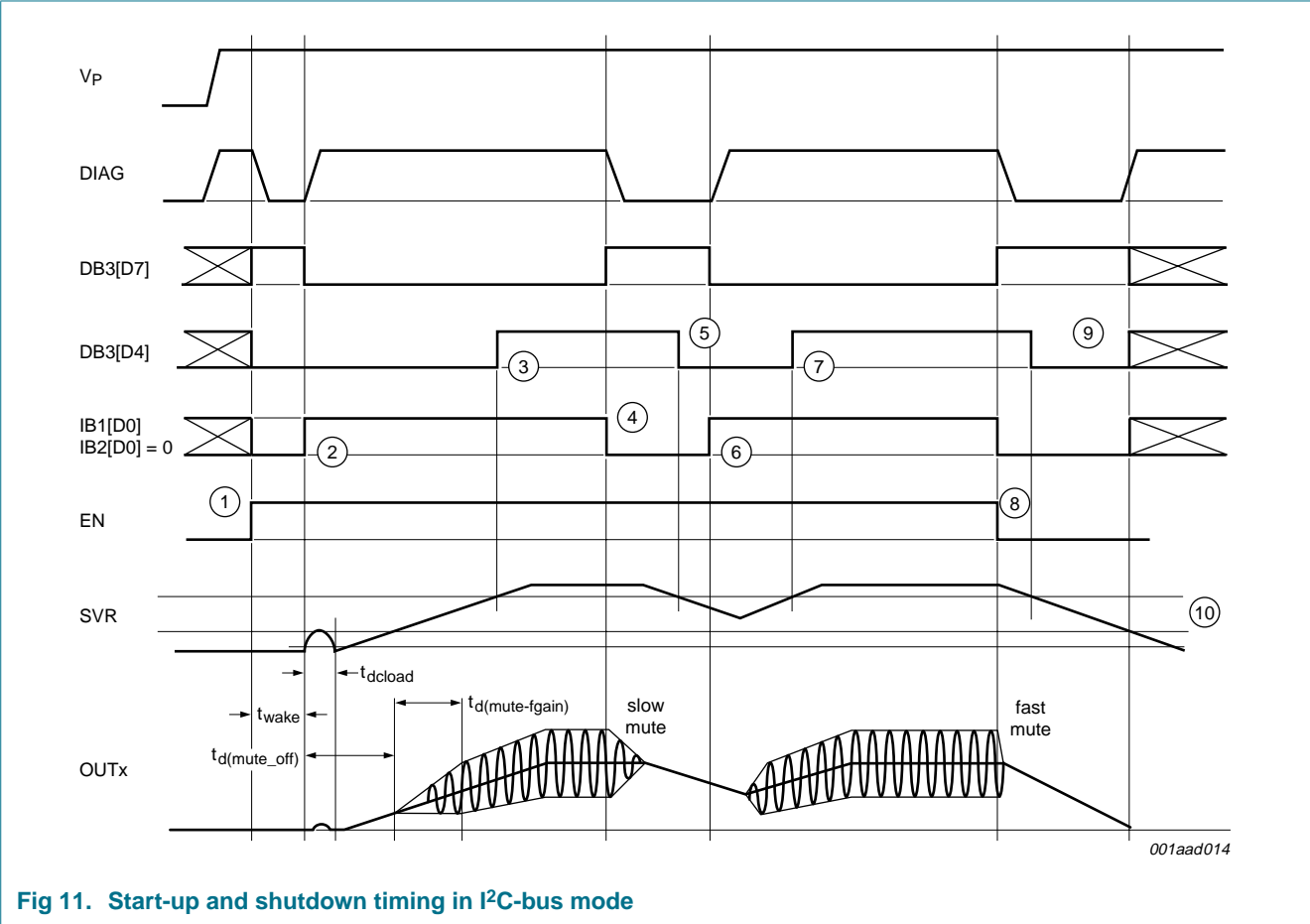


Fig 11. Start-up and shutdown timing in I<sup>2</sup>C-bus mode

Table 20. Start-up and shutdown timing in I<sup>2</sup>C-bus mode

Step	Action	Result
1	TDA1566 is enabled with EN	TDA1566 from off to standby DB3[D7] is set and DIAG is pulled LOW to indicate power-on reset
2	TDA1566 is switched from standby to operating with IB1[D0] = 1	DIAG is released DB3[D7] is reset SVR capacitor is charged, OUTx voltage tracks SVR voltage gradual increase of gain; when the SVR voltage increases above a threshold of 2 V + 2V <sub>BE</sub> the amplifiers operate at full gain

Table 20. Start-up and shutdown timing in I<sup>2</sup>C-bus mode ...continued

Step	Action	Result
3		SVR voltage has become larger than $V_P / 2$ resulting in setting DB3[D4]
4	TDA1566 is switched from operating to standby with IB1[D0] = 0	DIAG is pulled LOW SVR is discharged, OUTx voltage tracks SVR voltage amplifier is slow muted
5		SVR voltage has dropped below $V_P / 2$ resulting in resetting DB3[D4]
6	TDA1566 is switched from standby to operating with IB1[D0] = 1	see step 2
7		see step 3
8	TDA1566 is disabled with EN	DIAG is pulled LOW amplifier is fast muted SVR is discharged, OUTx voltage tracks SVR voltage
9		see step 5
10		OUTx is at ground potential, DIAG is released, TDA1566 is off

### 6.5.2 Engine start

The DC-output voltage of the amplifier follows the voltage on the SVR pin. On the SVR pin a capacitor is connected which is used for start-up and shutdown timing as well as for DC load detection. If the supply voltage drops during engine start below 8.6 V the SVR capacitor will be discharged and the fast mute is activated to prevent audible transients at the output.

If in I<sup>2</sup>C-bus mode the supply voltage drops below 5.5 V (see  $V_{P(POR)}$ ) the content of the I<sup>2</sup>C-bus latches cannot be guaranteed and the power-on reset will be activated: DB3[D7] = 1. All latches will be reset, the amplifier is switched off and the DIAG pin will be pulled LOW to indicate that a power-on reset has occurred. The TDA1566 will not start-up but wait for a command to start-up.

## 7. Limiting values

Table 21. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_P$	supply voltage	operating; $R_L = 4 \Omega$	-	18	V
		operating; $R_L = 2 \Omega$ or $1 \Omega$	-	16	V
		non operating	-1	+50	V
		load dump protection; during 50 ms; $t_r \geq 2.5$ ms	-	50	V
$V_{P(r)}$	reverse supply voltage	maximum 10 minutes	-	-2	V
$I_{OSM}$	non-repetitive peak output current		-	13	A

**Table 21. Limiting values ...continued**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
I <sub>ORM</sub>	repetitive peak output current		-	8	A
I <sub>BGM</sub>	peak back gate current	loss off GND or open V <sub>P</sub> application failure; supply decoupling capacitor of maximum 3 × 2200 µF/16 V and a series resistance of 70 mΩ	-	50	A
V <sub>1OHM</sub>	voltage on pin 1OHM	operating, non operating	[1] 0	24	V
V <sub>EN</sub>	voltage on pin EN	operating, non operating	[1] 0	24	V
V <sub>IN1-</sub>	voltage on pin IN1-	operating, non operating	[2] 0	13	V
V <sub>IN1+</sub>	voltage on pin IN1+	operating, non operating	[2] 0	13	V
V <sub>IN2-</sub>	voltage on pin IN2-	operating, non operating	[2] 0	13	V
V <sub>IN2+</sub>	voltage on pin IN2+	operating, non operating	[2] 0	13	V
V <sub>DIAG</sub>	voltage on pin DIAG	operating, non operating	[2] 0	13	V
V <sub>CLIP</sub>	voltage on pin CLIP	operating, non operating	[2] 0	13	V
V <sub>PROG</sub>	voltage on pin PROG	operating, non operating	[2] 0	13	V
V <sub>SVR</sub>	voltage on pin SVR	operating, non operating	[2] 0	13	V
V <sub>SCL</sub>	voltage on pin SCL	operating, non operating	[2] 0	6.5	V
V <sub>SDA</sub>	voltage on pin SDA	operating, non operating	[2] 0	6.5	V
V <sub>ADS1</sub>	voltage on pin ADS1	operating, non operating	[2] 0	6.5	V
V <sub>ADS2</sub>	voltage on pin ADS2	operating, non operating	[2] 0	6.5	V
T <sub>j</sub>	junction temperature		-	150	°C
T <sub>stg</sub>	storage temperature		-55	+150	°C
T <sub>amb</sub>	ambient temperature		-40	+85	°C
V <sub>(prot)</sub>	protection voltage	AC and DC short-circuit voltage of output pins and across the load	-	V <sub>P</sub>	V
P <sub>tot</sub>	total power dissipation	T <sub>case</sub> = 70 °C	-	80	W

**Table 21. Limiting values ...continued**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{\text{esd}}$	electrostatic discharge voltage	HBM			
		C = 100 pF; R <sub>s</sub> = 1500 $\Omega$	-	2000	V
		MM			
		C = 200 pF; R <sub>s</sub> = 10 $\Omega$ ; L = 0.75 $\mu$ H	-	200	V

[1] The voltage on this pin is clamped by an ESD protection. If this pin is connected to  $V_P$  a series resistance of 10 k $\Omega$  should be added.

[2] The voltage on this pin is clamped by an ESD protection.

## 8. Thermal characteristics

**Table 22. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
$R_{\text{th(j-c)}}$	thermal resistance from junction to case			
		TDA1566TH	1.0	K/W
		TDA1566J	1.0	K/W
$R_{\text{th(j-a)}}$	thermal resistance from junction to ambient			
		TDA1566TH in free air	35	K/W
		TDA1566J in free air	35	K/W

## 9. Characteristics

**Table 23. Characteristics**

Refer to test circuit (see [Figure 22](#));  $V_P = 14.4$  V;  $R_L = 4$   $\Omega$ ;  $-40$   $^{\circ}$ C <  $T_{\text{amb}}$  <  $+85$   $^{\circ}$ C and  $-40$   $^{\circ}$ C <  $T_j$  <  $+150$   $^{\circ}$ C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supply voltage behavior</b>						
$V_{P(\text{oper})}$	operating supply voltage	$R_L = 4$ $\Omega$	$V_{P(\text{low})(\text{mute})}$	14.4	18	V
		$R_L = 2$ $\Omega$ or 1 $\Omega$	[1] $V_{P(\text{low})(\text{mute})}$	14.4	16	V
$I_q$	quiescent current	no load	-	180	220	mA
$I_{\text{stb}}$	standby current	I <sup>2</sup> C-bus mode only	-	10	15	mA
$I_{\text{off}}$	off-state current	$V_{\text{EN}} \leq 0.4$ V; $T_j < 85$ $^{\circ}$ C	-	2	10	$\mu$ A
$V_O$	output voltage		6.7	7.2	7.6	V
$V_{P(\text{low})(\text{mute})}$	low supply voltage mute	falling supply voltage	6.5	7.2	7.7	V
		rising supply voltage	7.0	7.6	8.2	V
$V_{P(\text{POR})}$	power-on reset supply voltage		4.1	5.0	5.8	V

**Table 23. Characteristics ...continued**

Refer to test circuit (see [Figure 22](#));  $V_P = 14.4\text{ V}$ ;  $R_L = 4\ \Omega$ ;  $-40\text{ }^\circ\text{C} < T_{amb} < +85\text{ }^\circ\text{C}$  and  $-40\text{ }^\circ\text{C} < T_j < +150\text{ }^\circ\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>O(offset)</sub>	output offset voltage	amplifier mode; on	−50	0	+50	mV
		line driver mode; on	−25	0	+25	mV
		amplifier and line driver mode; mute	−25	0	+25	mV
Mode select pin EN (see <a href="#">Figure 5</a> )						
V <sub>EN</sub>	voltage on pin EN	off condition; I <sup>2</sup> C-bus and non-I <sup>2</sup> C-bus mode	-	-	1.0	V
		standby mode; I <sup>2</sup> C-bus mode	2.6	-	V <sub>P</sub>	V
		mute condition; non-I <sup>2</sup> C-bus mode	2.6	-	4.5	V
		operating condition; non-I <sup>2</sup> C-bus mode	<a href="#">[2]</a> 6.5	-	V <sub>P</sub>	V
I <sub>EN</sub>	current on pin EN	V <sub>EN</sub> = 8.5 V	<a href="#">[3]</a> -	10	70	μA
Start-up, shutdown and mute timing (see <a href="#">Figure 11</a> )						
t <sub>wake</sub>	wake-up time	time after wake-up via EN pin before first I <sup>2</sup> C-bus transmission is recognized	-	300	500	μs
t <sub>d(mute_off)</sub>	mute off delay time	I <sup>2</sup> C-bus mode with slow start enabled and non-I <sup>2</sup> C-bus mode; DC load detection disabled				
		C <sub>SVR</sub> = 22 μF	<a href="#">[4]</a> -	380	-	ms
		C <sub>SVR</sub> = 10 μF	<a href="#">[4]</a> -	170	-	ms
		I <sup>2</sup> C-bus mode only; DC load detection enabled; slow start enabled				
		C <sub>SVR</sub> = 22 μF	<a href="#">[4]</a> -	510	-	ms
		C <sub>SVR</sub> = 10 μF	<a href="#">[4]</a> -	250	-	ms
		I <sup>2</sup> C-bus mode only; DC load detection disabled; slow start disabled				
		C <sub>SVR</sub> = 22 μF	<a href="#">[4]</a> -	230	-	ms
		C <sub>SVR</sub> = 10 μF	<a href="#">[4]</a> -	110	-	ms
		I <sup>2</sup> C-bus mode only; DC load detection enabled; slow start disabled				
		C <sub>SVR</sub> = 22 μF	<a href="#">[4]</a> -	370	-	ms
		C <sub>SVR</sub> = 10 μF	<a href="#">[4]</a> -	180	-	ms
t <sub>det(DCload)</sub>	DC load detection time	I <sup>2</sup> C-bus mode only; DC load detection enabled				
		C <sub>SVR</sub> = 22 μF	<a href="#">[4]</a> -	160	-	ms
		C <sub>SVR</sub> = 10 μF	<a href="#">[4]</a> -	70	-	ms
t <sub>d(mute-fgain)</sub>	mute to full gain delay time	C <sub>SVR</sub> = 22 μF	<a href="#">[5]</a> -	90	-	ms
		C <sub>SVR</sub> = 10 μF	<a href="#">[5]</a> -	40	-	ms

**Table 23. Characteristics ...continued**

Refer to test circuit (see [Figure 22](#));  $V_P = 14.4\text{ V}$ ;  $R_L = 4\ \Omega$ ;  $-40\text{ }^\circ\text{C} < T_{amb} < +85\text{ }^\circ\text{C}$  and  $-40\text{ }^\circ\text{C} < T_j < +150\text{ }^\circ\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(\text{mute-on})}$	mute to on delay time	I <sup>2</sup> C-bus mode: IB2[D0] = 1 to 0	-	20	40	ms
		non-I <sup>2</sup> C-bus mode: $V_{EN}$ from 3.3 V to 8 V	-	20	40	ms
$t_{d(\text{slow\_mute})}$	slow mute delay time	I <sup>2</sup> C-bus mode: IB2[D0] = 0 to 1; IB2[D2] = 0	-	20	40	ms
		non-I <sup>2</sup> C-bus mode: $V_{EN}$ from 8 V to 3.3 V	-	20	40	ms
$t_{d(\text{fast\_mute})}$	fast mute delay time	on to mute in I <sup>2</sup> C-bus mode; IB2[D2] = 1; IB2[D0] = 0 to 1	-	0.1	1	ms
		on to standby in I <sup>2</sup> C-bus mode; IB2[D0] = 0; IB1[D0] = 1 to 0	-	20	40	ms
		on to off in I <sup>2</sup> C-bus and non-I <sup>2</sup> C-bus mode: $V_{EN}$ from 8 V to 0.5 V	-	0.1	1	ms
$t_{(\text{on-SVR})}$	time from amplifier switch-on to SVR above $V_P / 2$	via I <sup>2</sup> C-bus (IB1[D0]) to DB3[D4] = 1 (SVR above $V_P / 2$ ); I <sup>2</sup> C-bus mode with slow start enabled; DC load detection disabled				
		$C_{SVR} = 22\ \mu\text{F}$	-	1000	-	ms
		$C_{SVR} = 10\ \mu\text{F}$	-	440	-	ms
		I <sup>2</sup> C-bus mode only; DC load detection enabled; slow start enabled.				
		$C_{SVR} = 22\ \mu\text{F}$	-	1100	-	ms
		$C_{SVR} = 10\ \mu\text{F}$	-	530	-	ms
		I <sup>2</sup> C-bus mode only; DC load detection disabled; slow start disabled				
		$C_{SVR} = 22\ \mu\text{F}$	-	810	-	ms
		$C_{SVR} = 10\ \mu\text{F}$	-	370	-	ms
		I <sup>2</sup> C-bus mode only; DC load detection enabled; slow start disabled				
		$C_{SVR} = 22\ \mu\text{F}$	-	940	-	ms
		$C_{SVR} = 10\ \mu\text{F}$	-	450	-	ms

**I<sup>2</sup>C-bus interface and 1  $\Omega$  selection<sup>[6]</sup>**

$V_{IL(\text{SCL})}$	LOW-level input voltage on pin SCL	-	-	1.5	V
$V_{IL(\text{SDA})}$	LOW-level input voltage on pin SDA	-	-	1.5	V
$V_{IH(\text{SCL})}$	HIGH-level input voltage on pin SCL	2.3	-	5.5	V

**Table 23. Characteristics ...continued**

Refer to test circuit (see [Figure 22](#));  $V_P = 14.4\text{ V}$ ;  $R_L = 4\ \Omega$ ;  $-40\text{ }^\circ\text{C} < T_{amb} < +85\text{ }^\circ\text{C}$  and  $-40\text{ }^\circ\text{C} < T_j < +150\text{ }^\circ\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>IH(SDA)</sub>	HIGH-level input voltage on pin SDA		2.3	-	5.5	V
V <sub>OL(SDA)</sub>	LOW-level output voltage on pin SDA	I <sub>load</sub> = 5 mA	-	-	0.4	V
f <sub>clk</sub>	clock frequency		-	400	-	kHz
V <sub>1OHM</sub>	voltage on pin 1OHM	mono channel mode	<a href="#">[7]</a> 2.5	-	V <sub>P</sub>	V
		dual channel mode	0	-	1.5	V
I <sub>1OHM</sub>	current on pin 1OHM	V <sub>1OHM</sub> = 1.5 V	-	130	200	μA
		V <sub>1OHM</sub> = 5.5 V	-	-	5	μA
I <sub>SCL</sub>	current on pin SCL	V <sub>SCL</sub> = 1.5 V	-	-	5	μA
		V <sub>SCL</sub> = 5.5 V	-	-	5	μA
I <sub>SDA</sub>	current on pin SDA	V <sub>SDA</sub> = 1.5 V	-	-	5	μA
		V <sub>SDA</sub> = 5.5 V	-	-	5	μA
I <sub>ADS1</sub>	current on pin ADS1	ADS1 pin connected to GND	-	300	400	μA
		ADS1 pin connected via 33 kΩ to GND	-	70	100	μA
I <sub>ADS2</sub>	current on pin ADS2	ADS2 pin connected to GND	-	300	400	μA
		ADS2 pin connected via 33 kΩ to GND	-	70	100	μA
Diagnostic						
V <sub>OL(DIAG)</sub>	LOW-level output voltage on pin DIAG	fault condition; I <sub>DIAG</sub> = 1 mA	-	-	0.3	V
V <sub>OL(CLIP)</sub>	LOW-level output voltage on pin CLIP	TH version only; clip or temperature pre-warning active; I <sub>CLIP</sub> = 1 mA	-	-	0.3	V
I <sub>LIH(CLIP)</sub>	HIGH-level input leakage current on pin CLIP	diagnostic, clip or temperature pre-warning not activated	-	-	2	μA
I <sub>LIH(DIAG)</sub>	HIGH-level input leakage current on pin DIAG	diagnostic, clip or temperature pre-warning not activated	-	-	2	μA
V <sub>th(offset)</sub>	threshold voltage for offset detection		1.0	1.5	2.0	V
THD <sub>CLIP7</sub>	7 % clip detection level (THD)	I <sup>2</sup> C-bus mode: IB2[D7] = 1	<a href="#">[8]</a> -	7	-	%
THD <sub>CLIP3</sub>	3 % clip detection level (THD)	I <sup>2</sup> C-bus mode: IB2[D7] = 0 and non-I <sup>2</sup> C-bus mode	<a href="#">[8]</a> -	3	-	%
T <sub>j(AV)(warn1)</sub>	average junction temperature for pre-warning 1	I <sup>2</sup> C-bus mode: IB3[D4] = 0 and non-I <sup>2</sup> C-bus mode	-	145	-	°C
T <sub>j(AV)(warn2)</sub>	average junction temperature for pre-warning 2	I <sup>2</sup> C-bus mode: IB3[D4] = 1	-	122	-	°C



**Table 23. Characteristics ...continued**

Refer to test circuit (see [Figure 22](#));  $V_P = 14.4\text{ V}$ ;  $R_L = 4\ \Omega$ ;  $-40\text{ }^\circ\text{C} < T_{amb} < +85\text{ }^\circ\text{C}$  and  $-40\text{ }^\circ\text{C} < T_j < +150\text{ }^\circ\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{j(AV)(G(-0.5dB))}$	average junction temperature for 0.5 dB gain reduction	$V_i = 0.05\text{ V}$	-	155	-	$^\circ\text{C}$
$\Delta T_{j(warn1-mute)}$	difference in junction temperature between pre-warning 1 and mute		-	10	-	$^\circ\text{C}$
$\Delta T_{j(G(-0.5-40dB))}$	difference in junction temperature between 0.5 dB and 40 dB gain reduction		-	20	-	$^\circ\text{C}$
$T_{j(AV)(off)}$	average junction temperature for off		-	175	185	$^\circ\text{C}$
$Z_{th(load)}$	load detection threshold impedance	amplifier DC load detection; I <sup>2</sup> C-bus mode only: $R_{PROG} = 1500\ \Omega/1\ \%$	-	-	25	$\Omega$
		line driver DC load detection; I <sup>2</sup> C-bus mode only: $R_{PROG} = 1500\ \Omega/1\ \%$	120	-	500	$\Omega$
		open load DC load detection; I <sup>2</sup> C-bus mode only: $R_{PROG} = 1500\ \Omega/1\ \%$	<a href="#">[9]</a> 5	-	-	$\text{k}\Omega$
$I_{oM}$	peak output current	AC load bit is set; I <sup>2</sup> C-bus mode only: $R_{PROG} = 1500\ \Omega/1\ \%$ ; $T_j > 0\text{ }^\circ\text{C}$	320	-	-	mA
		AC load bit is not set; I <sup>2</sup> C-bus mode only: $R_{PROG} = 1500\ \Omega/1\ \%$ ; $T_j > 0\text{ }^\circ\text{C}$	-	-	200	mA

**Table 23. Characteristics ...continued**

Refer to test circuit (see [Figure 22](#));  $V_P = 14.4\text{ V}$ ;  $R_L = 4\ \Omega$ ;  $-40\text{ }^\circ\text{C} < T_{amb} < +85\text{ }^\circ\text{C}$  and  $-40\text{ }^\circ\text{C} < T_j < +150\text{ }^\circ\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Amplifier</b>						
$P_o$	output power	$R_L = 4\ \Omega$ ; $V_P = 14.4\text{ V}$ ; THD = 0.5 %	-	23	-	W
		$R_L = 4\ \Omega$ ; $V_P = 14.4\text{ V}$ ; THD = 3 %	-	24	-	W
		$R_L = 4\ \Omega$ ; $V_P = 14.4\text{ V}$ ; THD = 10 %	24	29	-	W
		$R_L = 4\ \Omega$ ; $V_P = 14.4\text{ V}$ maximum power; $V_i = 2\text{ V}$ (RMS) square wave	40	45	-	W
		$R_L = 4\ \Omega$ ; $V_P = 15.2\text{ V}$ maximum power; $V_i = 2\text{ V}$ (RMS) square wave	45	50	-	W
		$R_L = 2\ \Omega$ ; $V_P = 14.4\text{ V}$ ; THD = 0.5 %	-	38	-	W
		$R_L = 2\ \Omega$ ; $V_P = 14.4\text{ V}$ ; THD = 3 %	-	41	-	W
		$R_L = 2\ \Omega$ ; $V_P = 14.4\text{ V}$ ; THD = 10 %	39	50	-	W
		$R_L = 2\ \Omega$ ; $V_P = 14.4\text{ V}$ maximum power; $V_i = 2\text{ V}$ (RMS) square wave	67	75	-	W
		$R_L = 1\ \Omega$ ; $V_P = 14.4\text{ V}$ ; THD = 0.5 %	-	74	-	W
		$R_L = 1\ \Omega$ ; $V_P = 14.4\text{ V}$ ; THD = 3 %	-	81	-	W
		$R_L = 1\ \Omega$ ; $V_P = 14.4\text{ V}$ ; THD = 10 %	78	92	-	W
		$R_L = 1\ \Omega$ ; $V_P = 14.4\text{ V}$ maximum power; $V_i = 2\text{ V}$ (RMS) square wave	130	150	-	W
THD	total harmonic distortion	$P_o = 1\text{ W to }12\text{ W}$ ; $f = 1\text{ kHz}$ ; $R_L = 4\ \Omega$	-	0.005	0.1	%
		$P_o = 1\text{ W to }12\text{ W}$ ; $f = 1\text{ kHz}$ ; $R_L = 2\ \Omega$	-	0.01	0.2	%
		$P_o = 1\text{ W to }12\text{ W}$ ; $f = 1\text{ kHz}$ ; $R_L = 1\ \Omega$	-	0.02		%
		$P_o = 1\text{ W to }12\text{ W}$ ; $f = 10\text{ kHz}$ ; measured with 30 kHz filter; $R_L = 4\ \Omega$	-	0.1	0.3	%
		$P_o = 1\text{ W to }12\text{ W}$ ; $f = 10\text{ kHz}$ ; measured with 30 kHz filter; $R_L = 2\ \Omega$	-	0.2	0.6	%
		line driver mode; $V_o = 1\text{ V}$ (RMS) and $5\text{ V}$ (RMS); $f = 20\text{ Hz to }20\text{ kHz}$ ; $R_L = 400\ \Omega$	-	0.02	0.1	%

**Table 23. Characteristics ...continued**

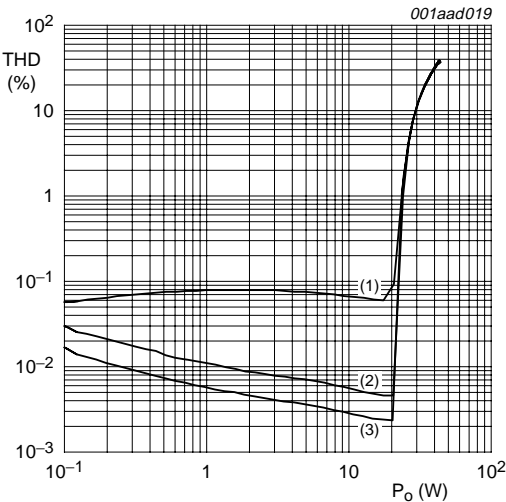
Refer to test circuit (see [Figure 22](#));  $V_P = 14.4\text{ V}$ ;  $R_L = 4\text{ }\Omega$ ;  $-40\text{ }^\circ\text{C} < T_{amb} < +85\text{ }^\circ\text{C}$  and  $-40\text{ }^\circ\text{C} < T_j < +150\text{ }^\circ\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\alpha_{CS}$	channel separation	$f = 1\text{ kHz to } 10\text{ kHz}$ ; $R_S = 2\text{ k}\Omega$	42	55	-	dB
SVRR	supply voltage rejection ratio	$f = 100\text{ Hz to } 10\text{ kHz}$ ; $R_S = 2\text{ k}\Omega$ ; $V_{ripple} = 2\text{ V (p-p)}$	45	70	-	dB
CMRR	common-mode rejection ratio	amplifier mode; $V_{cm} = 0.3\text{ V (p-p)}$ ; $f = 1\text{ kHz to } 3\text{ kHz}$ ; $R_S = 2\text{ k}\Omega$	60	70	-	dB
$V_{cm(max)(rms)}$	maximum common-mode voltage (RMS value)	$f = 1\text{ kHz}$ ; $V_i = 0.5\text{ V (RMS)}$ ; amplifier mode	-	-	1	V
		$f = 1\text{ kHz}$ ; $V_i = 1.6\text{ V (RMS)}$ ; line driver mode	-	-	0.6	V
$V_{n(o)(RMS)}$	RMS noise output voltage	line driver mode; filter 20 Hz to 22 kHz; $R_S = 2\text{ k}\Omega$	-	20	50	$\mu\text{V}$
		amplifier mode; filter 20 Hz to 22 kHz; $R_S = 2\text{ k}\Omega$	-	50	70	$\mu\text{V}$
		mute mode; filter 20 Hz to 22 kHz; $R_S = 2\text{ k}\Omega$	-	20	50	$\mu\text{V}$
$G_{v(amp)}$	voltage gain amplifier mode	$(V_{OUT1+} - V_{OUT1-}) / (V_{IN1+} - V_{IN1-})$	25	26	27	dB
$G_{v(ld)}$	voltage gain line driver mode	$(V_{OUT1+} - V_{OUT1-}) / (V_{IN1+} - V_{IN1-})$	15	16	17	dB
$Z_{i(sym)}$	symmetrical input impedance	$C = 470\text{ nF}$ <a href="#">[10]</a>	44	60	-	k $\Omega$
$\alpha_{mute}$	mute attenuation	$f = 1\text{ kHz}$ ; $V_i = 1\text{ V (RMS)}$	-	80	-	dB
$B_p$	power bandwidth	-1 dB; $C = 2.2\text{ }\mu\text{F}$ <a href="#">[11]</a>	-	20 to 20000	-	Hz

- [1] Operation above 16 V with a 2  $\Omega$  or 1  $\Omega$  mode with reactive load can trigger the amplifier protection. The amplifier switches off and will restart after 8 ms resulting in an 'audio hole'.
- [2] If the EN pin is connected with  $V_P$  a series resistance of 10 k $\Omega$  is necessary for load dump robustness.
- [3] If the EN pin is left unconnected the amplifier will be switched off.
- [4] The mute release is initiated when the SVR voltage increases above 3.5 V typical. Mute release is defined as the moment when the output signal has reached 10 % of the expected amplitude.
- [5] Mute release is defined as the moment when the output signal has reached 10 % of the expected amplitude ( $G_v \times V_i$ ). Full gain is defined as the moment when the output signal has reached 90 % of the expected amplitude ( $G_v \times V_i$ ).
- [6] Standard I<sup>2</sup>C-bus spec: maximum LOW level =  $0.3 \times V_{DD}$ , minimum HIGH level =  $0.7 \times V_{DD}$ . To comply with 5 V and 3.3 V logic the maximum LOW level is defined with  $V_{DD} = 5\text{ V}$  and the minimum HIGH level with  $V_{DD} = 3.3\text{ V}$ .
- [7] If the 1  $\Omega$  pin is connected with  $V_P$  a series resistance of 10 k $\Omega$  is necessary for load dump robustness.
- [8] Clip detect is not operational for  $V_P < 10\text{ V}$ .
- [9] If an open load is detected the amplifier is switched in line driver mode.
- [10]  $R_S$  is the total differential source resistance. -3 dB cut-off frequency is given as
- $$\frac{1}{2\pi \times R_i \times C_i} = \frac{1}{2\pi \times 22\text{ k}\Omega \times 470\text{ nF} \times 0.8} = 19\text{ Hz}$$
- assuming worst case low input resistance and 20 % spread in  $C_i$ .
- [11] Power bandwidth can be limited by the -3 dB cut-off frequency, see [Table note 10](#).

9.1 Performance diagrams

All graphs  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .



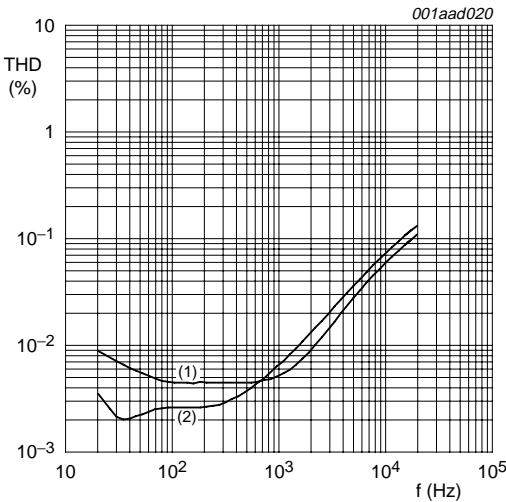
$R_L = 4\text{ }\Omega$ ; 80 kHz measurement filter.

(1)  $f = 10\text{ kHz}$ .

(2)  $f = 1\text{ kHz}$ .

(3)  $f = 100\text{ Hz}$ .

Fig 12. THD as a function of output power

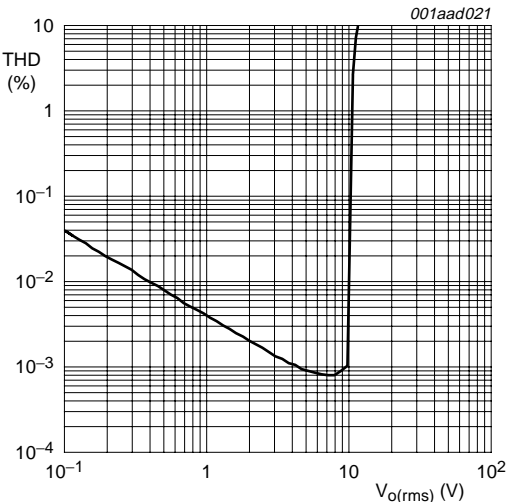


$R_L = 4\text{ }\Omega$ ; 80 kHz measurement filter.

(1)  $P_o = 1\text{ W}$ .

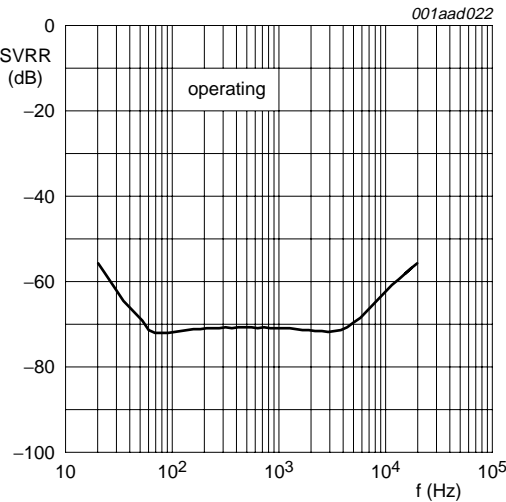
(2)  $P_o = 10\text{ W}$ .

Fig 13. THD as a function of frequency



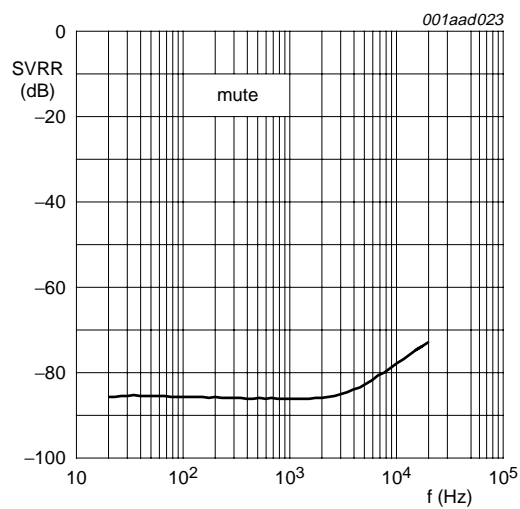
$R_L = 100\text{ }\Omega$ ; 80 kHz measurement filter;  $f = 1\text{ kHz}$ .

Fig 14. THD as a function of output voltage in line driver mode



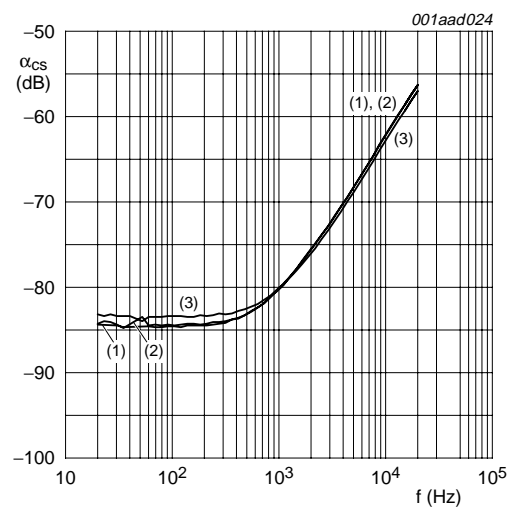
$R_s = 1\text{ k}\Omega$ ;  $C_{SVR} = 10\text{ }\mu\text{F}$ .

Fig 15. SVRR as a function of frequency (operating)



$R_s = 1\text{ k}\Omega$ ;  $C_{SVR} = 10\text{ }\mu\text{F}$ .

Fig 16. SVRR as a function of frequency (mute)



- (1)  $R_s = 0\text{ }\Omega$ .
- (2)  $R_s = 1\text{ k}\Omega$ .
- (3)  $R_s = 10\text{ k}\Omega$ .

Fig 17. Channel separation as a function of frequency

9.2 PCB layout

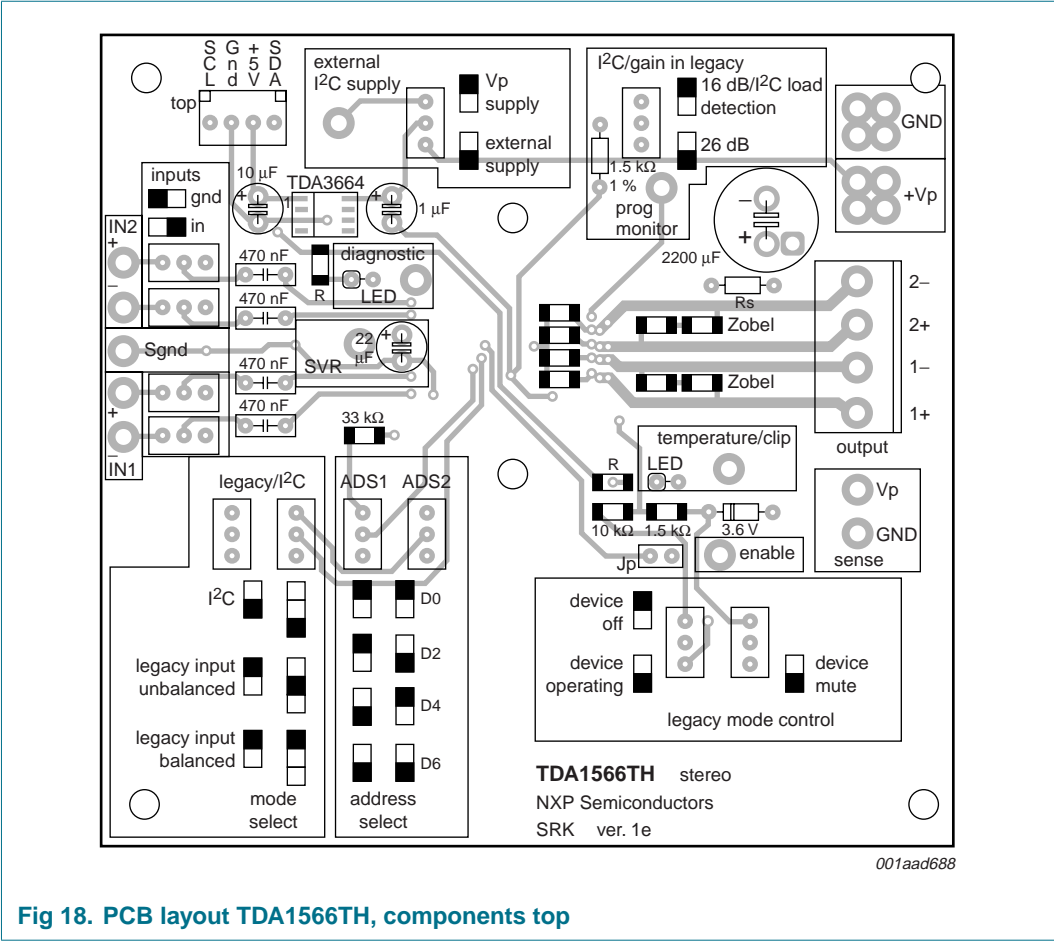
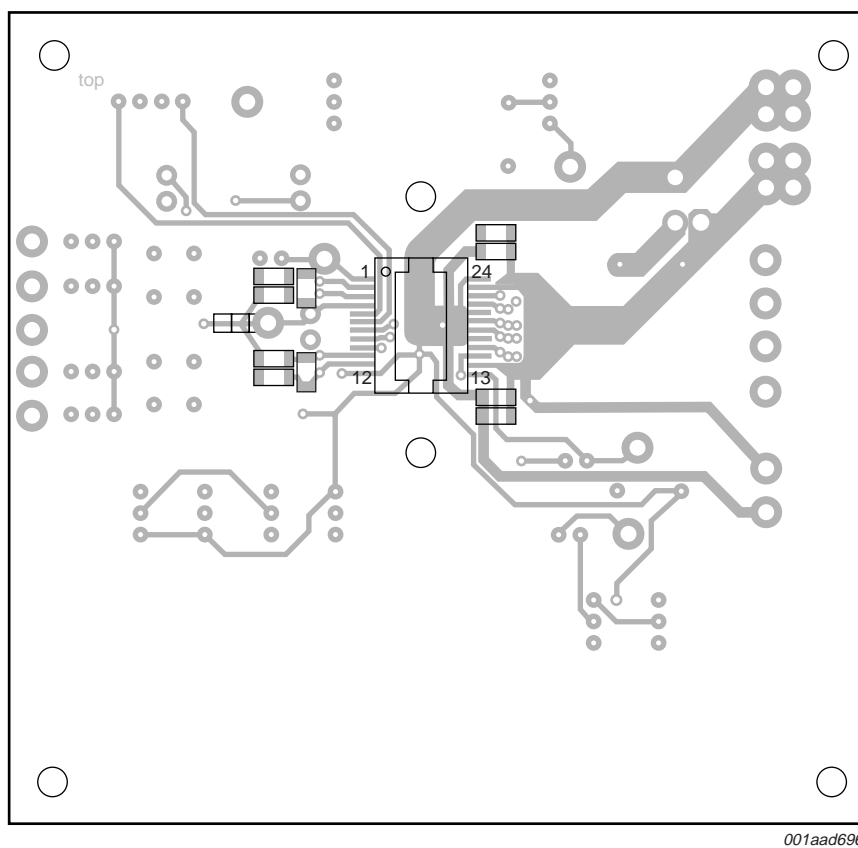


Fig 18. PCB layout TDA1566TH, components top



**Fig 19. PCB layout TDA1566TH, components bottom**

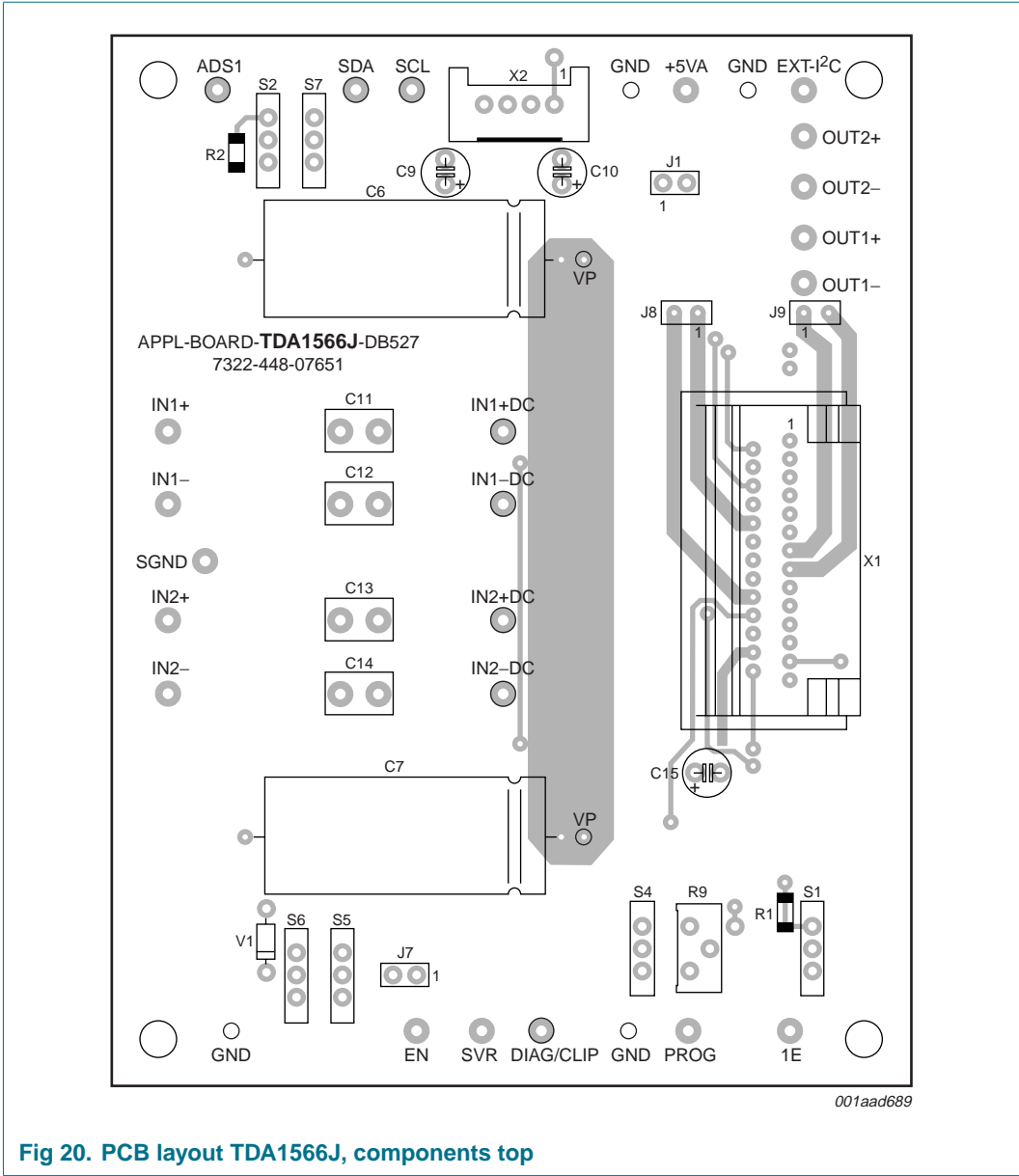
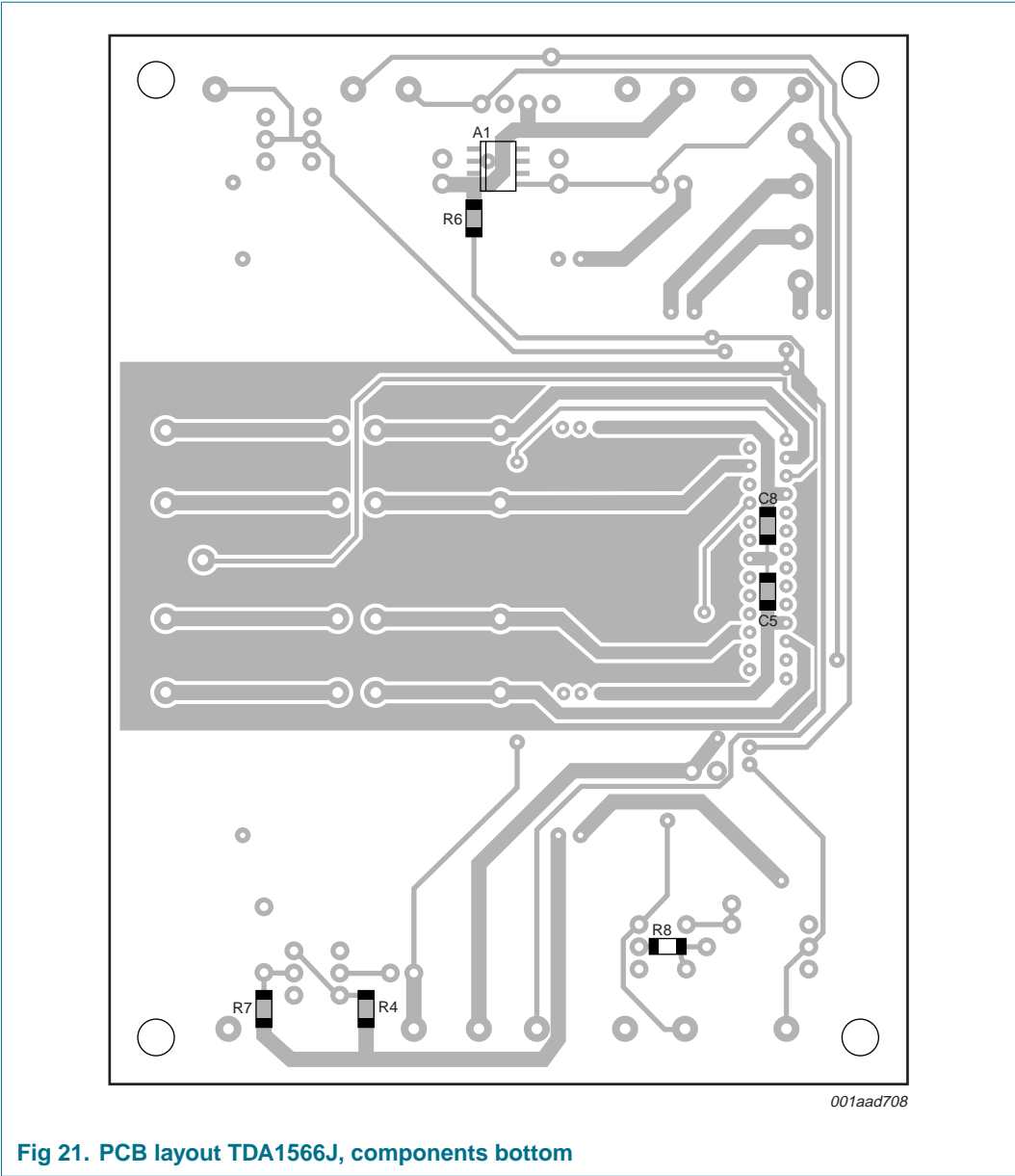
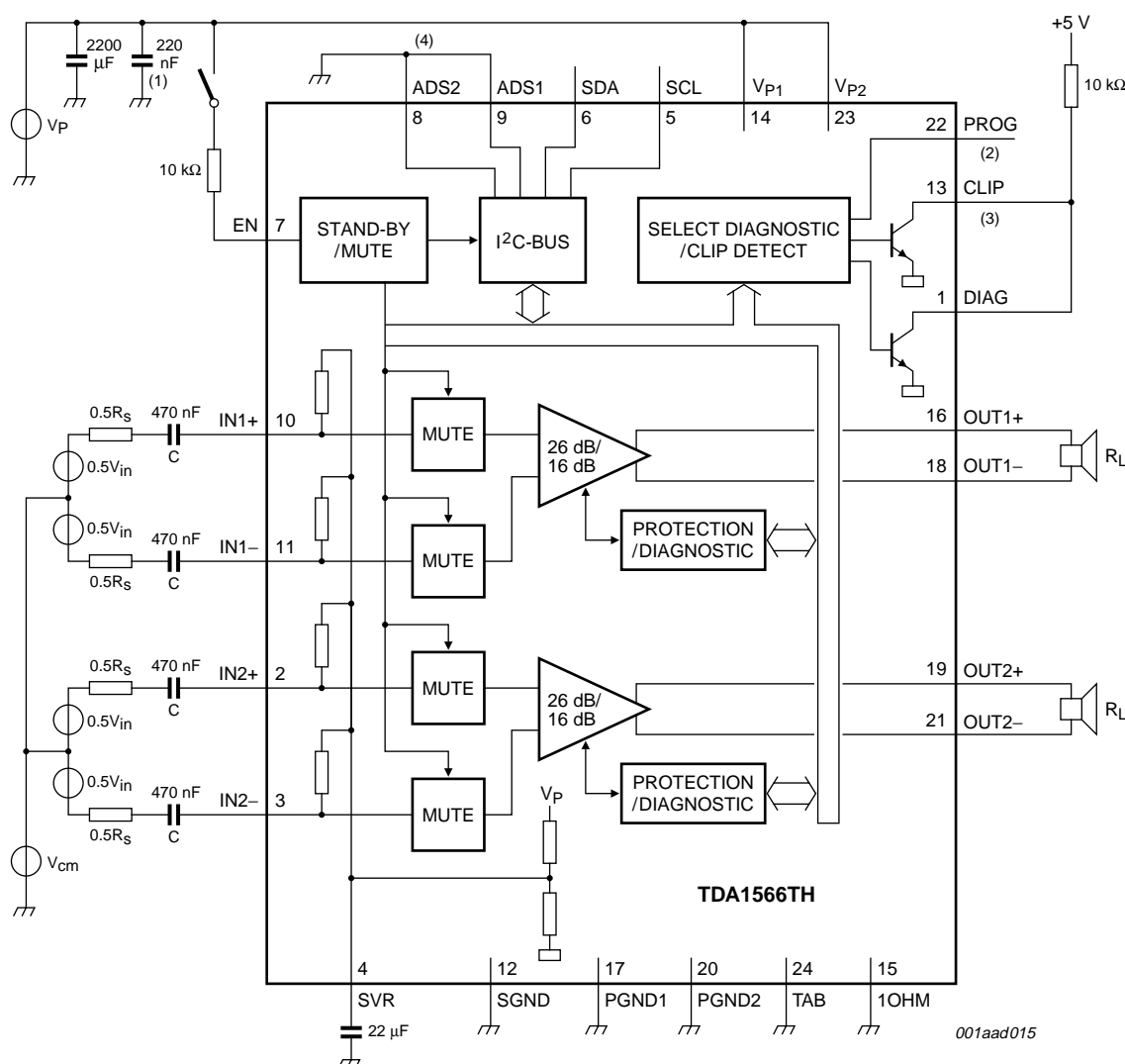


Fig 20. PCB layout TDA1566J, components top



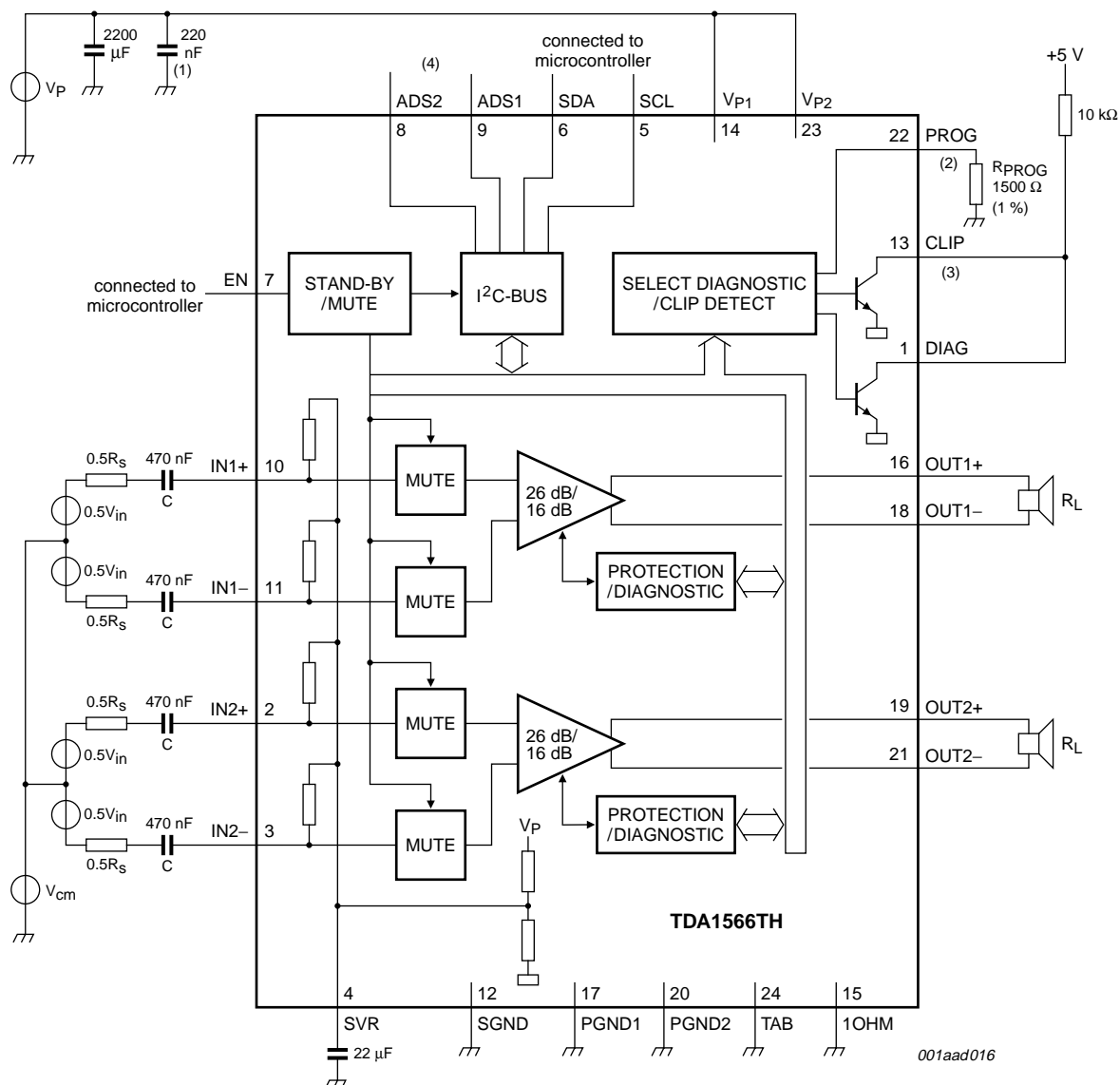


## 10. Test information



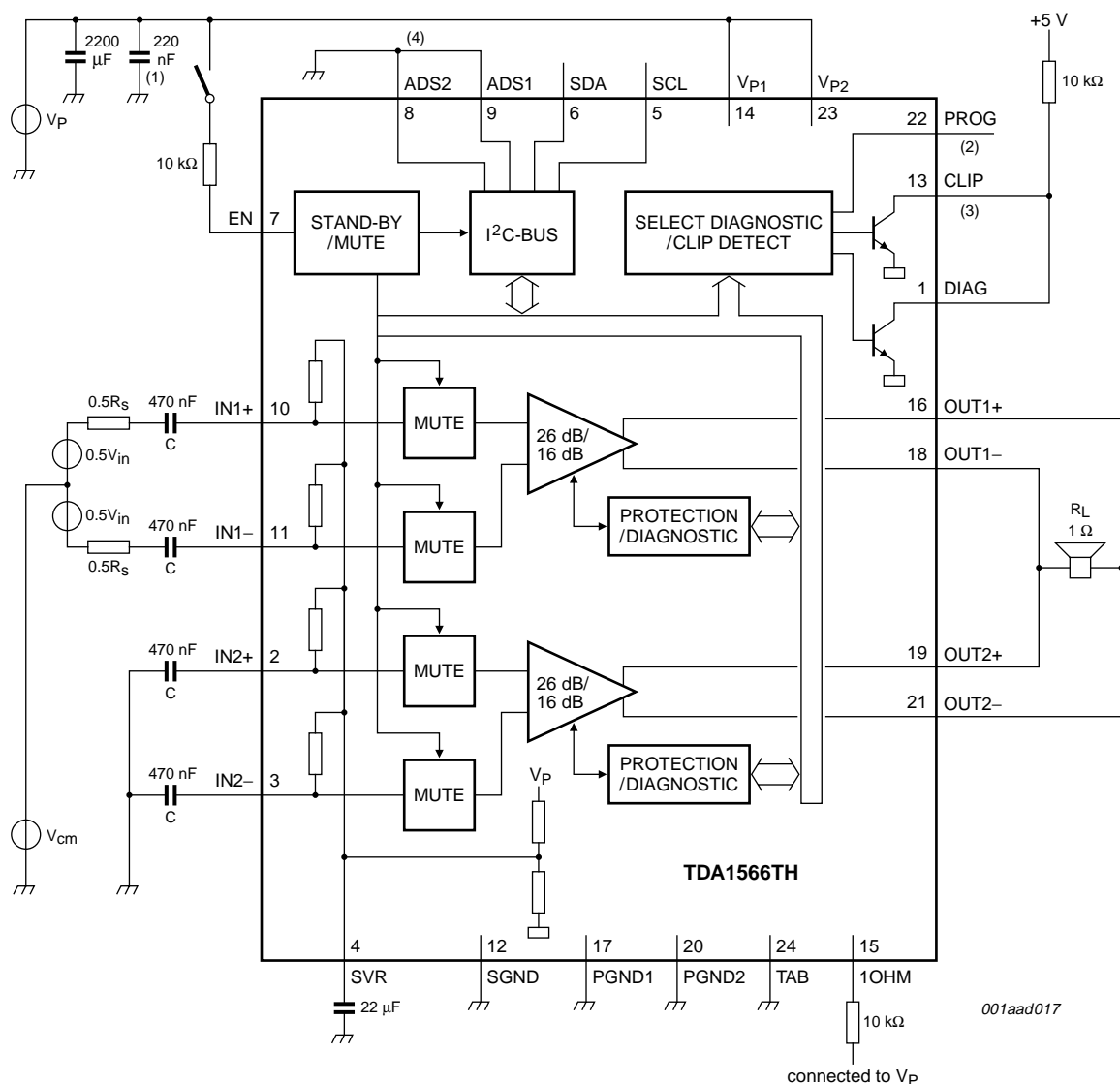
- (1) The 220 nF capacitor should be placed close to the V<sub>P</sub> and PGND pins of the IC.
- (2) In non-I<sup>2</sup>C-bus mode the PROG pin should be left unconnected for 26 dB gain selection or connected via a resistor of 1500 Ω to GND for 16 dB gain selection.
- (3) CLIP is not available in the DBS27P version.
- (4) In non-I<sup>2</sup>C-bus mode (ADS1 pin connected to GND) and balanced input source (ADS2 pin connected to GND) selected. ADS2 is not available in DBS27P version.

Fig 22. Non-I<sup>2</sup>C-bus mode (26 dB gain)



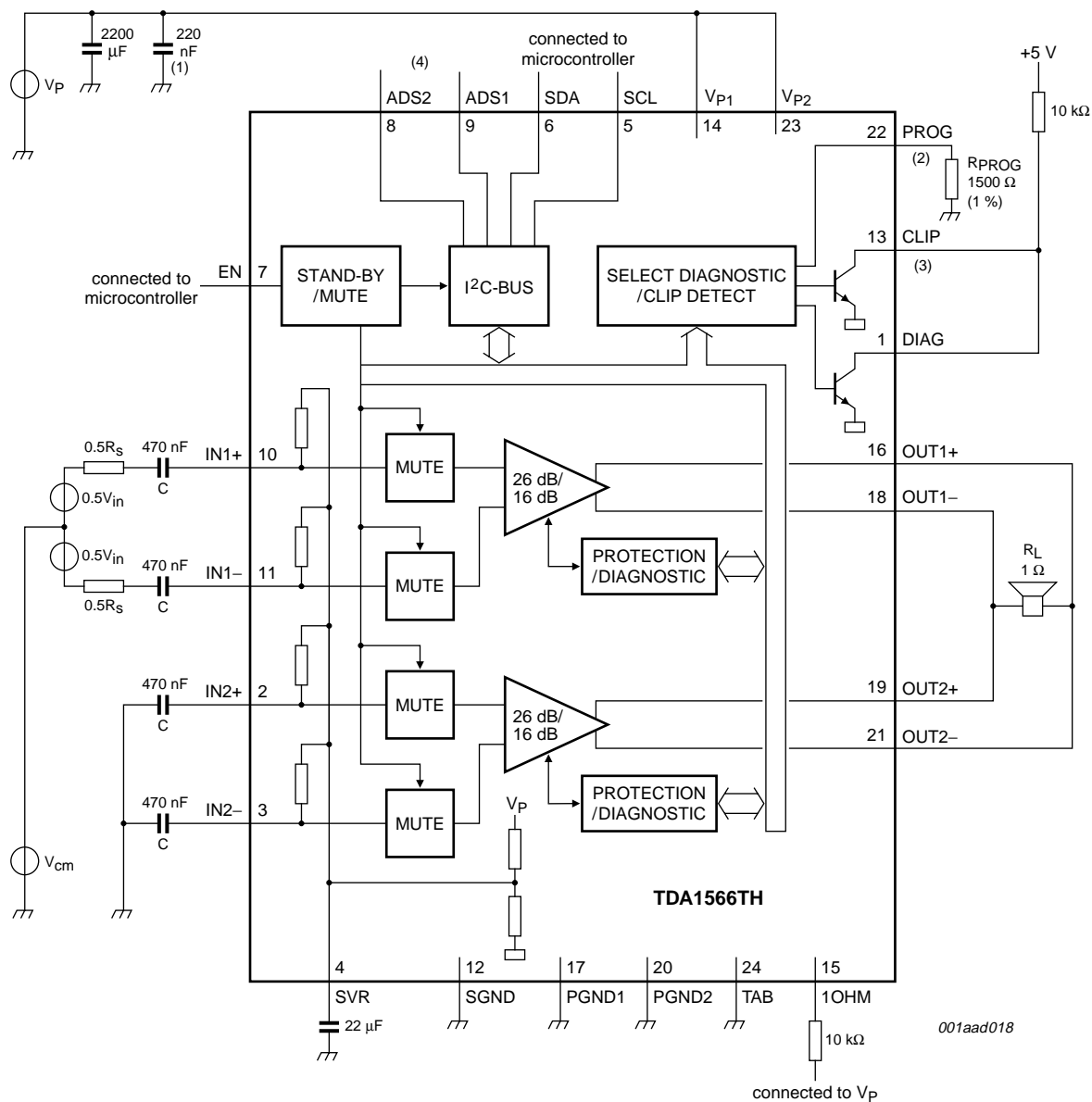
- (1) The 220 nF capacitor should be placed close to the V<sub>P</sub> and PGND pins of the IC.
- (2) R<sub>PROG</sub> defines the trip levels for the AC and DC load detection.
- (3) CLIP is not available in DBS27P version.
- (4) I<sup>2</sup>C-bus mode is selected with ADS1 open. ADS2 is not available in DBS27P version.

**Fig 23. I<sup>2</sup>C-bus mode**



- (1) The 220 nF capacitor should be placed close to the  $V_P$  and PGND pins of the IC.
- (2) In non-I<sup>2</sup>C-bus mode the PROG pin should be left unconnected for 26 dB gain selection or connected via a resistor of 1500  $\Omega$  to GND for 16 dB gain selection.
- (3) CLIP is not available in the DBS27P version.
- (4) In non-I<sup>2</sup>C-bus mode (ADS1 pin connected to GND) and balanced input source (ADS2 pin connected to GND) selected. ADS2 is not available in DBS27P version.

**Fig 24. Non-I<sup>2</sup>C-bus mode (1  $\Omega$  mode and 26 dB gain)**



- (1) The 220 nF capacitor should be placed close to the V<sub>p</sub> and PGND pins of the IC.
- (2) R<sub>prog</sub> defines the trip levels for the AC and DC load detection.
- (3) CLIP is not available in the DBS27P version.
- (4) I<sup>2</sup>C-bus mode is selected with ADS1 open. ADS2 is not available in DBS27P version.

Fig 25. I<sup>2</sup>C-bus mode (1 Ω mode)

11. Package outline

HSOP24: plastic, heatsink small outline package; 24 leads; low stand-off heightSOT566-3

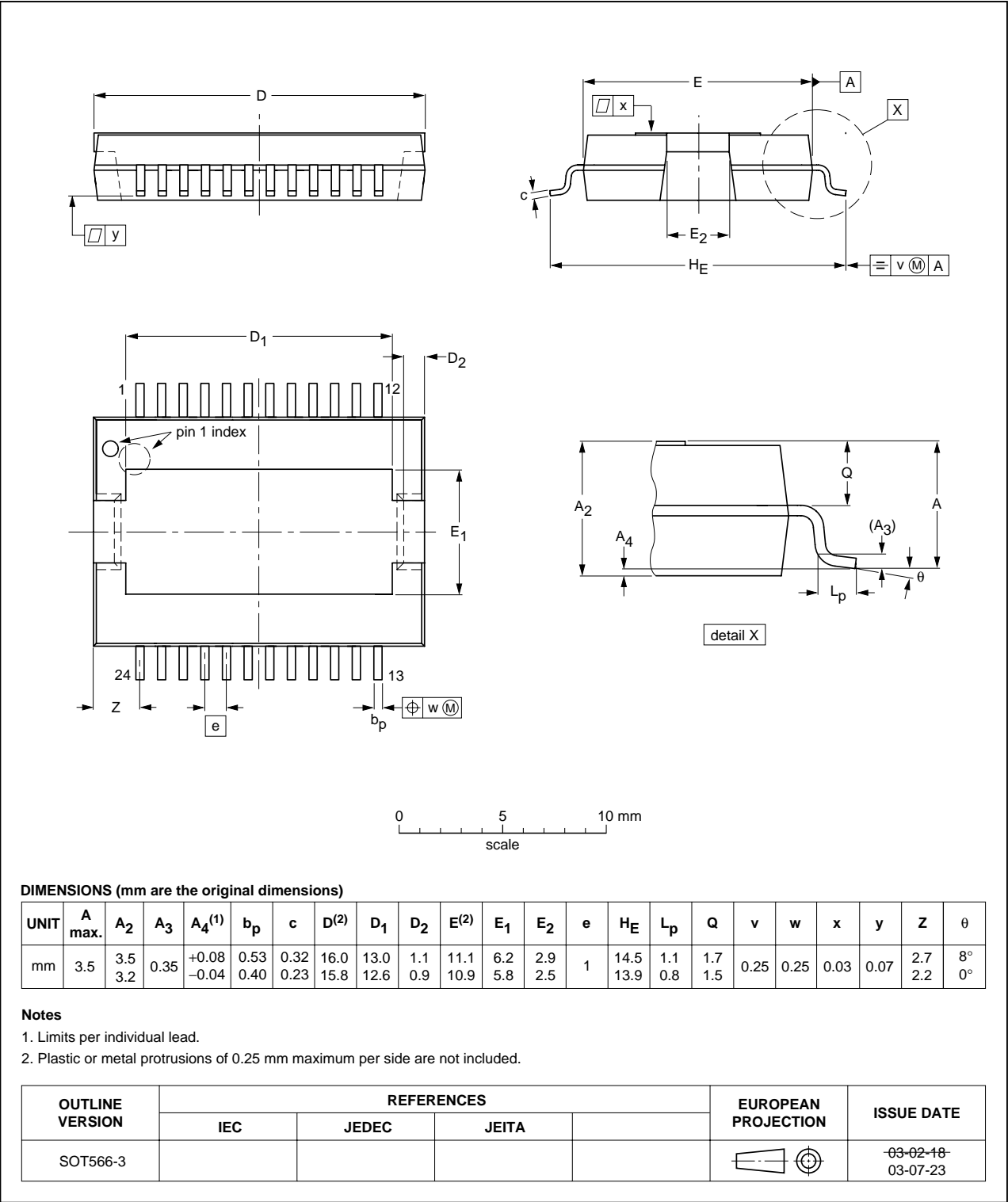


Fig 26. Package outline SOT566-3 (HSOP24)

DBS27P: plastic DIL-bent-SIL (special bent) power package; 27 leads (lead length 6.8 mm)

SOT827-1

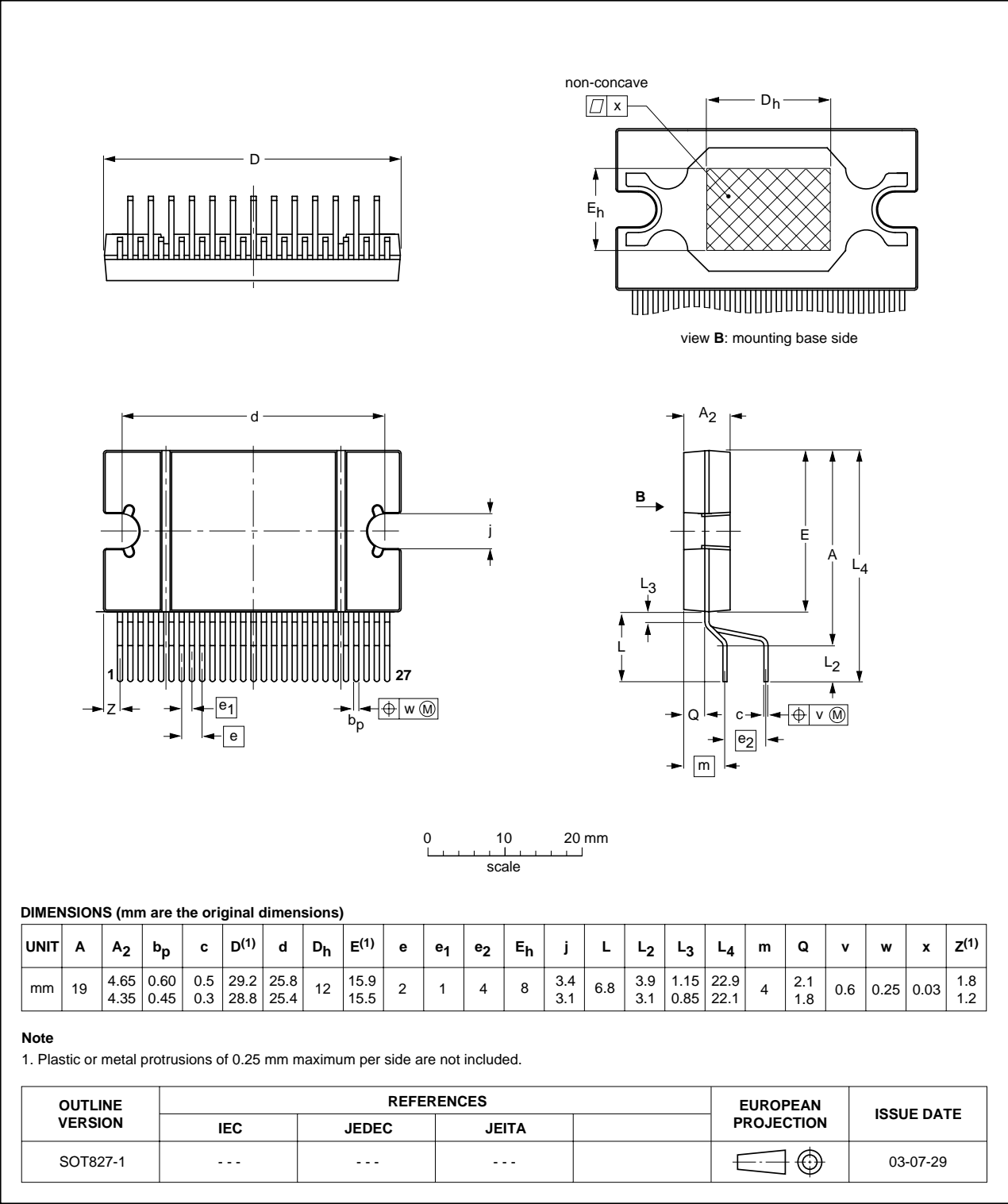


Fig 27. Package outline SOT827-1 (DBS27P)

## 12. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling integrated circuits.

## 13. Soldering

### 13.1 Introduction

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

### 13.2 Through-hole mount packages

#### 13.2.1 Soldering by dipping or by solder wave

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg(max)}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

#### 13.2.2 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 °C and 400 °C, contact may be up to 5 seconds.

### 13.3 Surface mount packages

#### 13.3.1 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 28](#)) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the



packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 24](#) and [25](#)

Table 24. SnPb eutectic process (from J-STD-020C)

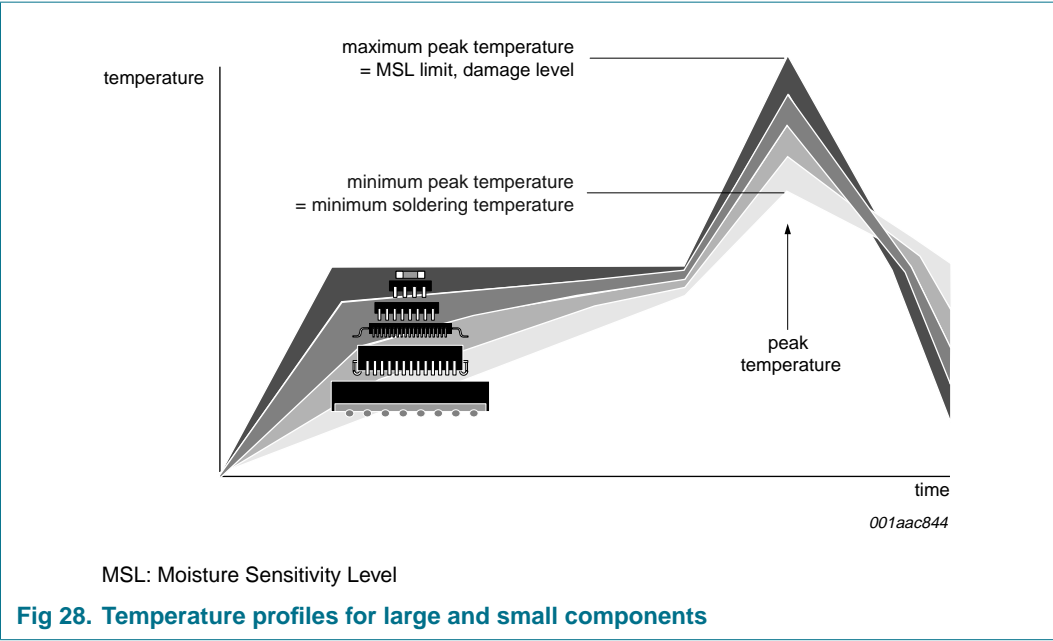
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 25. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 28](#).



For further information on temperature profiles, refer to Application Note *AN10365* “Surface mount reflow soldering description”.

### 13.3.2 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### 13.3.3 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

## 13.4 Package related soldering information

**Table 26. Suitability of IC packages for wave, reflow and dipping soldering methods**

Mounting	Package <sup>[1]</sup>	Soldering method		
		Wave	Reflow <sup>[2]</sup>	Dipping
Through-hole mount	CPGA, HCPGA	suitable	–	–
	DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable <sup>[3]</sup>	–	suitable
Through-hole-surface mount	PMFP <sup>[4]</sup>	not suitable	not suitable	–

Table 26. Suitability of IC packages for wave, reflow and dipping soldering methods ...continued

Mounting	Package <sup>[1]</sup>	Soldering method		
		Wave	Reflow <sup>[2]</sup>	Dipping
Surface mount	BGA, HTSSON..T <sup>[5]</sup> , LBGA, LFBGA, SQFP, SSOP..T <sup>[5]</sup> , TFBGA, VFBGA, XSON	not suitable	suitable	—
	DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable <sup>[6]</sup>	suitable	—
	PLCC <sup>[7]</sup> , SO, SOJ	suitable	suitable	—
	LQFP, QFP, TQFP	not recommended <sup>[7][8]</sup>	suitable	—
	SSOP, TSSOP, VSO, VSSOP	not recommended <sup>[9]</sup>	suitable	—
	CWQCCN..L <sup>[10]</sup> , WQCCN..L <sup>[10]</sup>	not suitable	not suitable	—

- [1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your NXP Semiconductors sales office.
- [2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect).
- [3] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
- [4] Hot bar soldering or manual soldering is suitable for PMFP packages.
- [5] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding  $217\text{ °C} \pm 10\text{ °C}$  measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
- [6] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- [7] If wave soldering is considered, then the package must be placed at a  $45^\circ$  angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- [8] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- [9] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
- [10] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

## 14. Revision history

Table 27. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA1566_2	20070820	Product data sheet	-	TDA1566_1
Modifications:	<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• <a href="#">Table 23 “Characteristics”</a> changed values for CMRR, P<sub>o</sub> and THD</li></ul>			
TDA1566_1 (9397 750 15043)	20060405	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 15.2 Definitions

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