19-3040; Rev 2; 5/07

Low-Input-Voltage, 300mA LDO Regulators with RESET in SOT and TDFN

General Description

The MAX1963/MAX1976 low-dropout linear regulators operate from a +1.62V to +3.6V supply and deliver a guaranteed 300mA continuous load current with a low 100mV dropout. The high-accuracy (±0.5%) output voltage is preset to an internally trimmed voltage in the +0.75V to +3.0V range. An active-low, open-drain reset output remains asserted for at least 2.2ms (MAX1963) or 70ms (MAX1976) after the output voltage reaches regulation. These devices are offered in 6-pin thin SOT23 and 6-pin 3mm x 3mm thin DFN packages.

An internal PMOS pass transistor allows the low supply current to remain independent of load and dropout voltage, making these devices ideal for portable battery-powered equipment such as personal digital assistants (PDAs), cell phones, cordless phones, and notebook computers. Other features include logic-controlled shutdown, short-circuit protection, and thermal-overload protection.

Applications

Notebook Computers

Cellular and PCS Telephones

Personal Digital Assistants (PDAs)

Hand-Held Computers

Digital Cameras

PCMCIA Cards

CD and MP3 Players

Features

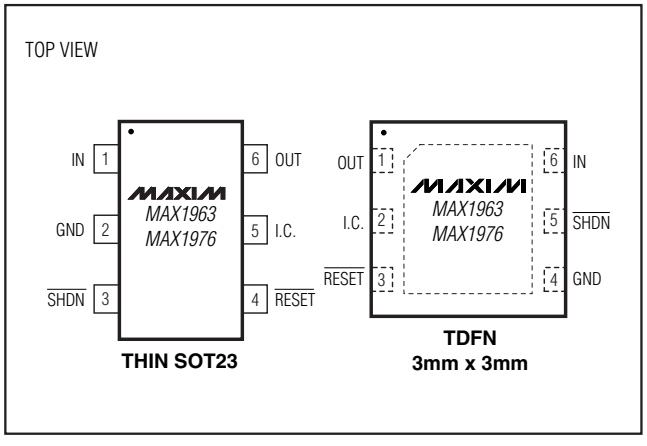
- **Low 1.62V Minimum Input Voltage**
- **Guaranteed 300mA Output Current**
- **±2.5% Accuracy Over Load/Line/Temp**
- **Low 100mV Dropout at 300mA Load**
- **2.2ms (MAX1963) or 70ms (MAX1976) $\overline{\text{RESET}}$ Output Flag**
- **Supply Current Independent of Load and Dropout Voltage**
- **Logic-Controlled Shutdown**
- **Thermal-Overload and Short-Circuit Protection**
- **Preset Output Voltages (0.75V to 3.0V)**
- **Tiny 6-Pin Thin SOT23 Package (<1.1mm High)**
- **Thin 6-Pin TDFN Package (<0.8mm High)**

Ordering Information

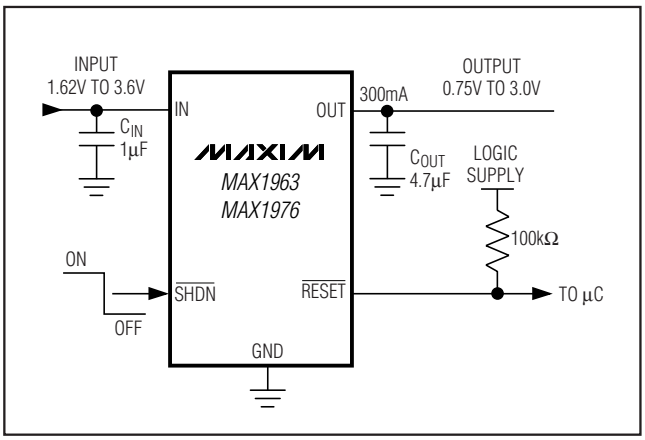
PART*	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX1963EZT_ _ _-T	-40°C to +85°C	6 Thin SOT23-6	Z6-1
MAX1963ETT_ _ _-T	-40°C to +85°C	6 TDFN	T633-2
MAX1976EZT_ _ _-T	-40°C to +85°C	6 Thin SOT23-6	Z6-1
MAX1976ETT_ _ _-T	-40°C to +85°C	6 TDFN	T633-2

**Insert the desired three-digit suffix (see the Selector Guide) into the blanks to complete the part number. Contact the factory for other output voltages.*

Pin Configurations



Typical Operating Circuit



Selector Guide appears at end of data sheet.

Low-Input-Voltage, 300mA LDO Regulators with RESET in SOT and TDFN

ABSOLUTE MAXIMUM RATINGS

IN, SHDN, RESET to GND .....-0.3V to +4.0V
OUT to GND .....-0.3V to (V_{IN} + 0.3V)
Output Short-Circuit Duration.....Continuous
Continuous Power Dissipation (T_A = +70°C)
6-Pin SOT23 (derate 9.1mW/°C above +70°C).....727mW
6-Pin TDFN (derate 24.4mW/°C above +70°C) 1951mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature..... +150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = (V_{OUT} + 0.5V) or 1.8V, whichever is greater; SHDN = IN, C_{IN} = 1µF, C_{OUT} = 4.7µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}			1.62		3.60	V
Input Undervoltage Lockout	V_{UVLO}	V_{IN} rising or falling (180mV typical hysteresis)		1.30		1.60	V
Output Voltage Accuracy		I_{OUT} = 1mA to 300mA, V_{IN} = (V_{OUT} + 0.5V) to +3.6V		-2.5	±0.5	+2.5	%
Maximum Output Current	I_{OUT}	Continuous		300			mA_{RMS}
Current Limit	I_{LIM}	V_{OUT} = 96% of nominal value		450	550	650	mA
Ground Current	I_Q	No load			70	140	µA
		I_{OUT} = 300mA			90		
		Dropout (Note 2)			70		
Dropout Voltage	V_{IN} - V_{OUT}	I_{OUT} = 300mA, V_{OUT} ≥ 1.8V (Note 2)			100	200	mV
Load Regulation	ΔV_{LDR}	I_{OUT} = 1mA to 300mA			0.02	0.3	%
Line Regulation	ΔV_{LNR}	V_{IN} = (V_{OUT} + 0.5V) to +3.6V, I_{OUT} = 1mA		-0.15	+0.01	+0.15	%/V
Output Noise		10Hz to 100kHz, I_{OUT} = 10mA, V_{OUT} = 1.5V			86		$µV_{RMS}$
PSRR		f < 1kHz, I_{OUT} = 10mA			70		dB
SHUTDOWN							
Shutdown Supply Current	I_{OFF}	SHDN = GND	T_A = +25°C		0.001	1	µA
			T_A = +85°C		0.01		
SHDN Input Logic Levels	V_{IH}	V_{IN} = 1.62V to 3.6V		1.4			V
	V_{IL}	V_{IN} = 1.62V to 3.6V				0.6	
SHDN Input Bias Current	I_{SHDN}	V_{SHDN} = 0 or 3.6V	T_A = +25°C		1	300	nA
			T_A = +85°C		5		
Turn-On Delay		From SHDN high to OUT high, V_{OUT} = 1.8V			90		µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = (V_{OUT} + 0.5V) or 1.8V, whichever is greater; $\overline{SHDN}$ = IN, C_{IN} = 1µF, C_{OUT} = 4.7µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

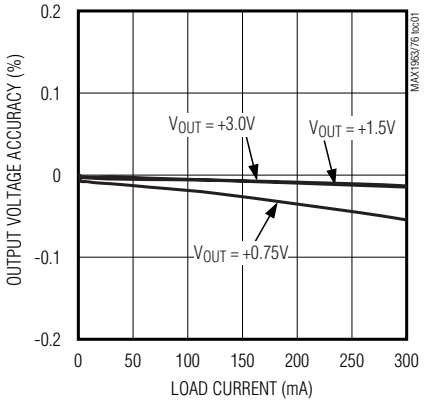
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{RESET}$ OUTPUT							
Reset Threshold Accuracy		V_{OUT} falling, (1.7% typical hysteresis)		80	82.5	85	%V_{OUT}
$\overline{RESET}$ Output Low Voltage	V_{OL}	$I_{\overline{RESET}}$ = 100µA			1	100	mV
		V_{IN} = +1.0V, $I_{\overline{RESET}}$ = 100µA			30	400	
$\overline{RESET}$ Output High Leakage	I_{OH}	$V_{\overline{RESET}}$ = 3.6V, $\overline{RESET}$ not asserted	T_A = +25°C		0.001	1	µA
			T_A = +85°C		0.01		
Reset Delay	t_{RP}	From V_{OUT} high to $\overline{RESET}$ rising	MAX1963	2.2	3.2	5.5	ms
			MAX1976	70	100	160	
THERMAL PROTECTION							
Thermal-Shutdown Temperature	$T_{\overline{SHDN}}$				+165		°C
Thermal-Shutdown Hysteresis	$\Delta T_{\overline{SHDN}}$				15		°C

Note 1: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.
Note 2: The dropout voltage is defined as V_{IN} - V_{OUT}, when V_{OUT} is 4% lower than the value of V_{OUT} when V_{IN} = V_{OUT} + 0.5V.

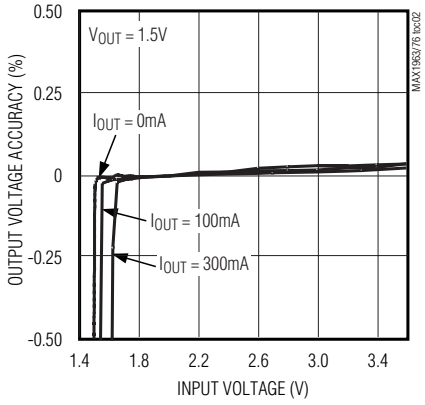
Typical Operating Characteristics

(V_{IN} = (V_{OUT} + 0.5V) or 1.8V, whichever is greater; $\overline{SHDN}$ = IN, C_{IN} = 1µF, C_{OUT} = 4.7µF, T_A = +25°C, unless otherwise noted.)

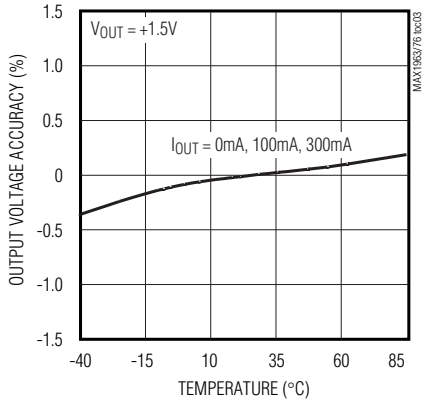
OUTPUT VOLTAGE ACCURACY vs. LOAD CURRENT



OUTPUT VOLTAGE ACCURACY vs. INPUT VOLTAGE



OUTPUT VOLTAGE ACCURACY vs. TEMPERATURE

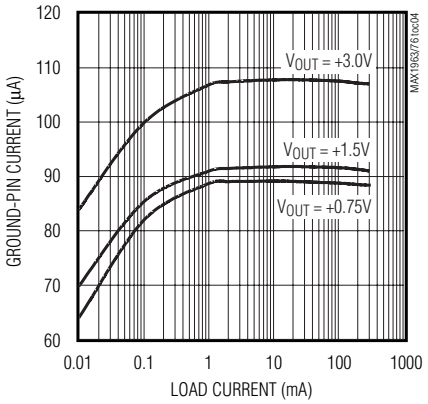


Low-Input-Voltage, 300mA LDO Regulators with $\overline{\text{RESET}}$ in SOT and TDFN

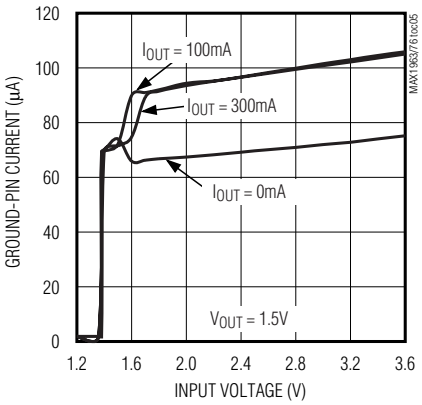
Typical Operating Characteristics (continued)

(V_{IN} = (V_{OUT} + 0.5V) or 1.8V, whichever is greater; $\overline{SHDN}$ = IN, C_{IN} = 1µF, C_{OUT} = 4.7µF, T_A = +25°C, unless otherwise noted.)

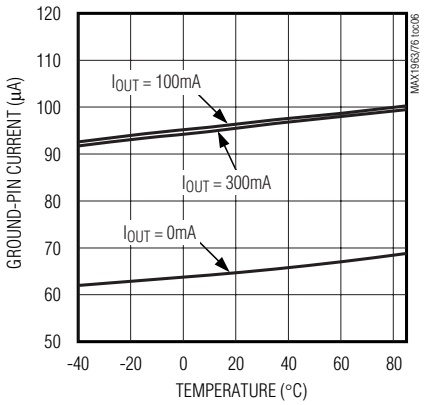
GROUND-PIN CURRENT vs. LOAD CURRENT



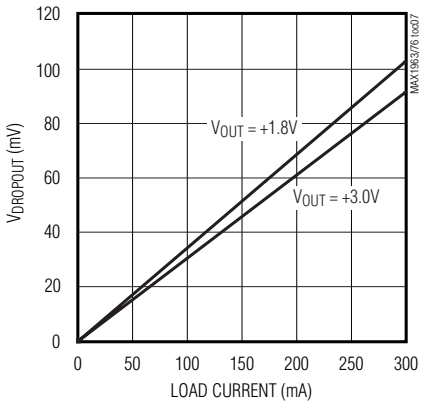
GROUND-PIN CURRENT vs. INPUT VOLTAGE



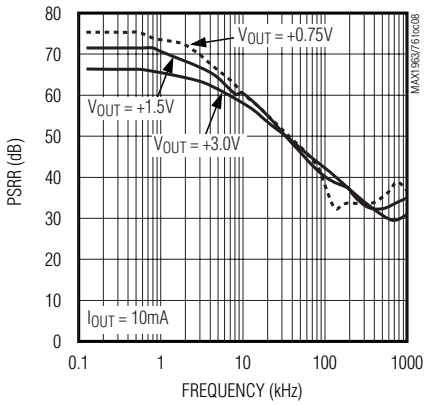
GROUND-PIN CURRENT vs. TEMPERATURE



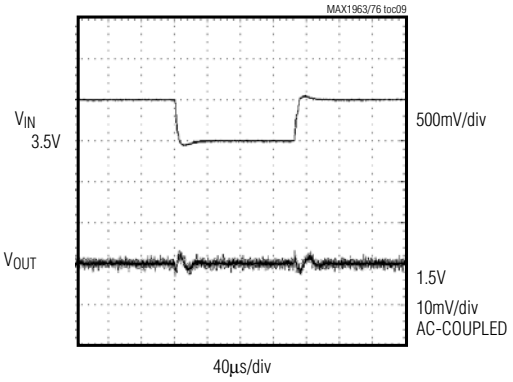
DROPOUT VOLTAGE vs. LOAD CURRENT



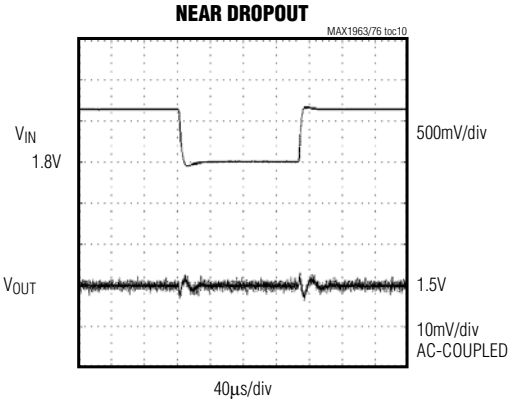
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



LINE-TRANSIENT RESPONSE



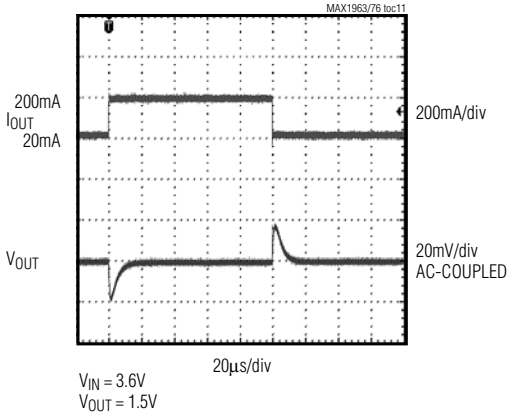
LINE-TRANSIENT RESPONSE NEAR DROPOUT



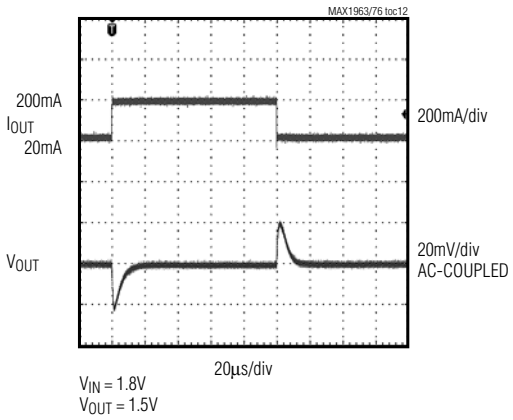
Typical Operating Characteristics (continued)

(V_{IN} = (V_{OUT} + 0.5V) or 1.8V, whichever is greater; $\overline{SHDN}$ = IN, C_{IN} = 1µF, C_{OUT} = 4.7µF, T_A = +25°C, unless otherwise noted.)

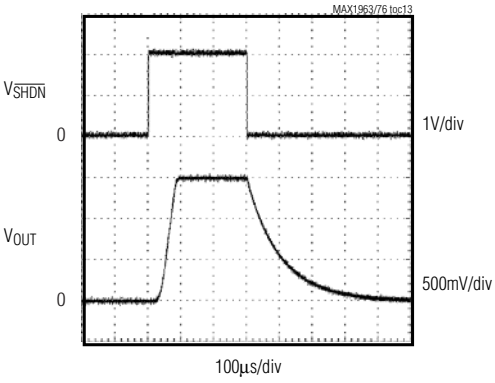
LOAD-TRANSIENT RESPONSE



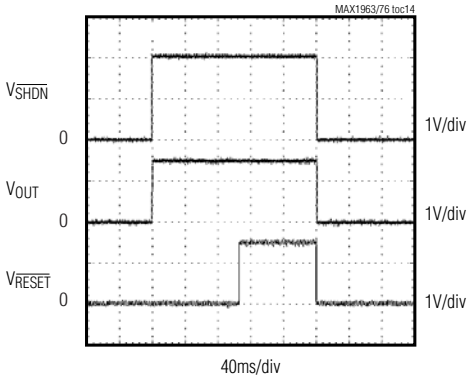
LOAD-TRANSIENT RESPONSE NEAR DROPOUT



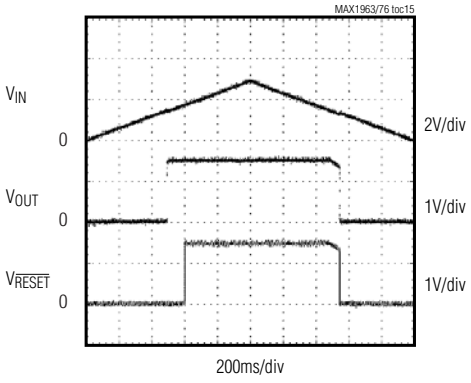
SHUTDOWN RESPONSE



MAX1976A SHUTDOWN/RESET RESPONSE



MAX1976A LINE/RESET RESPONSE



Low-Input-Voltage, 300mA LDO Regulators with RESET in SOT and TDFN

Pin Description

PIN		NAME	FUNCTION
SOT23	TDFN		
1	6	IN	Regulator Input. Supply voltage can range from +1.62V to +3.6V. Bypass IN with at least a 1µF ceramic capacitor to GND (see the *Capacitor Selection and Regulator Stability* section).
2	—	GND	Ground. GND also functions as a heatsink. Solder to a large pad or circuit-board ground plane to maximize SOT23 power dissipation.
—	4	GND	Ground
3	5	$\overline{SHDN}$	Active-Low Shutdown Input. A logic low reduces supply current to below 1µA. Connect to IN or logic high for normal operation.
4	3	$\overline{RESET}$	Open-Drain, Active-Low Reset Output. $\overline{RESET}$ rises 3.2ms (MAX1963) or 100ms (MAX1976) after the output has achieved regulation. $\overline{RESET}$ falls immediately if V_{OUT} drops below 82.5% of its nominal voltage, or if the MAX1963/MAX1976 are shut down.
5	2	I.C.	Internally Connected. Leave floating or connect to GND.
6	1	OUT	Regulator Output. Sources up to 300mA. Bypass with a 4.7µF low-ESR ceramic capacitor to GND.
—	Exposed Pad	EP	Ground. EP also functions as a heatsink. Solder EP to a large pad or circuit-board ground plane to maximize TDFN power dissipation.

Detailed Description

The MAX1963/MAX1976 are low-dropout, high-accuracy, low-quiescent-current linear regulators designed primarily for battery-powered applications. These devices supply loads up to 300mA and are available with preset output voltages from +0.75V to +3.0V. As illustrated in Figure 1, the MAX1963/MAX1976 consist of a reference, an error amplifier, a P-channel pass transistor, an internal feedback voltage-divider, and a power-good comparator.

The reference is connected to the error amplifier, which compares this reference with the feedback voltage and amplifies the difference. If the feedback voltage is lower than the reference voltage, the pass-transistor gate is pulled lower, which allows more current to pass to the output and increases the output voltage. If the feedback voltage is too high, the pass-transistor gate is pulled up, allowing less current to pass to the output.

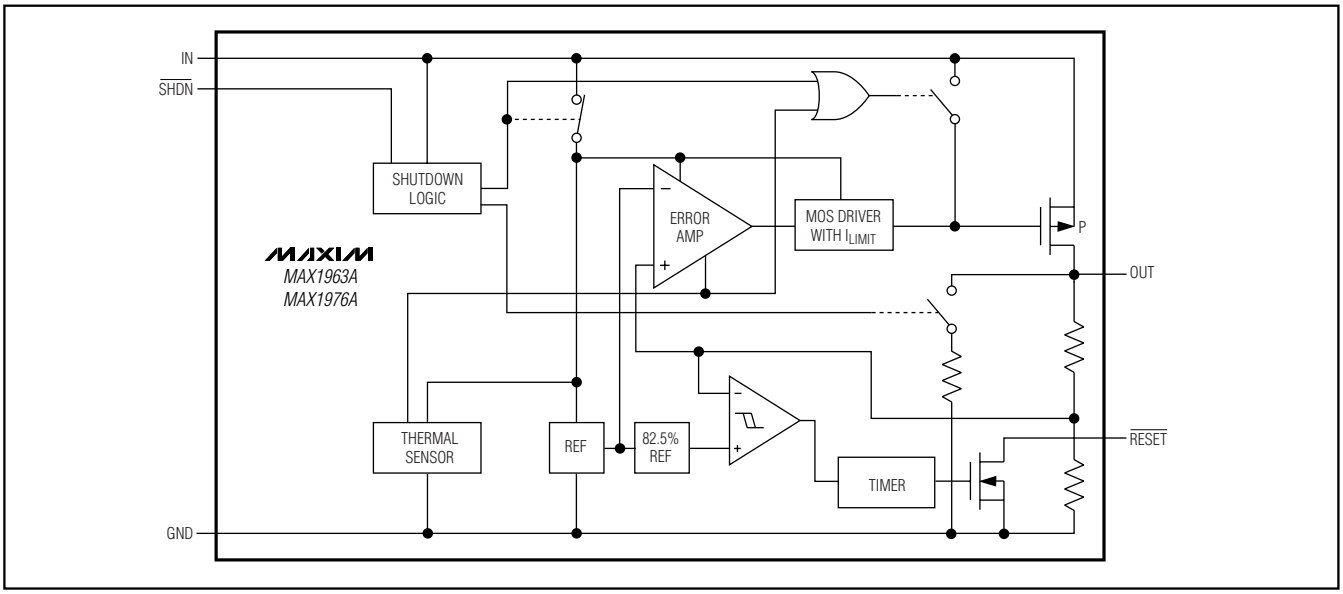


Figure 1. Functional Diagram

Internal P-Channel Pass Transistor

The MAX1963/MAX1976 feature a 0.33Ω ($R_{DS(ON)}$) P-channel MOSFET pass transistor. Unlike similar designs using PNP pass transistors, P-channel MOSFETs require no base drive, which reduces quiescent current. PNP-based regulators also waste considerable current in dropout when the pass transistor saturates and use high base-drive currents under large loads. The MAX1963/MAX1976 do not suffer from these problems and consume only 90µA (typ) of quiescent current under heavy loads, as well as in dropout.

Shutdown

Pull $\overline{SHDN}$ low to enter shutdown. During shutdown, the output is disconnected from the input, an internal 1.5kΩ resistor pulls OUT to GND, $\overline{RESET}$ is actively pulled low, and the supply current drops below 1µA.

$\overline{RESET}$ Output

The MAX1963/MAX1976 microprocessor (µP) supervisory circuitry asserts a guaranteed logic-low reset during power-up, power-down, and brownout conditions down to +1V. $\overline{RESET}$ asserts when V_{OUT} is below the reset threshold and remains asserted for at least t_{RP} after V_{OUT} rises above the reset threshold of regulation.

Current Limit

The MAX1963/MAX1976 monitor and control the pass transistor's gate voltage, limiting the output current to 450mA (min). If the output exceeds I_{LIM}, the MAX1963/MAX1976 output voltage drops.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the MAX1963/MAX1976. When the junction temperature exceeds T_J = +165°C, a thermal sensor turns off the pass transistor, allowing the IC to cool. The thermal sensor turns the pass transistor on again after the junction temperature cools by 15°C, resulting in a pulsed output during continuous thermal-overload conditions. Thermal-overload protection safeguards the MAX1963/MAX1976 in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction-temperature rating of T_J = +150°C.

Operating Region and Power Dissipation

The MAX1963/MAX1976 maximum power dissipation depends on the thermal resistance of the IC package and circuit board, the temperature difference between the die junction and ambient air, and the rate of airflow. The power dissipated in the device is $P = I_{OUT} \times (V_{IN} - V_{OUT})$. The maximum allowed power dissipation is:

$$P_{MAX} = (T_{J(MAX)} - T_A) / (\theta_{JC} + \theta_{CA})$$

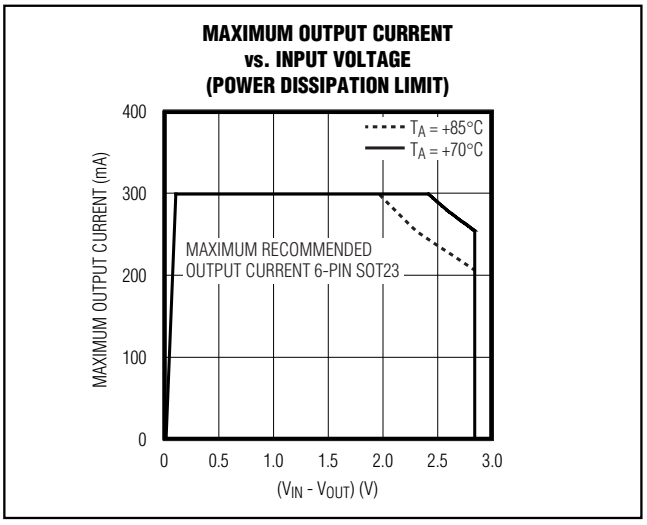


Figure 2. Power Operating Regions for the 6-Pin SOT23: Maximum Output Current vs. Input Voltage

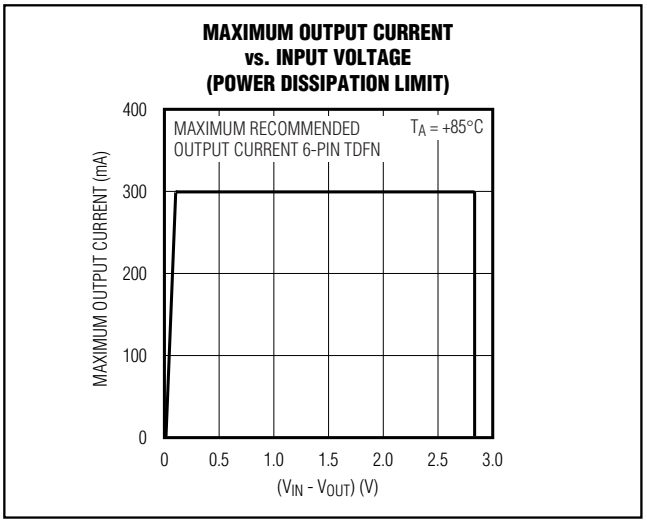


Figure 3. Power Operating Regions for the 6-Pin TDFN: Maximum Output Current vs. Input Voltage

where ($T_{J(MAX)}$ - T_A) is the temperature difference between the MAX1963/MAX1976 die junction and the surrounding air, θ_{JC} is the thermal resistance of the junction to the case, and θ_{CA} is the thermal resistance from the case through the PC board, copper traces, and other materials to the surrounding air. For best heatsinking, expand the copper connected to the exposed paddle or GND.

Low-Input-Voltage, 300mA LDO Regulators with RESET in SOT and TDFN

The MAX1963/MAX1976 deliver up to 300mA and operate with an input voltage up to +3.6V. However, when using the 6-pin SOT23 version, high output currents can only be sustained when the input-output differential voltage is less than 2V, as shown in Figure 2.

The maximum allowed power dissipation for the 6-pin TDFN is 1.951W at T_A = +70°C. Figure 3 shows that the maximum input-output differential voltage is not limited by the TDFN package power rating.

Applications Information

Capacitor Selection and Regulator Stability

Capacitors are required at the MAX1963/MAX1976 input and output for stable operation over the full temperature range and with load currents up to 300mA. Connect a 1µF ceramic capacitor between IN and GND and a 4.7µF low-ESR ceramic capacitor between OUT and GND. The input capacitor (C_{IN}) lowers the source impedance of the input supply. Use larger output capacitors to reduce noise and improve load-transient response, stability, and power-supply rejection.

The output capacitor's equivalent series resistance (ESR) affects stability and output noise. Use output capacitors with an ESR of 30mΩ or less to ensure stability and optimize transient response. Surface-mount ceramic capacitors have very low ESR and are commonly available in values up to 10µF. Connect C_{IN} and C_{OUT} as close to the MAX1963/MAX1976 as possible to minimize the impact of PC board trace inductance.

Noise, PSRR, and Transient Response

The MAX1963/MAX1976 are designed to operate with low dropout voltages and low quiescent currents in battery-powered systems while still maintaining good noise, transient response, and AC rejection. See the *Typical Operating Characteristics* for a plot of Power-Supply Rejection Ratio (PSRR) versus Frequency. When operating from noisy sources, improved supply-noise rejection and transient response can be achieved by increasing the values of the input and output bypass capacitors and through passive filtering techniques.

The MAX1963/MAX1976 load-transient response (see the *Typical Operating Characteristics*) shows two components of the output response: a near-zero DC shift from the output impedance due to the load-current change, and the transient response. A typical transient response for a step change in the load current from 20mA to 200mA is 20mV. Increasing the output capacitor's value and decreasing the ESR attenuates the overshoot.

Input-Output (Dropout) Voltage

A regulator's minimum input-output voltage difference (dropout voltage) determines the lowest usable supply voltage. In battery-powered systems, this determines the useful end-of-life battery voltage. Because the MAX1963/MAX1976 use a P-channel MOSFET pass transistor, the dropout voltage is a function of drain-to-source on-resistance ($R_{DS(ON)}$ = 0.33Ω) multiplied by the load current (see the *Typical Operating Characteristics*).

$$V_{DROPOUT} = V_{IN} - V_{OUT} = 0.33\Omega \times I_{OUT}$$

The MAX1963/MAX1976 ground current reduces to 70µA in dropout.

Selector Guide

V_{OUT} (V)	SUFFIX	MAX1963 TOP MARK		MAX1976 TOP MARK	
		SOT	TDFN	SOT	TDFN
0.75	075	**AABA**	**AFQ**	**AAAQ**	**AGA**
0.85	085	—	—	**AABP**	**AHD**
0.90	090	**AABB**	**AFR**	**AABK**	AGB
1.00	100	**AABC**	**AFS**	**AABL**	**AGC**
1.10	110	**AABD**	**AFT**	**AABM**	**AGD**
1.20	120	**AABE**	**AFU**	**AAAK**	**AGE**
1.30	130	**AABF**	**AFV**	**AABN**	**AGF**
1.50	150	**AABG**	**AFW**	**AAAL**	**AGG**
1.60	160	—	—	**AABO**	**AHC**
1.80	180	**AABH**	**AFX**	**AAAM**	**AGH**
2.50	250	**AABI**	**AFY**	**AAAN**	**AGI**
2.85	285	—	—	**AAAO**	AGJ
3.00	300	**AABJ**	**AFZ**	**AAAP**	**AGK**

*(Note: Standard voltage options, shown in **bold**, are available. Contact the factory for other output voltages between 1.5V and 4.5V. Minimum order quantity is 15,000 units.)*

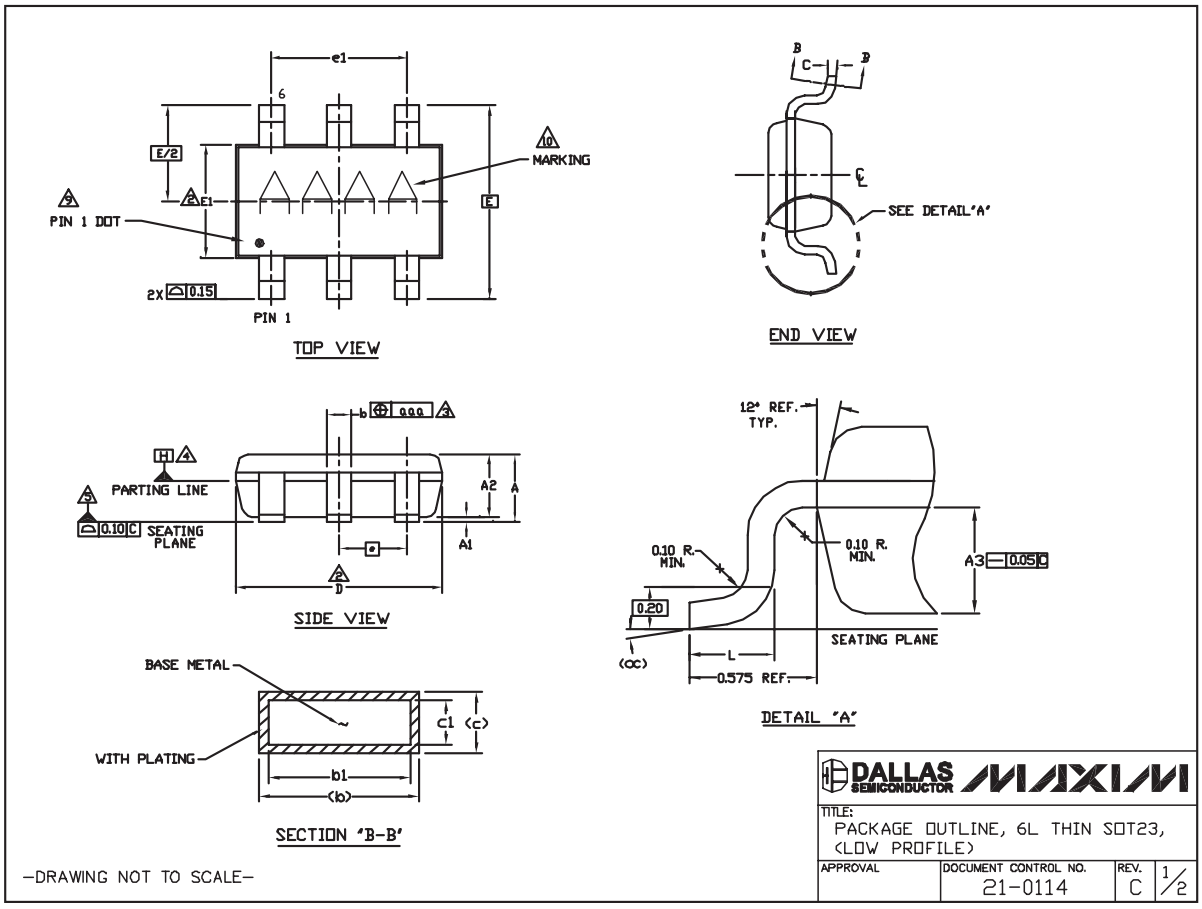
Chip Information

TRANSISTOR COUNT: 2556

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Low-Input-Voltage, 300mA LDO Regulators with $\overline{\text{RESET}}$ in SOT and TDFN

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. "D" AND "E1" ARE REFERENCE DATUM AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE BOTTOM PARTING LINE. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15mm ON "D" AND 0.25mm ON "E" PER SIDE.
3. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.07mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DATUM PLANE "H" LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT THE BOTTOM OF PARTING LINE.
5. THE LEAD TIPS MUST LINE WITHIN A SPECIFIED TOLERANCE ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL LINES, ONE PLANE IS THE SEATING PLANE, DATUM [-C-], AND THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITH 0.10mm AT SEATING PLANE.
6. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-193 EXCEPT FOR THE "e" DIMENSION WHICH IS 0.95mm INSTEAD OF 1.00mm. THIS PART IS IN FULL COMPLIANCE TO EIAJ SPECIFICATION SC-74.
7. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
8. WARPAGE SHALL NOT EXCEED 0.10mm.
9. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 PP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.

SYMBOLS			
	MIN	NOM	MAX
A	-	-	1.10
A1	0.00	0.075	0.10
A2	0.85	0.88	0.90
A3		0.50 BSC	
b	0.30	-	0.45
b1	0.25	0.35	0.40
c	0.15	-	0.20
c1	0.12	0.127	0.15
D	2.80	2.90	3.00
E		2.75 BSC	
E1	1.55	1.60	1.65
L	0.30	0.40	0.50
e1		1.90 BSC	
e		0.95 BSC	
OC	0°	4°	8°
aaa		0.20	
Pkg. codes: Z6-1, Z6-2			

DALLAS SEMICONDUCTOR MAXIM

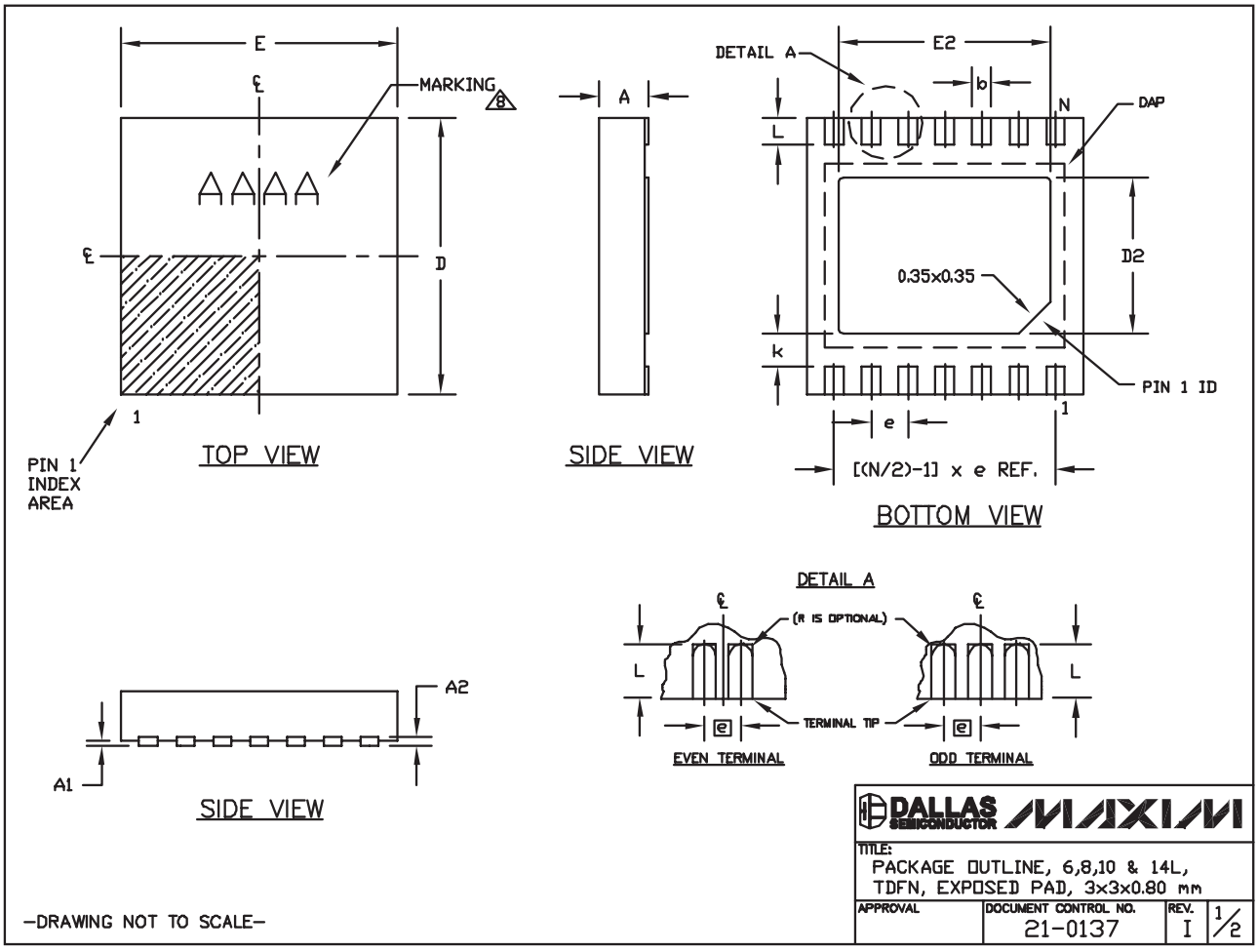
TITLE: PACKAGE OUTLINE, 6L THIN SOT23, (LOW PROFILE)

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0114	C	2/2

-DRAWING NOT TO SCALE-

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Low-Input-Voltage, 300mA LDO Regulators with RESET in SOT and TDFN

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0137	I	2/2

Revision History

Pages changed at Rev 2: 1, 2, 9–12