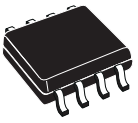
LK115XX30
LK115XX33 - LK115XX50

Very low drop with inhibit voltage regulators

Features

- Very low dropout voltage (0.2 V typ.)
- Very low quiescent current
  (Typ. 0.01 µA in off mode, 280 µA in on mode)
- Output current up to 100 mA
- Two logic-controlled electronic shutdowns
- Output voltages of 3.0; 3.3; 5.0 V
- Internal current and thermal limit
- Only 2.2 µF for stability
- V_{OUT} tolerance ± 3 % at 25 °C
- Supply voltage rejection: 80 dB (typ)
- Temperature range: -40 °C to 125 °C



SO-8

It requires only a 2.2 µF capacitor for stability allowing space and cost saving.

Description

The LK115XX series are very low drop regulators available in SO-8 package and in a wide range of output voltages.

The very low drop voltage (0.2 V) and the very low quiescent current (0.01 µA in OFF MODE, 280 µA in ON MODE) make them particularly suitable for low noise, low power applications and specially in battery powered systems.

Both active HIGH and active LOW shutdown logic control are available (pin 2 and 3). This means that when the device is used as a local regulator, it is possible to put a part of the board in standby, decreasing the total power consumption.

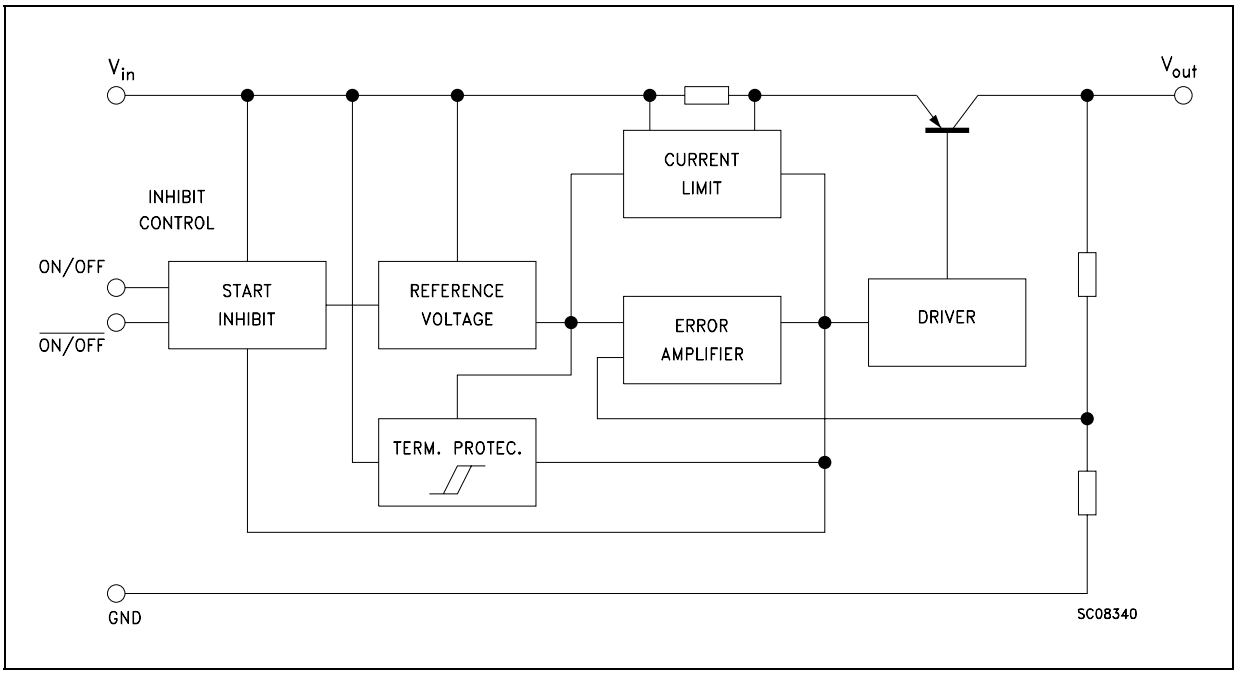
Table 1. Device summary

Order codes	Output voltages
LK115D30-TR	3 V
LK115D33-TR	3.3 V
LK115D50-TR	5 V

Contents

1 Diagram

Figure 1. Schematic diagram



2 Pin configuration

Figure 2. Pin connection (top view)

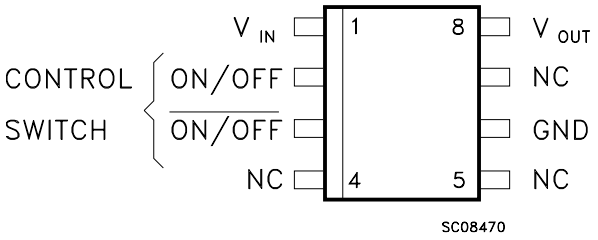


Table 2. Truth table

ON/$\overline{\text{OFF}}$ (Pin 2)	$\overline{\text{ON}}$/OFF (Pin 3)	Status
H	L	ON
H	H	OFF
L	L	OFF
L	H	NOT ALLOWED

Note: Logic levels are those defined in the electrical characteristics.

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_I	DC input voltage	20	V
I_O	Output current	Internally limited	
P_{TOT}	Power dissipation	Internally limited	
T_{STG}	Storage temperature range	-40 to 150	°C
T_{OP}	Operating junction temperature range	-40 to 125	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

4 Test circuits

Figure 3. Supply current (On mode)

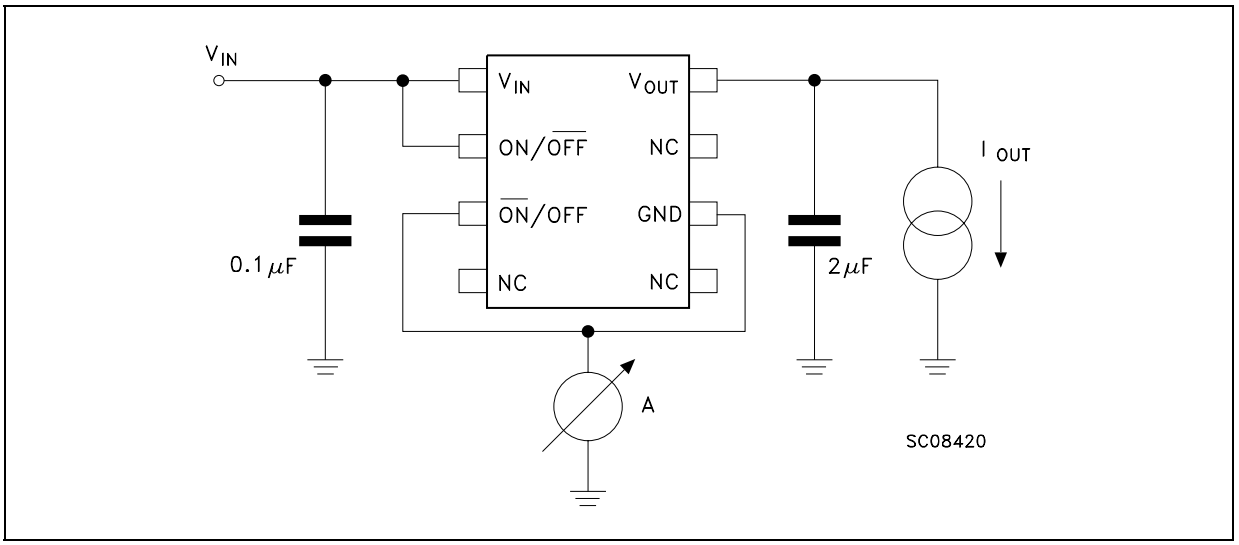
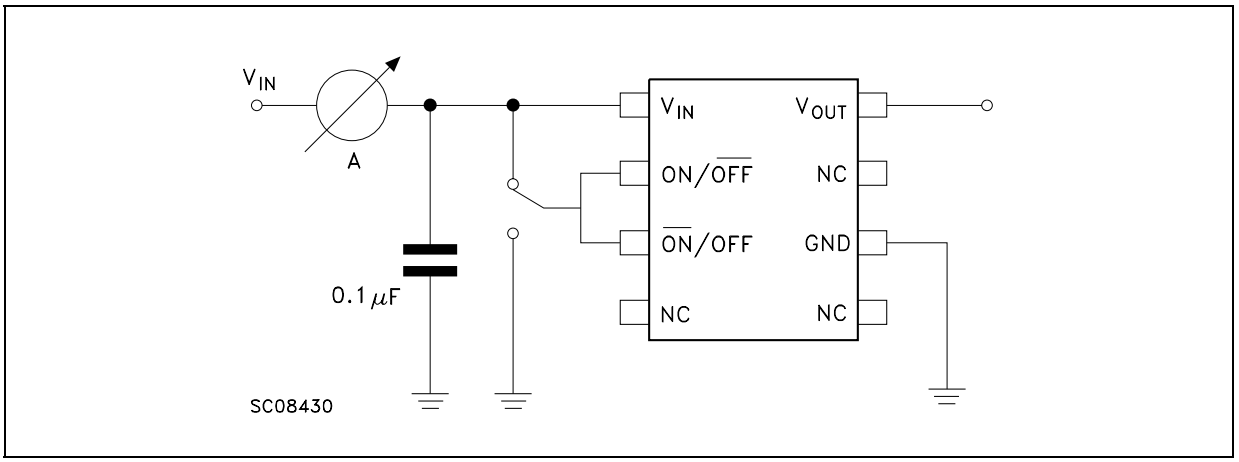


Figure 4. Supply current (Off mode)



Note: The switch emulates the two possibilities to set the regulator in OFF mode.

5 Electrical characteristics

Table 4. Electrical characteristics for LK115D30 (refer to the test circuits, T_J = 25 °C, C_I = 0.1 µF, C_O = 2.2 µF unless otherwise specified.)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_O	Output voltage	I_O = 10 mA, V_I = 5 V		2.910	3	3.090	V
		I_O = 10 mA, V_I = 5 V, T_a= -40 to 125°C		2.850		3.150	
V_I	Operating input voltage	I_O = 100 mA				20	V
I_{out}	Output current limit			120	200		mA
ΔV_O	Line regulation	V_I = 4 to 20 V, I_O = 0.5 mA			2	10	mV
ΔV_O	Load regulation	V_I = 4 V, I_O = 0.5 to 100 mA			4	20	mV
I_d	Quiescent current (On Mode)	V_I = 4 to 20 V, I_O = 0			0.28	0.5	mA
		V_I = 4 to 20 V, I_O = 100 mA			1.5	3	
	(Off Mode)	V_I = 4 to 20 V			0.01	2	µA
SVR	Supply voltage rejection	I_O = 5 mA V_I = 5 V ± 1V	f = 120 Hz		79		dB
			f = 1 kHz		74		
			f = 10 kHz		57		
eN	Output noise voltage (RMS)	B = 10 Hz to 100 kHz			66		µV
V_d	Dropout voltage	I_O = 60 mA			0.17		V
V_{HIc}	ON/$\overline{OFF}$ Control (pin 2)	Pin 3 to GND, OFF		0		0.5	V
		Pin 3 to GND, ON		2.4		V_{in}	
V_{LIc}	$\overline{ON}$/OFF Control (pin 3)	Pin 2 to V_{in}, OFF		V_{in}-0.2		V_{in}	V
		Pin 2 to V_{in}, ON		0		V_{in}-2.4	
C_O	Output bypass capacitance	ESR = 0.5 to 10 Ω, I_O = 0 to 100 mA		2	10		µF

Table 5. Electrical characteristics for LK115D33 (refer to the test circuits, T_J = 25 °C, C_I = 0.1 µF, C_O = 2.2 µF unless otherwise specified.)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_O	Output voltage	I_O = 10 mA, V_I = 5.3 V		3.2	3.3	3.4	V
		I_O = 10 mA, V_I = 5.3 V, T_a= -40 to 125°C		3.135		3.465	
V_I	Operating input voltage	I_O = 100 mA				20	V
I_{out}	Output current limit			120	200		mA
ΔV_O	Line regulation	V_I = 4.3 to 20 V, I_O = 0.5 mA			2	10	mV
ΔV_O	Load regulation	V_I = 4.3 V, I_O = 0.5 to 100 mA			4	20	mV
I_d	Quiescent current (On Mode)	V_I = 4.3 to 20 V, I_O = 0			0.28	0.5	mA
		V_I = 4.3 to 20 V, I_O = 100 mA			1.5	3	
	(Off Mode)	V_I = 4.3 to 20 V			0.01	2	µA
SVR	Supply voltage rejection	I_O = 5 mA V_I = 5.3 V ± 1V	f = 120 Hz		79		dB
			f = 1 kHz		74		
			f = 10 kHz		57		
eN	Output noise voltage (RMS)	B = 10 Hz to 100 kHz			72.6		µV
V_d	Dropout voltage	I_O = 60 mA			0.17		V
V_{HIc}	ON/$\overline{OFF}$ Control (pin 2)	Pin 3 to GND, OFF		0		0.5	V
		Pin 3 to GND, ON		2.4		V_{in}	
V_{LIc}	$\overline{ON}$/OFF Control (pin 3)	Pin 2 to V_{in}, OFF		V_{in}-0.2		V_{in}	V
		Pin 2 to V_{in}, ON		0		V_{in}-2.4	
C_O	Output bypass capacitance	ESR = 0.5 to 10Ω, I_O = 0 to 100 mA		2	10		µF

Table 6. Electrical characteristics for LK115D50 (refer to the test circuits, T_J = 25 °C, C_I = 0.1 µF, C_O = 2.2 µF unless otherwise specified.)

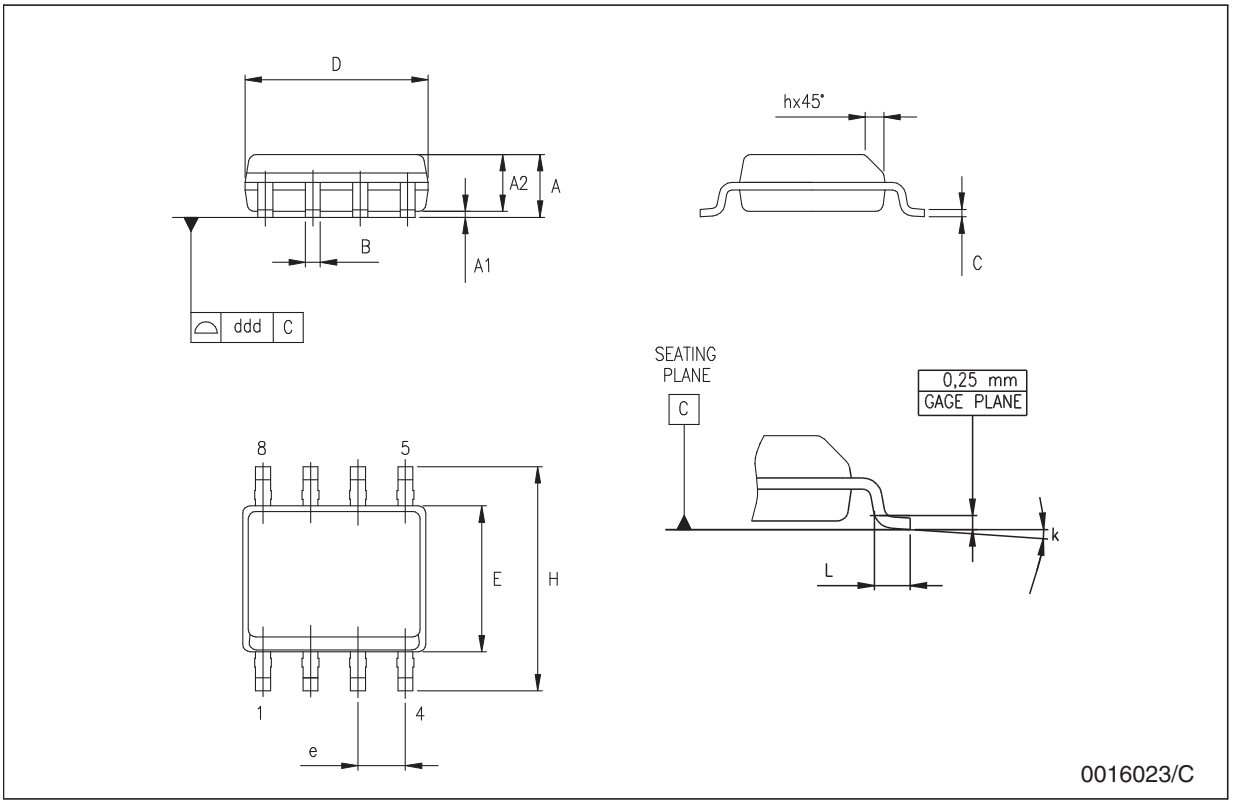
Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_O	Output voltage	I_O = 10 mA, V_I = 7 V		4.85	5	5.15	V
		I_O = 10 mA, V_I = 7 V, T_a= -40 to 125°C		4.75		5.25	
V_I	Operating input voltage	I_O = 100 mA				20	V
I_{out}	Output current limit			120	200		mA
ΔV_O	Line regulation	V_I = 6 to 20 V, I_O = 0.5 mA			3	15	mV
ΔV_O	Load regulation	V_I = 6 V, I_O = 0.5 to 100 mA			4	20	mV
I_d	Quiescent current (On Mode)	V_I = 6 to 20 V, I_O = 0			0.28	0.5	mA
		V_I = 6 to 20 V, I_O = 100 mA			1.5	3	
	(Off Mode)	V_I = 6 to 20 V			0.01	2	µA
SVR	Supply voltage rejection	I_O = 5 mA V_I = 7 V ± 1V	f = 120 Hz		75		dB
			f = 1 kHz		70		
			f = 10 kHz		55		
eN	Output noise voltage (RMS)	B = 10 Hz to 100 kHz			110		µV
V_d	Dropout voltage	I_O = 60 mA			0.17		V
V_{HIc}	ON/$\overline{OFF}$ Control (pin 2)	Pin 3 to GND, OFF		0		0.5	V
		Pin 3 to GND, ON		2.4		V_{in}	
V_{LIc}	$\overline{ON}$/OFF Control (pin 3)	Pin 2 to V_{in}, OFF		V_{in}-0.2		V_{in}	V
		Pin 2 to V_{in}, ON		0		V_{in}-2.4	
C_O	Output bypass capacitance	ESR = 0.5 to 10Ω, I_O = 0 to 100 mA		2	10		µF

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

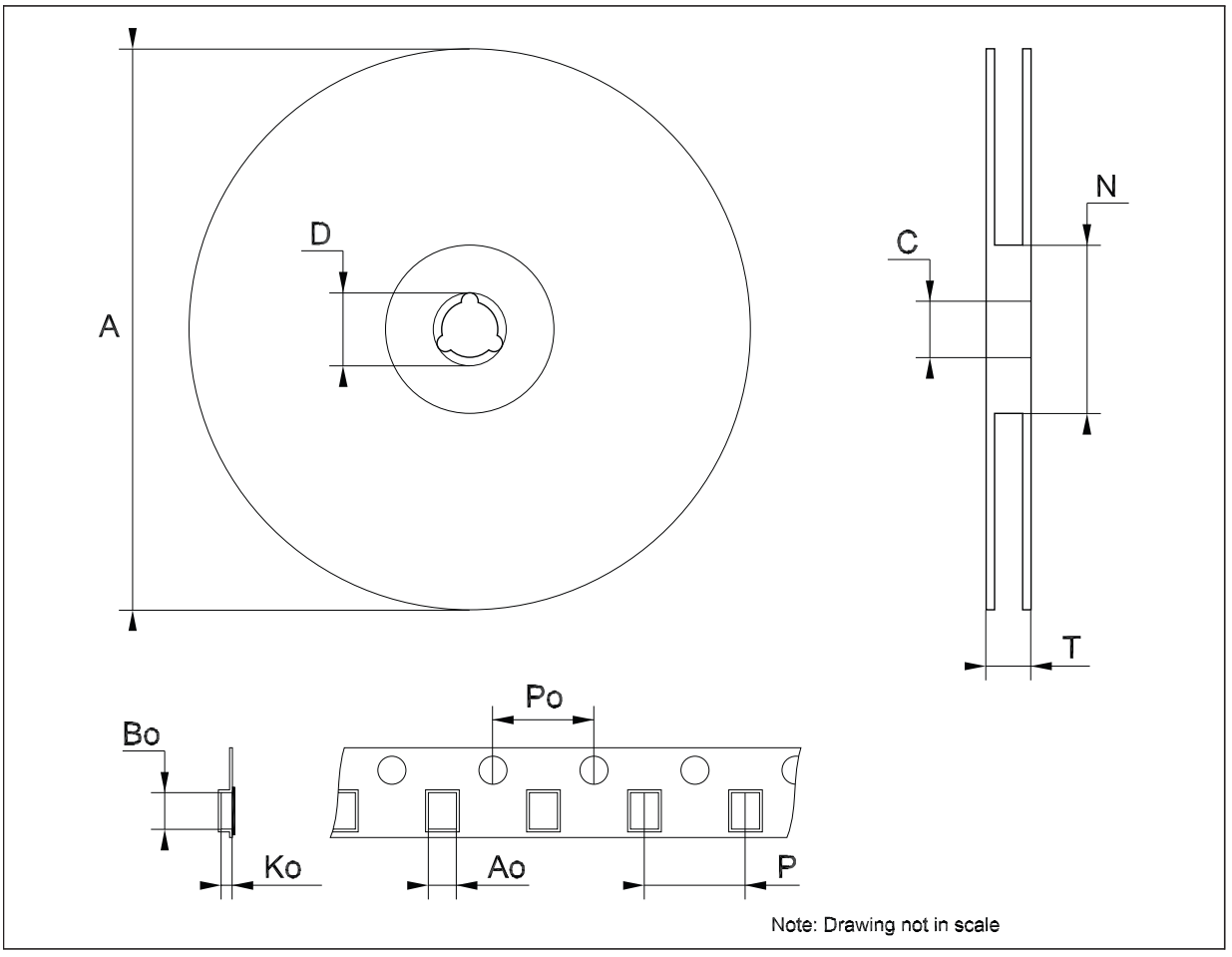
SO-8 mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



Tape & reel SO-8 mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	8.1		8.5	0.319		0.335
Bo	5.5		5.9	0.216		0.232
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Note: Drawing not in scale

7 Revision history

Table 7. Document revision history

Date	Revision	Changes
07-Jun-2006	3	Order codes updated.
07-Jul-2008	4	Added *Table 1 on page 1*.