LF155/A/156/A/157/A, LF255/256/257,
LF355/A/356/A/357/A-T

DESCRIPTION

LF155, LF155A, LF255, LF355, LF355A (Low Supply Current)
LF156, LF156A, LF256, LF356, LF356A (Wide Band)
LF157, LF157A, LF257, LF357, LF357A (Wide Band)
The LF155, LF156, LF157 Series of operational amplifiers employ well matched, high voltage JFET input structures on the same monolithic chip as bipolar devices. These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time and low noise.

COMMON FEATURES

(LF155A/156A/157A)

- **Low input bias current 30pA**
- **Low input offset current 3pA**
- **High input impedance $10^{12}\Omega$**
- **Low input offset voltage 1mV**
- **Low V_{OS} temperature drift 3μV/°C**
- **Low input noise current 0.01pA/$\sqrt{Hz}$**

SPECIFIC FEATURES

	LF155A	LF156A
• Settling time (0.01%)	4μs	1.5μs
• High slew rate	5v/μs	12v/μs
• Wide bandwidth	2.5MHz	5MHz
• Low input noise	20nV/$\sqrt{Hz}$	12nV/$\sqrt{Hz}$

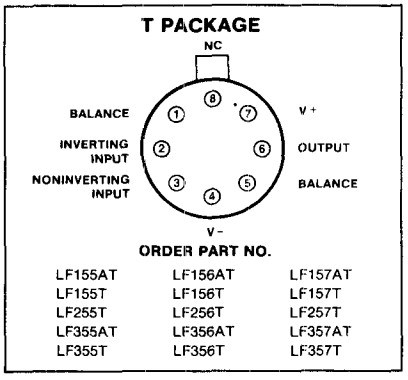
- **LF155, LF156—military qualifications pending**

	LF157A (A_V = 5)
• Settling time (0.01%)	1.5μs
• High slew rate	50v/μs
• Wide bandwidth	20MHz
• Low input noise	12nV/$\sqrt{Hz}$

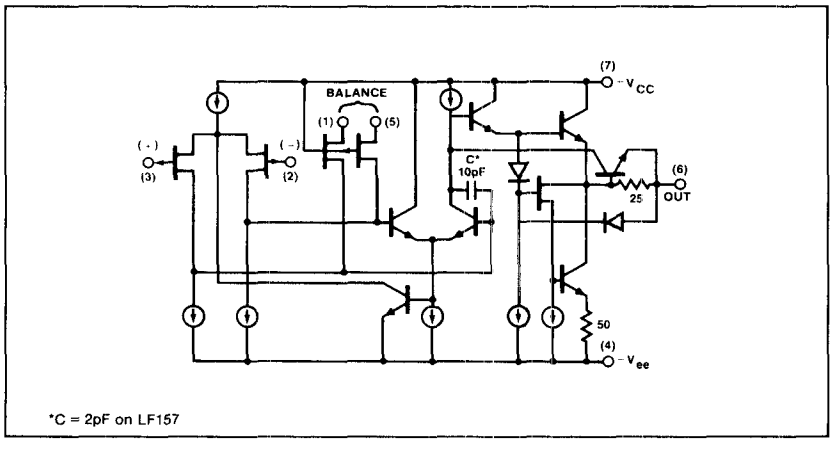
APPLICATIONS

- **Precision high speed integrators**
- **Fast A/D, D/A converters**
- **High impedance buffers**
- **Wideband, low noise, low drift amplifier**

PIN CONFIGURATION



EQUIVALENT SCHEMATIC



*C = 2pF on LF157

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
LF155A/6A/7A, LF155/6/7	±22	V
LF255/6/7	±22	V
LF355A/6A/7A, LF355/6/7	±18	V
Power dissipation[1] TO-99 (T-package)		
LF155A/6A/7A, LF155/6/7	670	mW
LF255/6/7	570	mW
LF355A/6A/7A, LF355/6/7	500	mW
Operating temperature range		
LF155A/6A/7A, LF155/6/7	-55 to +125	°C
LF255/6/7	-25 to +85	°C
LF355A/6A/7A, LF355/6/7	0 to +70	°C
T_J (Max)		
LF155A/6A/7A, LF155/6/7	150	°C
LF255/6/7	115	°C
LF355A/6A/7A, LF355/6/7	100	°C
Input voltage range[2]		
LF155A/6A/7A, LF155/6/7	±20	V
LF255/6/7	±20	V
LF355A/6A/7A, LF355/6/7	±20	V
Output short circuit duration		
LF155A/6A/7A, LF155/6/7	Continuous	
LF255/6/7	Continuous	
LF355A/6A/7A, LF355/6/7	Continuous	
Storage temperature range		
LF155A/6A/7A, LF155/6/7	-65 to +150	°C
LF255/6/7	-65 to +150	°C
LF355A/6A/7A, LF355/6/7	-65 to +150	°C
Lead temperature (soldering, 10sec.)	300	°C
LF155A/6A/7A, LF155/6/7	300	°C
LF255/6/7	300	°C
LF355A/6A/7A, LF355/6/7	300	°C

NOTES

1. The TO-99 package must be derated based on a thermal resistance of 150°C/W junction to ambient or 25°C/W junction to case.
2. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

LF155/A/156/A/157/A, LF255/256/257,
LF355/A/356/A/357/A-T

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C unless otherwise specified. (See notes on following page.)

PARAMETER		TEST CONDITIONS	LF155A/6A/7A			LF355A/6A/7A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	R_S = 50Ω		1	2 2.5		1	2 2.3	mV mV
$\Delta V_{OS}/\Delta T$	Avg. TC of input offset voltage	R_S = 50Ω		3	5		3	5	µV/°C
$\Delta TC/\Delta V_{OS}$	Change in average TC[2] with V_{OS} adjust	R_S = 50Ω		0.5			0.5		µV/°C per mV
I_{OS}	Input offset current[1,3]	T_J = 25°C $T_J \leq T_{high}$		3	10 10		3	10 1	pA nA
I_B	Input bias current[1,3]	T_J = 25°C $T_J \leq T_{high}$		30	50 25		30	50 5	pA nA
R_{IN}	Input resistance	T_J = 25°C		10^{12}			10^{12}		Ω
A_{VOL}	Large signal voltage gain	V_S = ± 15V V_O = ± 10V, R_L = 2kΩ Over temp.	50 25	200		50 25	200		V/mV V/mV
V_O	Output voltage swing	V_S = ± 15V, R_L = 10kΩ V_S = ± 15V, R_L = 2kΩ	±12 ±10	±13 ±12		±12 ±10	±13 ±12		V V
V_{CM}	Input common mode Voltage range	V_S = ± 15V	±11	+15.1 -12		±11	+15.1 -12		V V V
CMRR	Common-mode rejection ratio		85	100		85	100		dB
PSRR	Supply volt. rej. ratio[4]		85	100		85	100		dB

DC ELECTRICAL CHARACTERISTICS

(Cont'd) T_A = 25°C unless otherwise specified. (See notes on following page.)

PARAMETER		TEST CONDITIONS	LF155/6/7			LF255/6/7			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	R_S = 50Ω		3	5 7		3	5 6.5	mV mV
$\Delta V_{OS}/\Delta T$	Avg. TC of input offset voltage	R_S = 50Ω		5			5		µV/°C
$\Delta TC/\Delta V_{OS}$	Change in average TC[2] with V_{OS} adjust	R_S = 50Ω		0.5			0.5		µV/°C per mV
I_{OS}	Input offset current[1,3]	T_J = 25°C $T_J \leq T_{high}$		3	20 20		3	20 1	pA nA
I_B	Input bias current[1,3]	T_J = 25°C $T_J \leq T_{high}$		30	100 50		30	100 5	pA nA
R_{IN}	Input resistance	T_J = 25°C		10^{12}			10^{12}		Ω
A_{VOL}	Large signal voltage gain	V_S = ± 15V V_O = ± 10V, R_L = 2kΩ Over temp.	50 25	200		50 25	200		V/mV V/mV
V_O	Output voltage swing	V_S = ± 15V, R_L = 10kΩ V_S = ± 15V, R_L = 2kΩ	±12 ±10	±13 ±12		±12 ±10	±13 ±12		V V
V_{CM}	Input common mode Voltage range	V_S = ± 15V	±11	+15.1 -12		±11	+15.1 -12		V V V
CMRR	Common-mode rejection ratio		85	100		85	100		dB
PSRR	Supply volt. rej. ratio[4]		85	100		85	100		dB

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	LF355/6/7			UNIT
			Min	Typ	Max	
V_{OS}	*Input offset voltage*	$R_S = 50\Omega$		*3*	*10* 13	*mV* mV
$\Delta V_{OS}/\Delta T$	Avg. TC of input offset voltage	$R_S = 50\Omega$		5		$\mu V/°C$
$\Delta TC/\Delta V_{OS}$	Change in average TC[2] with V_{OS} adjust	$R_S = 50\Omega$		0.5		$\mu V/°C$ per mV
I_{OS}	Input offset current[1,3]	$T_J = 25°C$ $T_J \leq T_{high}$		3	50 2	pA nA
I_B	Input bias current[1,3]	$T_J = 25°C$ $T_J \leq T_{high}$		30	200 8	pA nA
R_{IN}	Input resistance	$T_J = 25°C$				Ω
A_{VOL}	Large signal voltage gain	$V_S = \pm 15V$ $V_O = \pm 10V, R_L = 2k\Omega$	25	10^{12} 200		V/mV
		Over temp.	*15*			V/mV
V_O	Output voltage swing	$V_S = \pm 15V, R_L = 10k\Omega$ $V_S = \pm 15V, R_L = 2k\Omega$	±12 ±10	±13 ±12		V V
V_{CM}	Input common mode Voltage range	$V_S = \pm 15V$	±10	+15.1 -12		V V V
CMRR	*Common-mode rejection ratio*		*80*	100		dB
PSRR	Supply volt. rej. ratio[4]		80	100		dB

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

PARAMETER	LF155A/355A LF155/255			LF355			LF156A/LF156/256			UNIT
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supply current		2	4		2	4		5	7	mA

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

PARAMETER	LF356A/LF356			LF157A/LF157/257			LF357A/LF357			UNIT
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supply current		5	10		5	7		5	10	mA

NOTES

1. These specifications apply for $\pm 15V \leq V_S \leq \pm 20V$, $-55°C \leq T_A \pm 125°C$ and $T_{HIGH} = +125°C$ unless otherwise stated for the LF155A/6A/7A and the LF155/6/7. For the LF255/6/7, these specifications apply for $\pm 15V \leq V_S \leq \pm 20V$, $-25°C \leq T_A \leq +85°C$ and $T_{HIGH} = 85°C$ unless otherwise stated. For the LF355A/6A/7A, these specifications apply for $\pm 15V \leq V_S \leq \pm 20V$, $0°C \leq T_A \leq +70°C$ and $T_{HIGH} = +70°C$, and for the LF355/6/7 these specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.
2. The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5μV/°C typically) for each mV of adjustment from its original unadjusted value. Common mode rejection and open loop voltage gain are also unaffected by offset adjustment.
3. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \theta_{jA}$ Pd where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
4. Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.[1]

PARAMETER	TEST CONDITIONS	LF155A/LF355A			LF156A/356A			LF157A/357A			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SR Slew rate	LF155/156 LF155A/6A: $A_V = 1$	3	5		10	12		40	50		V/μs
GBW Gain bandwidth product			2.5		4	4.5		15	20		MHz
t_S Settling time[5] to 0.01%			4			1.5			1.5		μs
e_n Equiv. input noise volt.	$R_S = 100\Omega$										
	f = 100Hz		25			15			15		nV/√Hz
	f = 1000Hz		20			12			12		nV/√Hz
i_n Equiv. input noise current	f = 100Hz		0.01			0.01			0.01		pA/√Hz
	f = 1000Hz		0.01			0.01			0.01		pA/√Hz
C_{IN} Input capacitance			3			3			3		pF

AC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.[1]

PARAMETER	TEST CONDITIONS	LF155/255/355			LF156/256			LF356			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SR Slew rate	LF155/156 LF155A/6A: $A_V = 1$,		5		7.5	12			12		V/μs
GBW Gain bandwidth product			2.5			5			5		MHz
t_S Settling time[5] to 0.01%			4			1.5			1.5		μs
e_n Equiv. input noise volt.	$R_S = 100\Omega$										
	f = 100Hz		25			15			15		nV/√Hz
	f = 1000Hz		20			12			12		nV/√Hz
i_n Equiv. input noise current	f = 100Hz		0.01			0.01			0.01		pA/√Hz
	f = 1000Hz		0.01			0.01			0.01		pA/√Hz
C_{IN} Input capacitance			3			3			3		pF

AC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.[1]

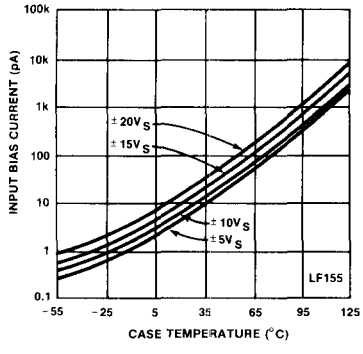
PARAMETER		TEST CONDITIONS	LF157/257			LF357			UNIT
			Min	Typ	Max	Min	Typ	Max	
SR	Slew rate	LF157A/LF157: $A_V = 5$	30	50			50		V/μs
GBW	Gain bandwidth product			20			20		MHz
t_S	Settling time[5] to 0.01%			1.5			1.5		μs
e_n	Equiv. input noise volt.	$R_S = 100\Omega$							
		f = 100Hz		15			15		nV/√Hz
		f = 1000Hz		12			12		nV/√Hz
i_n	Equiv. input noise current	f = 100Hz		0.01			0.01		pA/√Hz
		f = 1000Hz		0.01			0.01		pA/√Hz
C_{IN}	Input capacitance			3			3		pF

NOTE

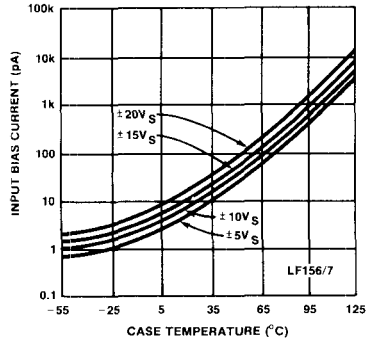
5. Settling time is defined here, for a unity gain inverter connection using 2kΩ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157, $A_V = -5$, the feedback resistor from output to input is 2kΩ and the output step is 10V (See Settling Time Test Circuit).

TYPICAL DC PERFORMANCE CHARACTERISTICS (curves are for LF155, LF156 and LF157 unless otherwise specified.)

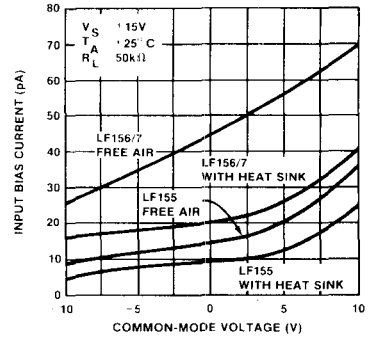
INPUT BIAS CURRENT



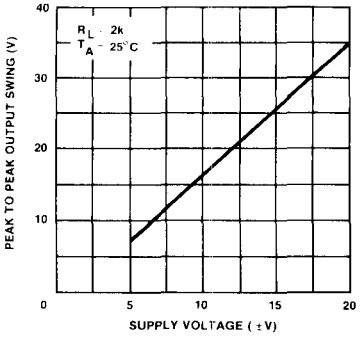
INPUT BIAS CURRENT



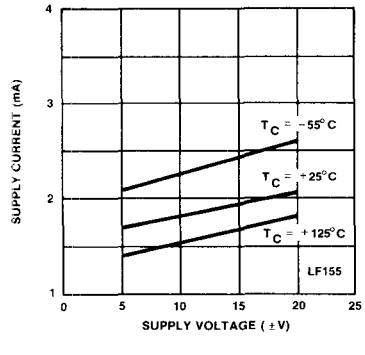
INPUT BIAS CURRENT



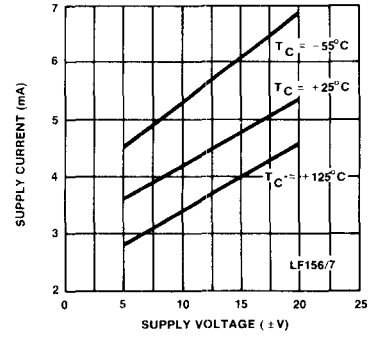
VOLTAGE SWING



SUPPLY CURRENT

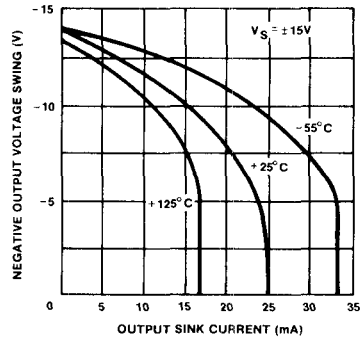


SUPPLY CURRENT

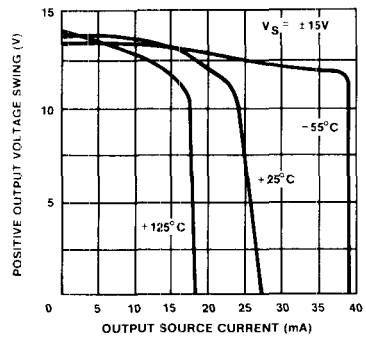


TYPICAL DC PERFORMANCE CHARACTERISTICS (Cont'd)

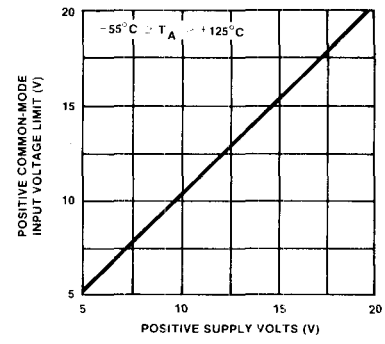
NEGATIVE CURRENT LIMIT



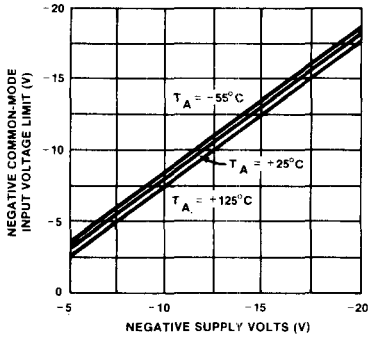
POSITIVE CURRENT LIMIT



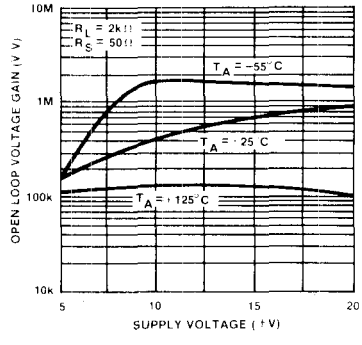
POSITIVE COMMON-MODE INPUT VOLTAGE LIMIT



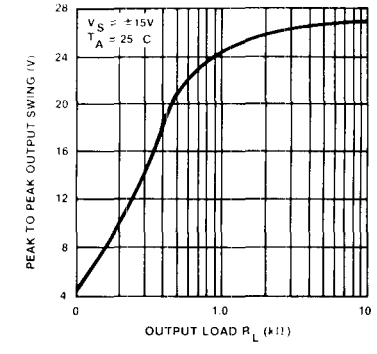
NEGATIVE COMMON-MODE INPUT VOLTAGE LIMIT



OPEN LOOP VOLTAGE GAIN

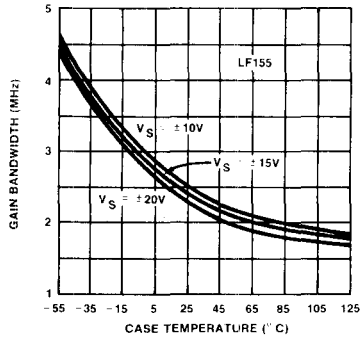


OUTPUT VOLTAGE SWING

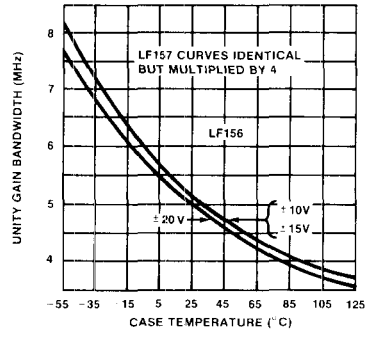


TYPICAL AC PERFORMANCE CHARACTERISTICS

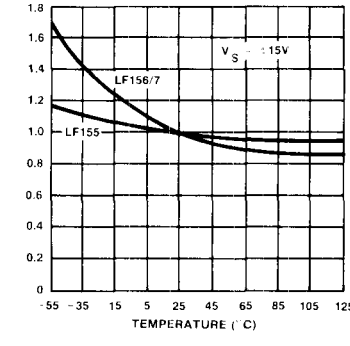
GAIN BANDWIDTH



UNITY GAIN BANDWIDTH

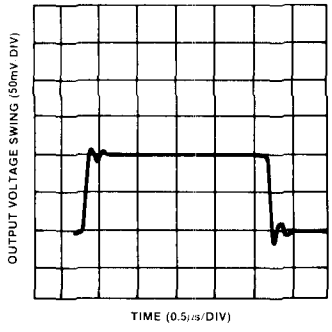


NORMALIZED SLEW RATE

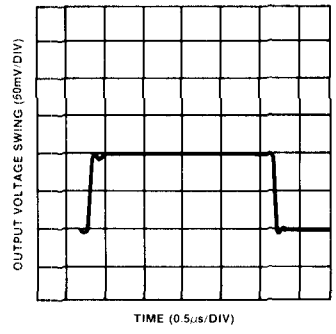


TYPICAL AC PERFORMANCE CHARACTERISTICS (Cont'd)

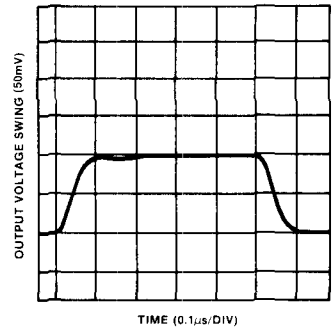
LF155 SMALL SIGNAL PULSE RESPONSE, $A_V = +1$



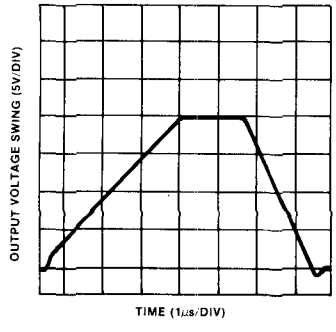
LF156 SMALL SIGNAL PULSE RESPONSE, $A_V = +1$



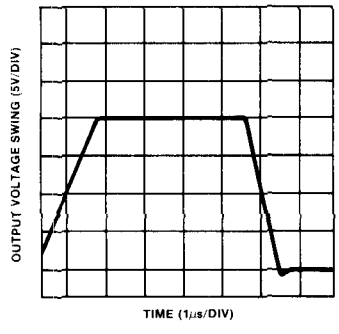
LF157 SMALL SIGNAL PULSE RESPONSE, $A_V = +5$



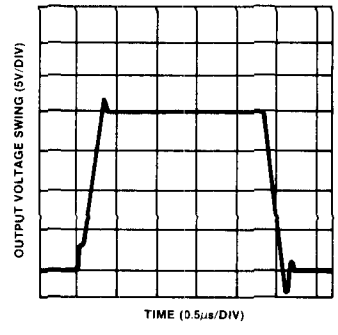
LF155 LARGE SIGNAL PULSE RESPONSE, $A_V = +1$



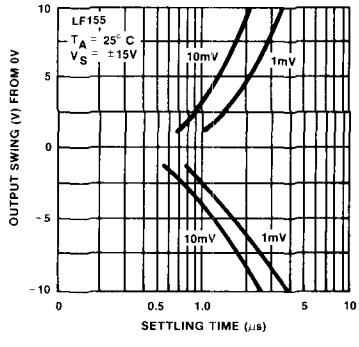
LF156 LARGE SIGNAL PULSE RESPONSE, $A_V = +1$



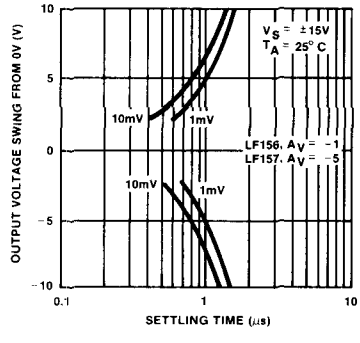
LF157 LARGE SIGNAL PULSE RESPONSE, $A_V = +5$



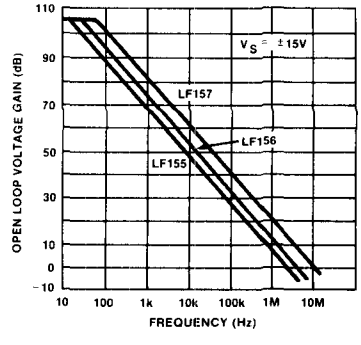
INVERTER SETTLING TIME



INVERTER SETTLING TIME

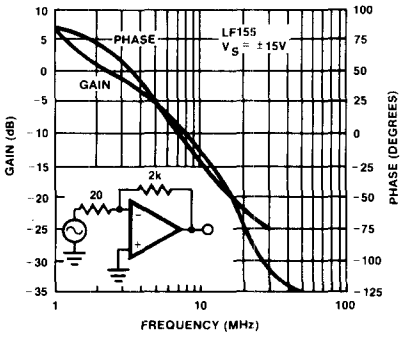


OPEN LOOP FREQUENCY RESPONSE

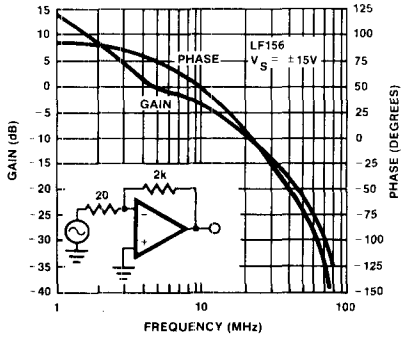


TYPICAL AC PERFORMANCE CHARACTERISTICS (Cont'd)

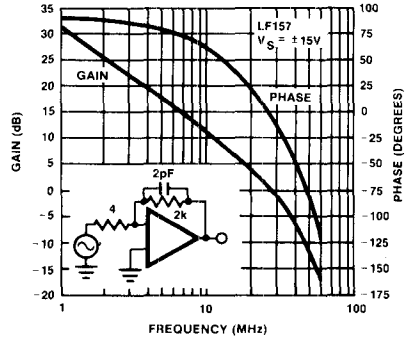
BODE PLOT



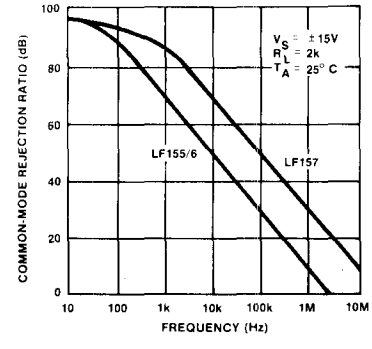
BODE PLOT



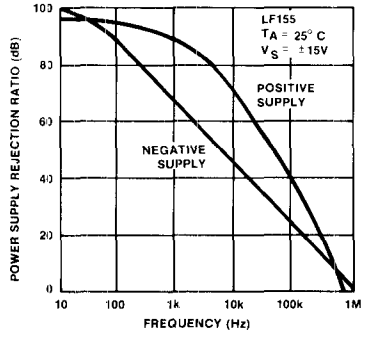
BODE PLOT



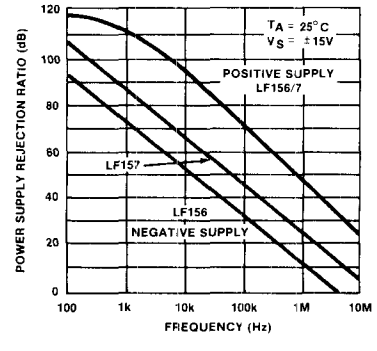
COMMON-MODE REJECTION RATIO



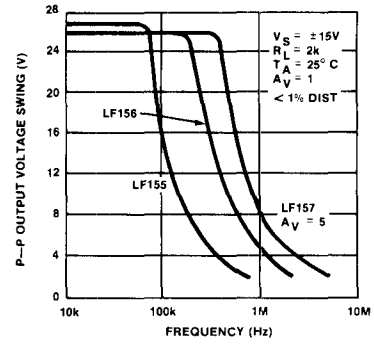
POWER SUPPLY REJECTION RATIO



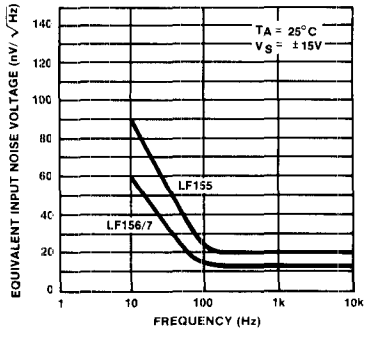
POWER SUPPLY REJECTION RATIO



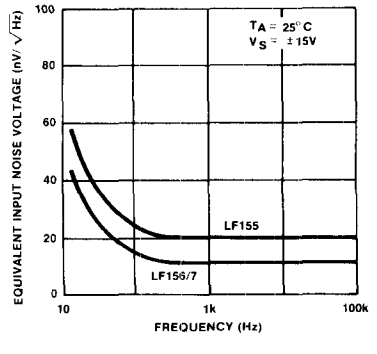
UNDISTORTED OUTPUT VOLTAGE SWING



EQUIVALENT INPUT NOISE VOLTAGE

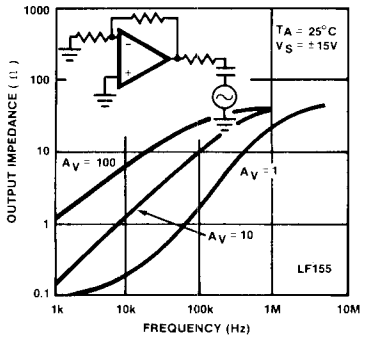


EQUIVALENT INPUT NOISE VOLTAGE (EXPANDED SCALE)

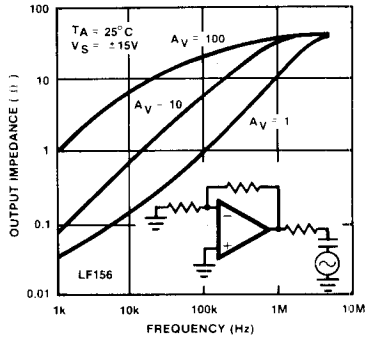


TYPICAL AC PERFORMANCE CHARACTERISTICS (Cont'd)

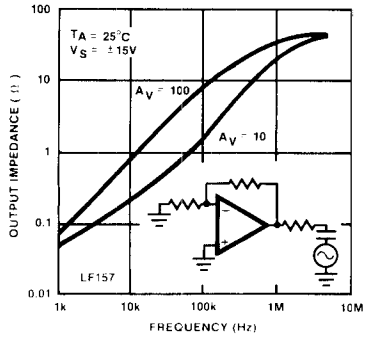
OUTPUT IMPEDANCE



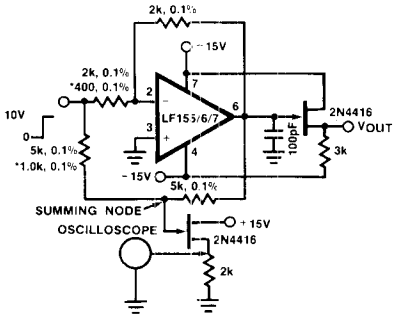
OUTPUT IMPEDANCE



OUTPUT IMPEDANCE



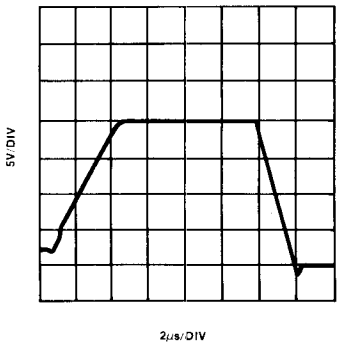
SETTLING TIME TEST CIRCUIT



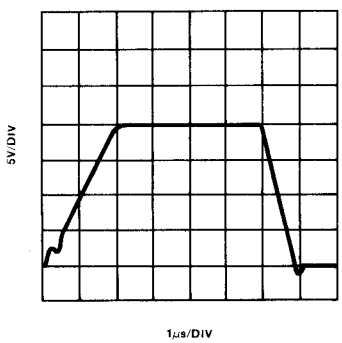
- Settling time is tested with the LF155/6 connected as unity gain inverter and LF157 connected for $A_V = -5$
- FET used to isolate the probe capacitance
- Output = 10V step
- $A_V = -5$ for LF157

LARGE SIGNAL INVERTER OUTPUT, V_{OUT} (FROM SETTLING TIME CIRCUIT)

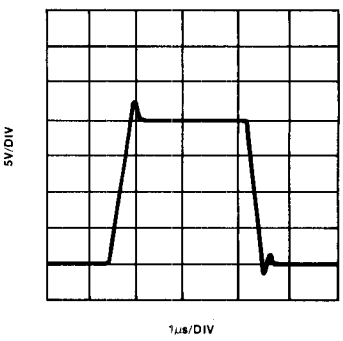
LF155



LF156



LF157



APPLICATION HINTS

The LF155/6/7 series are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

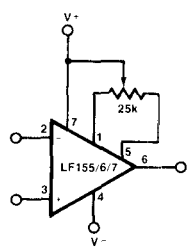
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

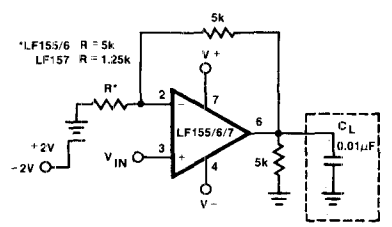
TYPICAL CIRCUIT CONNECTIONS

V_{OS} ADJUSTMENT



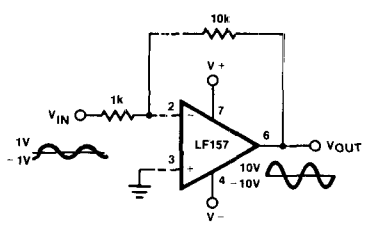
- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V+
- For potentiometers with temperature coefficient of 100ppm/°C or less the additional drift with adjust is ≈ 0.5μV/°C/mV of adjustment
- Typical overall drift: 5μV/°C ± (0.5μV/°C/mV of adj.)

DRIVING CAPACITIVE LOADS



Due to a unique output stage design these amplifiers have the ability to drive large capacitive loads and still maintain stability. C_L max ≤ 0.01μF.
Overshoot ≤ 20%
Setting time (t_S) ≥ 5μs

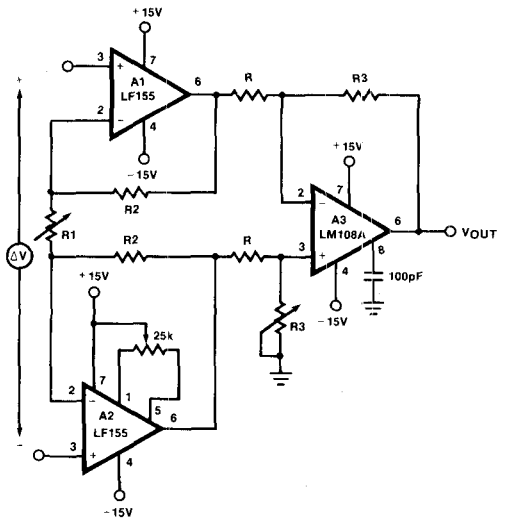
LF157. A LARGE POWER BW AMPLIFIER



For distortion < 1% and a 20V p-p V_{OUT} swing power bandwidth is: 500kHz.

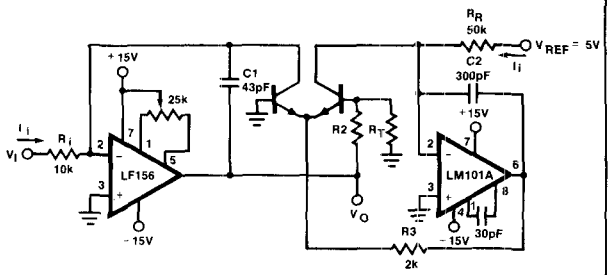
TYPICAL APPLICATIONS

HIGH IMPEDANCE, LOW DRIFT INSTRUMENTATION AMPLIFIER



- $V_{OUT} = \frac{R3}{R}\left[\frac{2R2}{R1} + 1\right]\Delta V$, V- +2V ≤ V_{IN} Common-Mode ≤ V+
- System V_{OS} adjusted via A2 V_{OS} adjust
- Trim R3 to boost up CMRR to 120dB.

FAST LOGARITHMIC CONVERTER

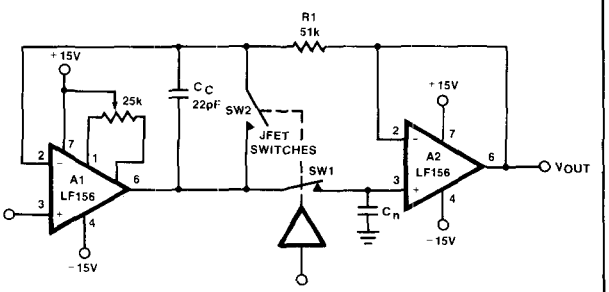


$$|V_{OUT}| = \left[1 + \frac{R2}{R_T}\right]\frac{kT}{q} \ln V_I\left[\frac{R_r}{V_{REF}\, R_i}\right] = \log V_I \frac{1}{R_i\, I_R}$$

R2 = 15.71, R_T = 1k, 0.3%°C (for temperature compensation)

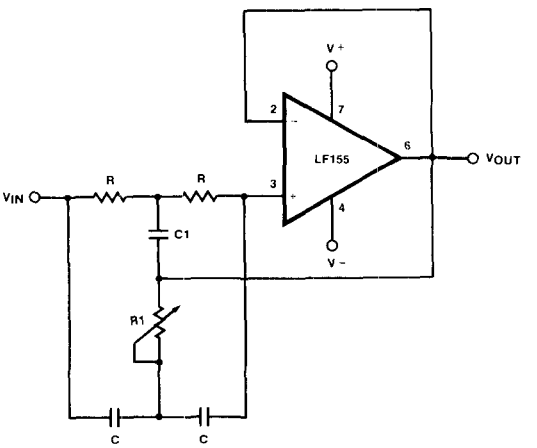
- Dynamic range: 100μA ≤ I_i ≤ 1mA (5 decades, |V_O| = 1V/decades)
- *Transient response: 3μs for Δ, = decades*
- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF156 to minimize quiescent error
- R_T: Tel Labs type Q81 + 0.3%/°C.

HIGH ACCURACY SAMPLE AND HOLD



- By closing the loop through A2 the V_{OUT} accuracy will be determined uniquely by A1. No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added on propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold.
- R1, C_C: additional compensation
- Use LF156 for
  - Δ Fast settling time
  - Δ Low V_{OS}

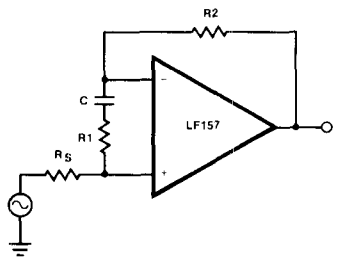
HIGH Q NOTCH FILTER



- 2R1 = R = 10MΩ
  2C = C1 = 300pF
- Capacitors should be matched to obtain high Q
- f_{NOTCH} = 120Hz, notch = 55dB, Q > 180
- *Use LF155 for*
  - Δ Low I_B
  - Δ Low supply current

TYPICAL APPLICATIONS (Cont'd)

NON-INVERTING UNITY GAIN OPERATION FOR LF157

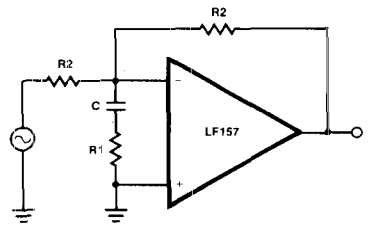


$$R1C1 \geq \frac{1}{(2\pi)\,(5MHz)}$$

$$R1 = \frac{R2 + R5}{4}$$

$A_{V(DC)} = -1$
f-3dB ≈ 5MHz

INVERTING UNITY GAIN FOR LF157

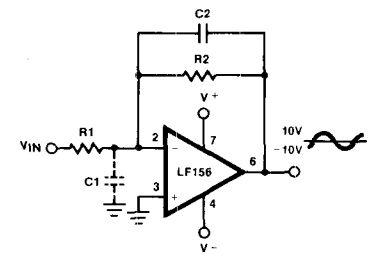


$$R1C1 \geq \frac{1}{(2\pi)\,(5MHz)}$$

$$R1 = \frac{R2}{4}$$

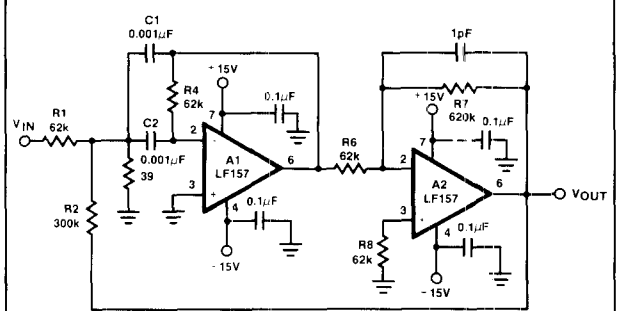
$A_{VI(DC)} = -1$
f-3dB ≈ 5MHz

WIDE BW LOW NOISE, LOW DRIFT AMPLIFIER



- Power BW: $f_{MAX} = \frac{S_r}{2\pi/p} \cong 240kHz$
- Parasitic input capacitance C1 ≅ 3pF for LF155, LF156, and LF157 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2C2 ≅ R1C1.

HIGH Q BAND PASS FILTER



- By adding positive feedback (R2) Q increases to 40
- f_{BP} = 100kHz

$$\frac{V_{OUT}}{V_{IN}} = 10\sqrt{Q}$$

- Clean layout recommended
- Response to a 1V p-p tone burst: 300μs