

Automotive-grade P-channel -40 V, 12 mΩ typ., -50 A STripFET™ F6 Power MOSFET in a DPAK package

Datasheet - production data

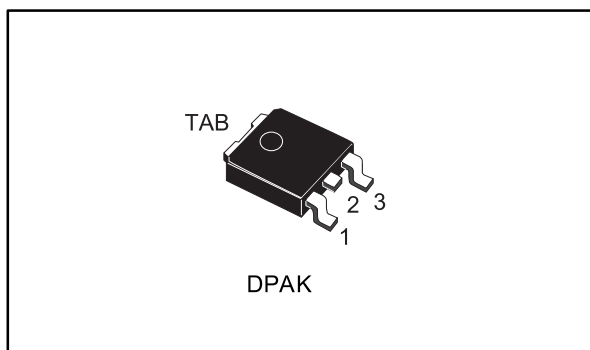
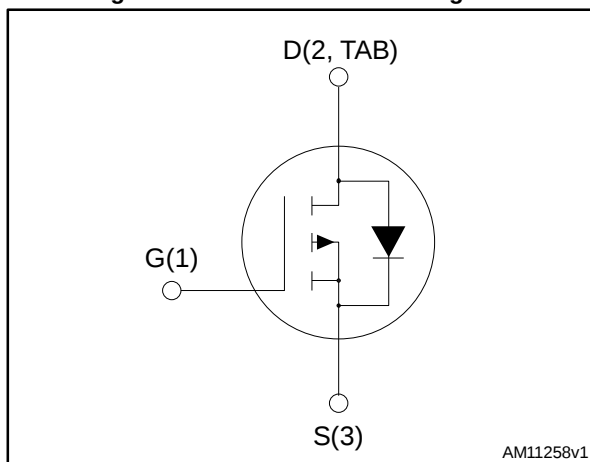


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STD45P4LLF6AG	-40 V	15 mΩ	-50 A

- Designed for automotive applications and AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET™ F6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low R_{DS(on)} in all packages.

Table 1: Device summary

Order code	Marking	Package	Packing
STD45P4LLF6AG	45P4LLF6	DPAK	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	-40	V
V_{GS}	Gate-source voltage	± 18 V	V
I_D	Drain current (continuous) at $T_{case} = 25\text{ }^{\circ}\text{C}$	-50	A
	Drain current (continuous) at $T_{case} = 100\text{ }^{\circ}\text{C}$	-31	
$I_{DM}^{(1)}$	Drain current (pulsed)	-200	A
P_{TOT}	Total dissipation at $T_{case} = 25\text{ }^{\circ}\text{C}$	58	W
$E_{AS}^{(2)}$	Single pulse avalanche energy	160	mJ
T_{stg}	Storage temperature	-55 to 150	$^{\circ}\text{C}$
$T_J^{(3)}$	Operating junction temperature		

Notes:

⁽¹⁾ Pulse width is limited by safe operating area.

⁽²⁾ starting $T_J = 25\text{ }^{\circ}\text{C}$, $R_G = 47\text{ }\Omega$, $I_{D(min)} = -25\text{ A}$.

⁽³⁾ HTRB performed at $T_J = 175\text{ }^{\circ}\text{C}$, $V_{DS} = 100\% V_{(BR)DSS}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.14	$^{\circ}\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	50	

2 Electrical characteristics

($T_{\text{case}} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = -250\text{ }\mu\text{A}$	-40			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = -40\text{ V}$			-1	μA
		$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = -40\text{ V}$, $T_{\text{case}} = 125\text{ }^{\circ}\text{C}$			-10	
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = -18\text{ V}$			-100	nA
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = -250\text{ }\mu\text{A}$	-1		-2.5	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = -10\text{ V}$, $I_{\text{D}} = -25\text{ A}$		12	15	m Ω
		$V_{\text{GS}} = -4.5\text{ V}$, $I_{\text{D}} = -25\text{ A}$		17	20	

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{\text{DS}} = -25\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$	-	3525	-	pF
C_{oss}	Output capacitance		-	345	-	
C_{rss}	Reverse transfer capacitance		-	240	-	
Q_{g}	Total gate charge	$V_{\text{DD}} = -20\text{ V}$, $I_{\text{D}} = -50\text{ A}$, $V_{\text{GS}} = -10\text{ V}$ (see Figure 14: "Gate charge test circuit")	-	65.5	-	nC
Q_{gs}	Gate-source charge		-	11.5	-	
Q_{gd}	Gate-drain charge		-	13	-	

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = -20\text{ V}$, $I_{\text{D}} = -25\text{ A}$ $R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = -10\text{ V}$ (see Figure 13: "Switching times test circuit for resistive load")	-	12	-	ns
t_{r}	Rise time		-	35.5	-	
$t_{\text{d(off)}}$	Turn-off delay time		-	63.5	-	
t_{f}	Fall time		-	31	-	

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		-50	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		-200	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = -50\text{ A}$	-		-1.3	V
t_{rr}	Reverse recovery time	$I_{SD} = -50\text{ A}$, $di/dt = -100\text{ A}/\mu\text{s}$, $V_{DD} = -32\text{ V}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	27.5		ns
Q_{rr}	Reverse recovery charge		-	24.5		nC
I_{RRM}	Reverse recovery current		-	-1.8		A

Notes:

(1) Pulse width is limited by safe operating area.

(2) Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

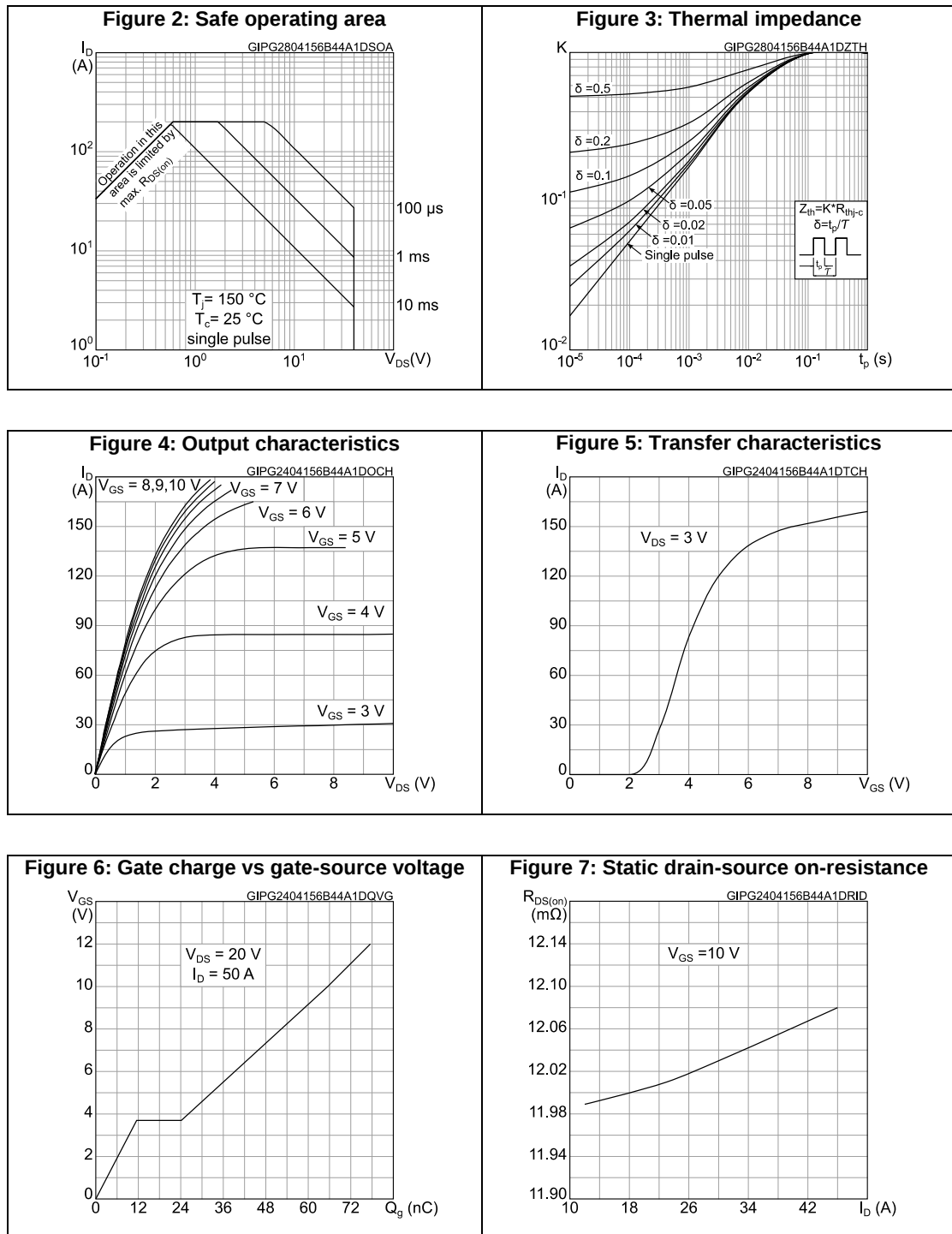


Figure 8: Capacitance variations

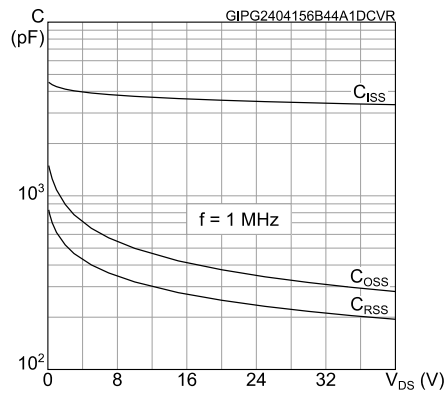


Figure 9: Normalized gate threshold voltage vs temperature

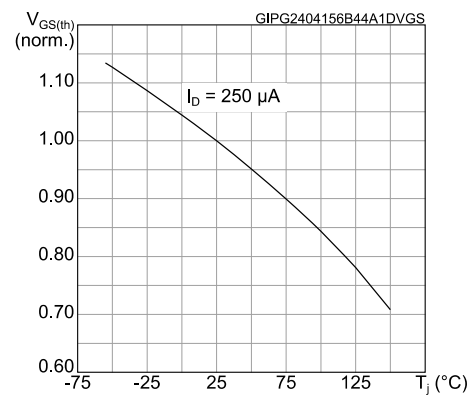


Figure 10: Normalized on-resistance vs temperature

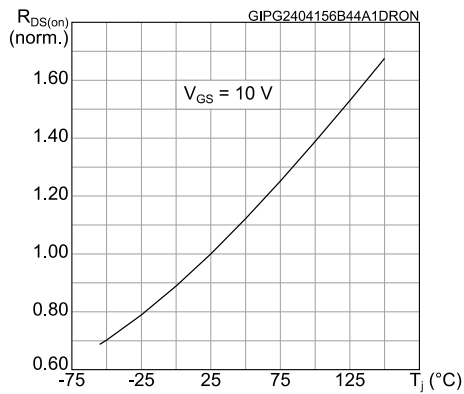


Figure 11: Normalized V(BR)DSS vs temperature

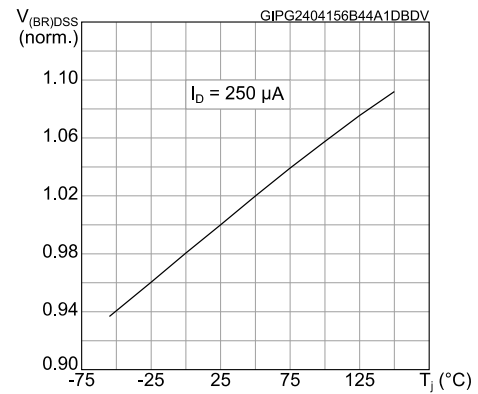
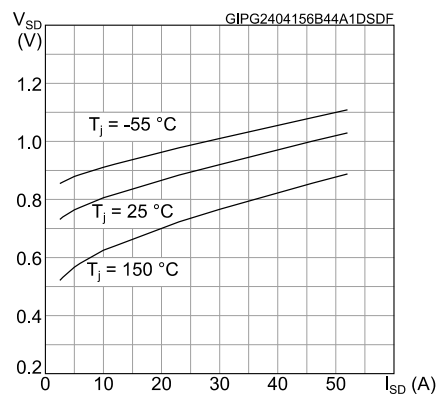


Figure 12: Source-drain diode forward characteristics



For the P-channel Power MOSFET, current and voltage polarities are reversed.

3 Test circuits

Figure 13: Switching times test circuit for resistive load

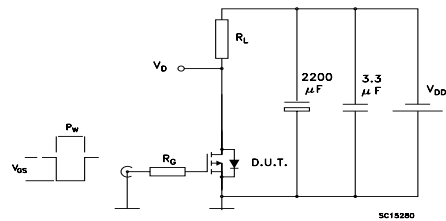


Figure 14: Gate charge test circuit

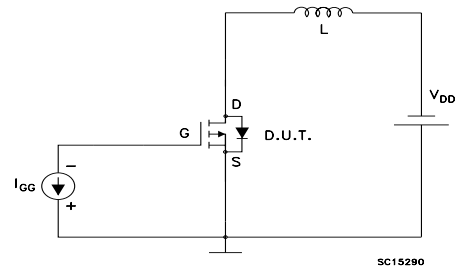
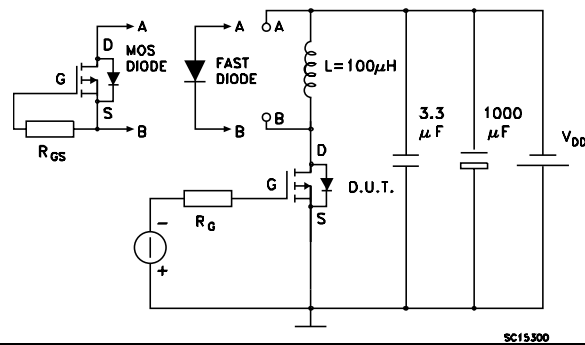


Figure 15: Test circuit for inductive load switching and diode recovery times

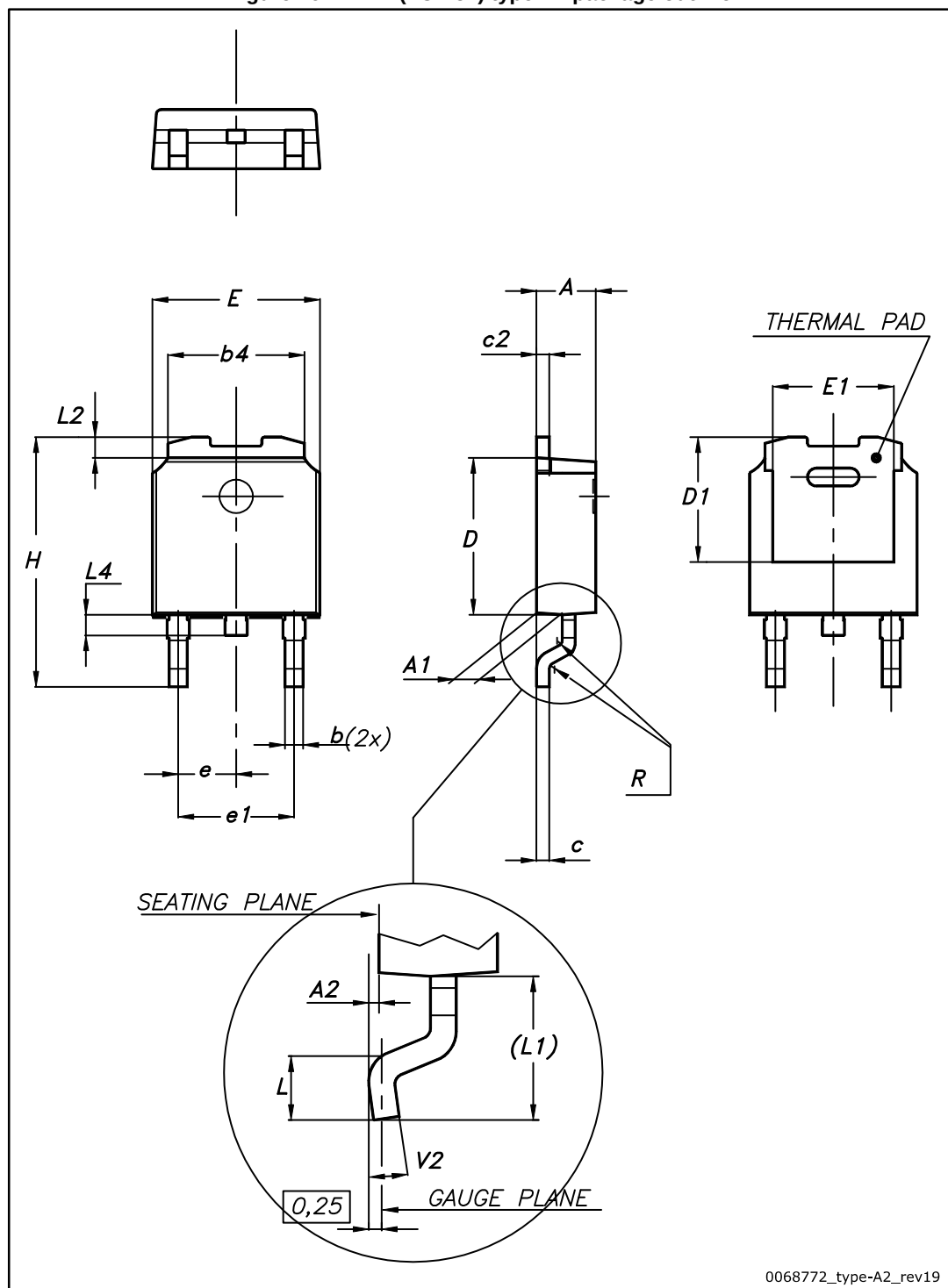


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 16: DPAK (TO-252) type A2 package outline

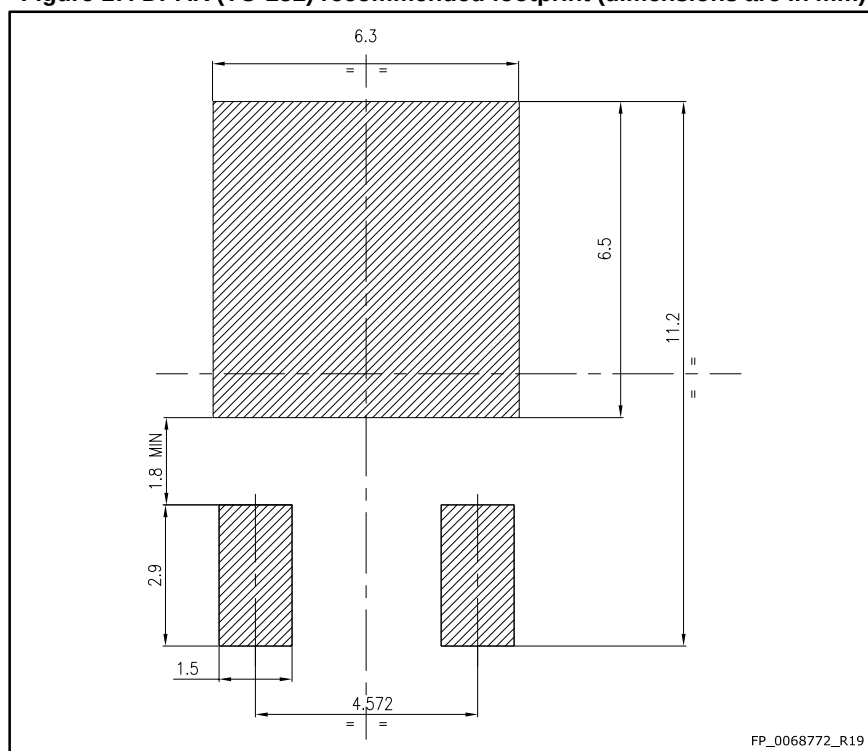


0068772_type-A2_rev19

Table 8: DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 17: DPAK (TO-252) recommended footprint (dimensions are in mm)



4.2 DPAK (TO-252) packing information

Figure 18: DPAK (TO-252) tape outline

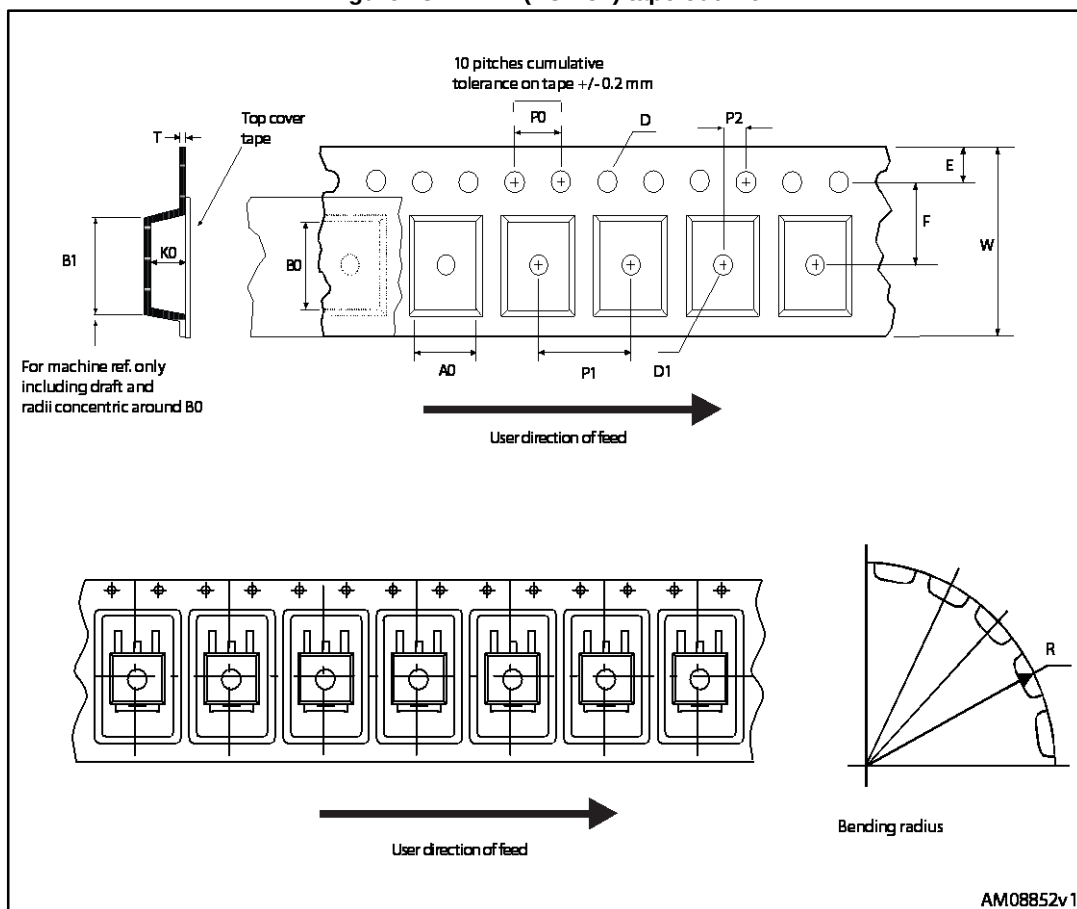


Figure 19: DPAK (TO-252) reel outline

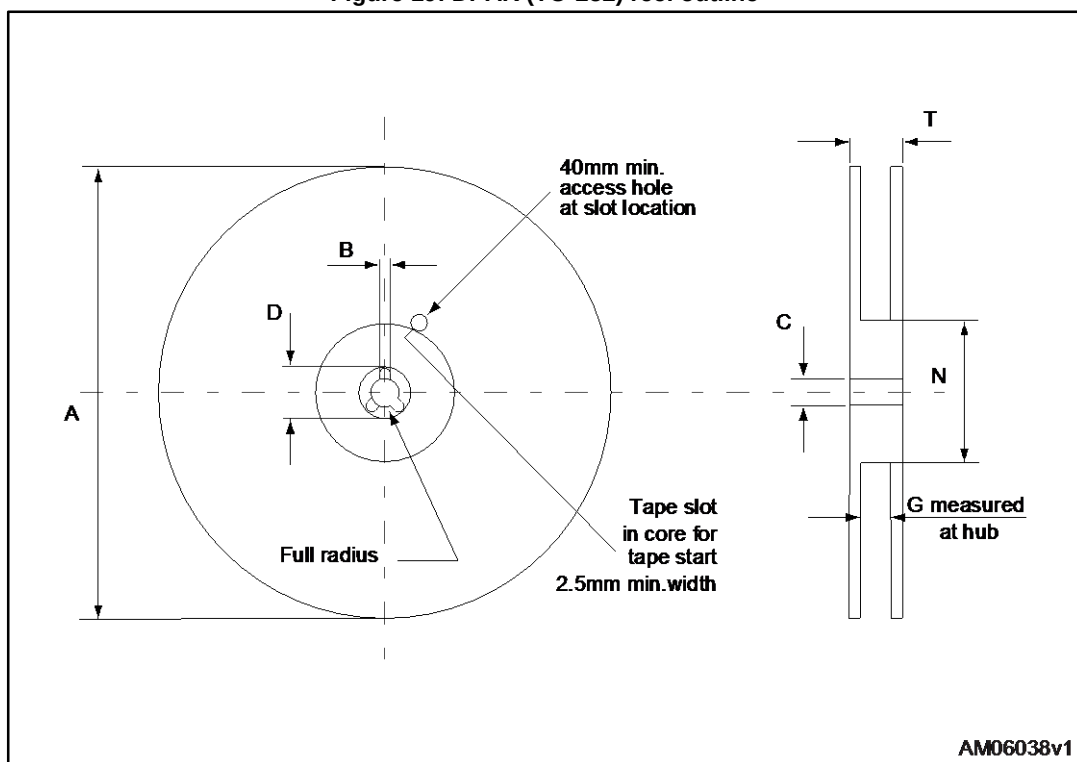


Table 9: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
28-Apr-2015	1	First release.
22-Jul-2015	2	Modified: V_{GS} values in absolute maximum ratings table and static table. Updated: DPAK (TO-252) type A2 package information section updated. Minor text changes.

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