



MIC94030/94031

TinyFET® P-Channel MOSFET

General Description

The MIC94030 and MIC94031 are 4-terminal silicon gate P-channel MOSFETs that provide low on-resistance in a very small package.

Designed for high-side switch applications where space is critical, the MIC94030/1 exhibits an on-resistance of typically 0.75Ω at 4.5V gate-to-source voltage. The MIC94030/1 also operates with only 2.7V gate-to-source voltage.

The MIC94030 is the basic 4-lead P-channel MOSFET. The MIC94031 is a variation that includes an internal gate pull-up resistor that can reduce the system parts count in many applications.

The 4-terminal SOT-143 package permits a substrate connection separate from the source connection. This 4-terminal configuration improves the θ_{JA} (improved heat dissipation) and makes analog switch applications practical.

The small size, low threshold, and low $R_{DS(on)}$ make the MIC94030/1 the ideal choice for PCMCIA card sleep mode or distributed power management applications.

Features

- 13.5V minimum drain-to-source breakdown
- 0.75Ω typical on-resistance
 - at 4.5V gate-to-source voltage
- 0.45Ω typical on-resistance
 - at 10V gate-to-source voltage
- Operates with 2.7V gate-to-source voltage
- Separate substrate connection for added control
- Industry's smallest surface mount package

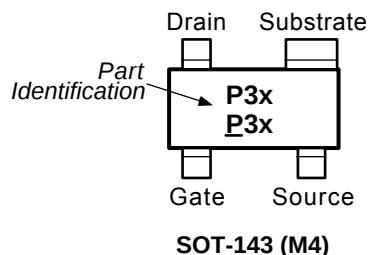
Applications

- Distributed power management
- PCMCIA card power management
- Battery-powered computers, peripherals
- Hand-held bar-code scanners
- Portable communications equipment

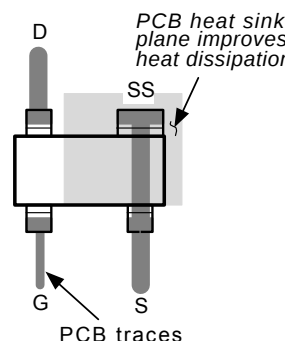
Ordering Information

Part Number				Junction Temp. Range	Package
Standard	Marking	Pb-Free	Marking		
MIC94030BM4	P30	MIC94030YM4	<u>P</u> 30	-55° to +150°C	SOT-143
MIC94031BM4	P31	MIC94031YM4	<u>P</u> 31	-55° to +150°C	SOT-143

Pin Configuration



Typical PCB Layout



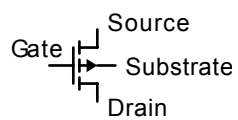
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July 2006

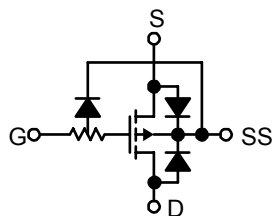
M9999-071106

Schematic Symbol

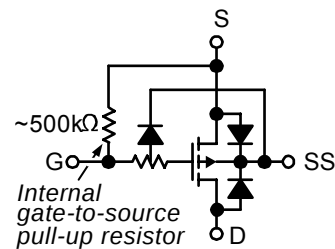


Schematic Symbol

Functional Diagrams



MIC94030



MIC94031

Absolute Maximum Ratings⁽¹⁾

Voltage and current values are negative. Signs not shown for clarity.

Drain-to-Source Voltage (pulse).....	16V
Gate-to-Source Voltage (pulse).....	16V
Continuous Drain Current	
$T_A = 25^\circ\text{C}$	1A
$T_A = 100^\circ\text{C}$	0.5A
Operating Junction Temperature	-55°C to $+150^\circ\text{C}$
Storage Temperature	-55°C to $+150^\circ\text{C}$

Total Power Dissipation

$T_A = 25^\circ\text{C}$	568mW
$T_A = 100^\circ\text{C}$	227mW

Thermal Resistance

θ_{JA}	220°C/W
θ_{JC}	130°C/W

Lead Temperature

1/16" from case, 10s.....	$+300^\circ\text{C}$
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Electrical Characteristics

Voltage and current values are negative. Signs not shown for clarity.

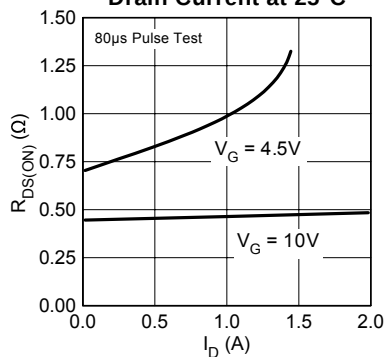
Symbol	Parameter	Condition (Note 1)	Min	Typ	Max	Units
V_{BDSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	13.5			V
V_{GS}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.6	1.0	1.4	V
I_{GSS}	Gate-Body Leakage	$V_{DS} = 0V, V_{GS} = 12V$, Note 2, Note 3			1	μA
R_{GS}	Gate-Source Resistor	$V_{DS} = 0V, V_{GS} = 12V$, Note 2, Note 4	500	750	1000	k Ω
C_{ISS}	Input Capacitance	$V_{GS} = 0V, V_{DS} = 12V$		100		pF
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 12V, V_{GS} = 0V$			25	μA
		$V_{DS} = 12V, V_{GS} = 0V, T_J = 125^\circ\text{C}$		0.010	250	μA
$I_{D(ON)}$	On-State Drain Current	$V_{DS} = 10V, V_{GS} = 10V$, Note 5		6.3		A
$R_{DS(ON)}$	Drain-Source On-State Resist	$V_{GS} = 10V, I_D = 100mA$ $V_{GS} = 4.5V, I_D = 100mA$ $V_{GS} = 2.7V, I_D = 100mA$		0.45 0.75 1.20	1.00	Ω Ω Ω
g_{FS}	Forward Transconductance	$V_{DS} = 10V, I_D = 200mA$, Note 5		480		mS

Notes:

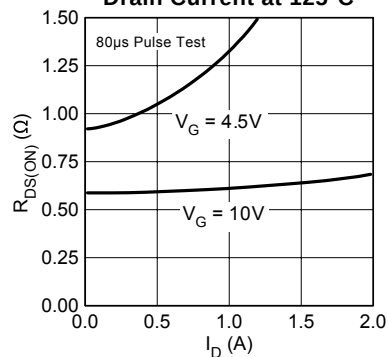
1. $T_A = 25^\circ\text{C}$ unless noted. Substrate connected to source for all conditions.
2. ESD gate protection diode conducts during positive gate-to-source voltage excursions.
3. MIC94030 only.
4. MIC94031 only.
5. Pulse Test: Pulse Width $\leq 80\mu\text{sec}$, Duty Cycle $\leq 0.5\%$.

Typical Characteristics

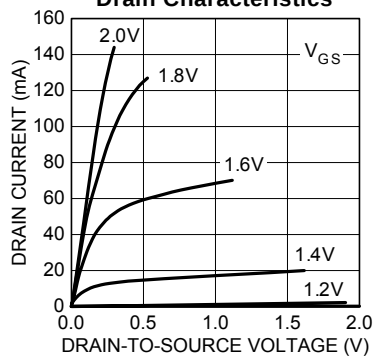
On Resistance vs.
Drain Current at 25°C



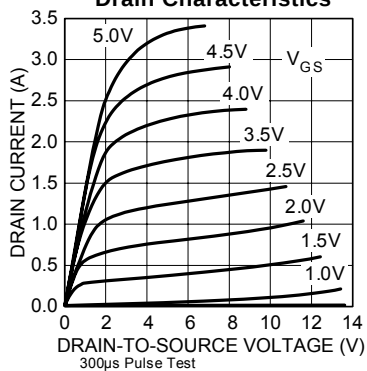
On Resistance vs.
Drain Current at 125°C



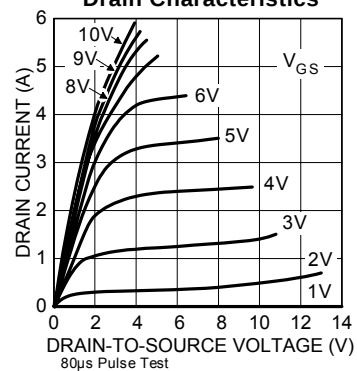
Drain Characteristics



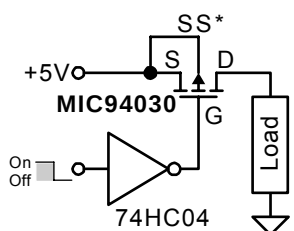
Drain Characteristics



Drain Characteristics

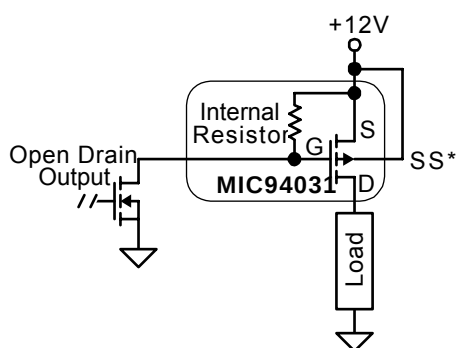


Typical Applications



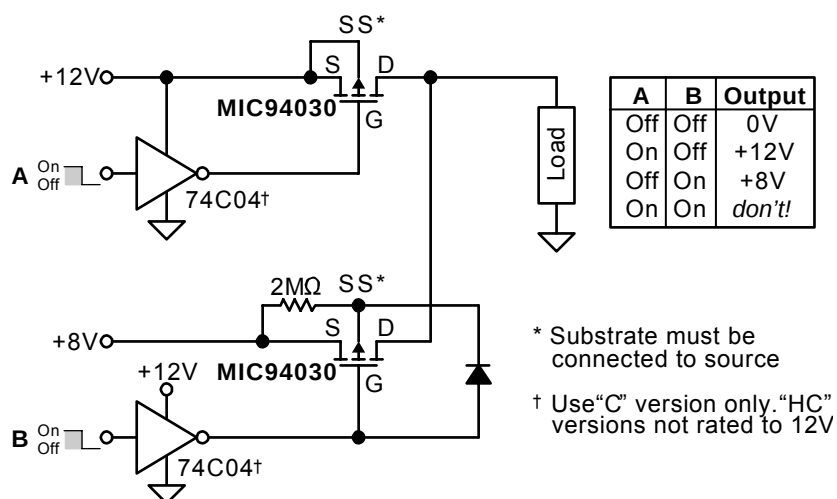
* Substrate must be connected to source

Figure 1. Power Switch Application



* Substrate must be connected to source

Figure 2. Power Control Application

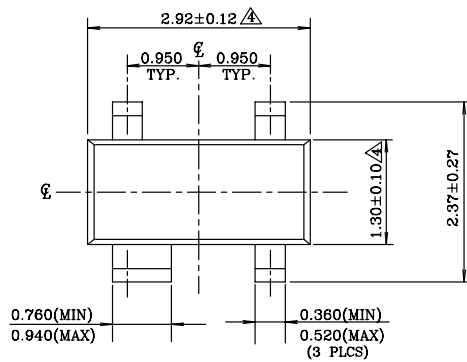


* Substrate must be connected to source

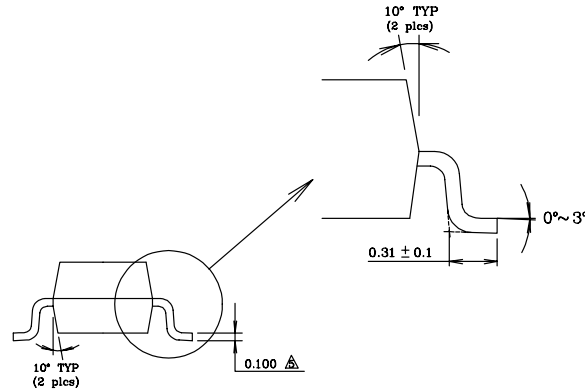
† Use "C" version only. "HC" versions not rated to 12V

Figure 3. Analog Switch Application

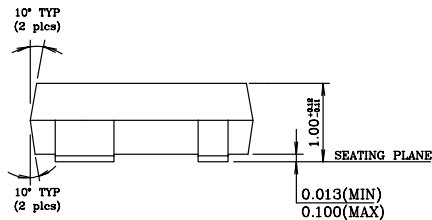
Package Information



TOP VIEW



END VIEW



SIDE VIEW

NOTE:

1. Dimensions and tolerances are as per ANSI Y14.5M, 1982.
2. Package surface to be mirror finish.
3. Die is facing up for mold & trim/form.
- △4 Dimension are exclusive of mold flash and gate burr.
- △5 Dimension are exclusive of solder plating.

SOT-143 (M4)

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