

74LVT245B

3.3 V octal transceiver with direction pin; 3-state

Rev. 3 — 30 July 2021

Product data sheet

1. General description

The 74LVT245B is an 8-bit transceiver with 3-state outputs. The device features an output enable ($\overline{OE}$) and send/receive (DIR) for direction control. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Bus hold data inputs eliminate the need for external pull-up resistors to define unused inputs

2. Features and benefits

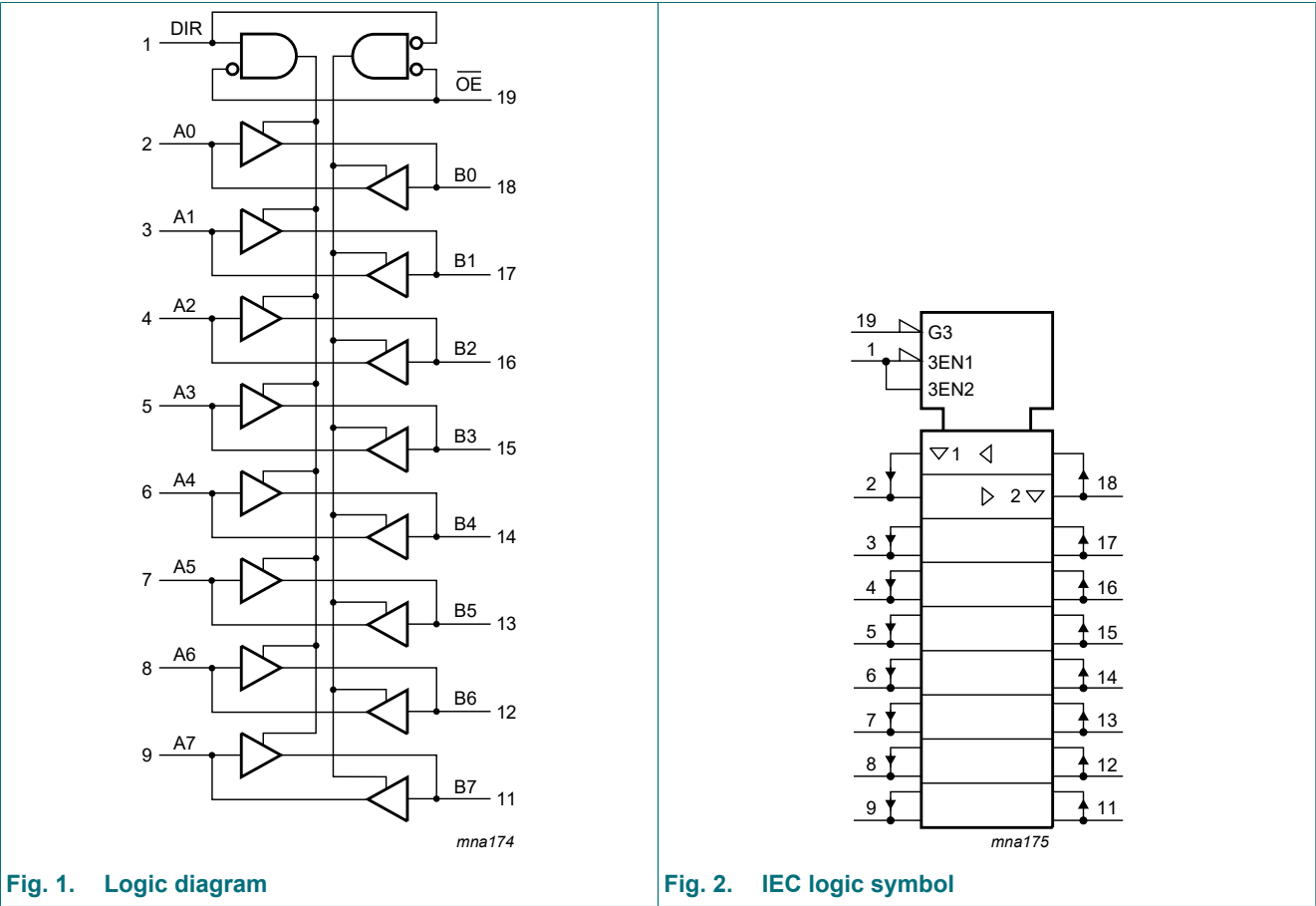
- Wide supply voltage range from 2.7 to 3.6 V
- 3-state buffers
- Octal bidirectional bus interface
- Overvoltage tolerant inputs to 5.5 V
- Direct interface with TTL levels
- BiCMOS high speed and output drive
- Output capability: +64 mA/-32 mA
- Latch-up protection exceeds 500 mA per JEDEC Std 17
- Bus-hold data inputs eliminate the need for external pull-up resistors for unused inputs
- No bus current loading when output is tied to 5 V bus
- Live insertion/extraction permitted
- Power-up 3-state
- I_{OFF} circuitry provides partial Power-down mode operation
- Complies with JEDEC standard JESD8C (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114E exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to 85 °C

3. Ordering information

Table 1. Ordering information

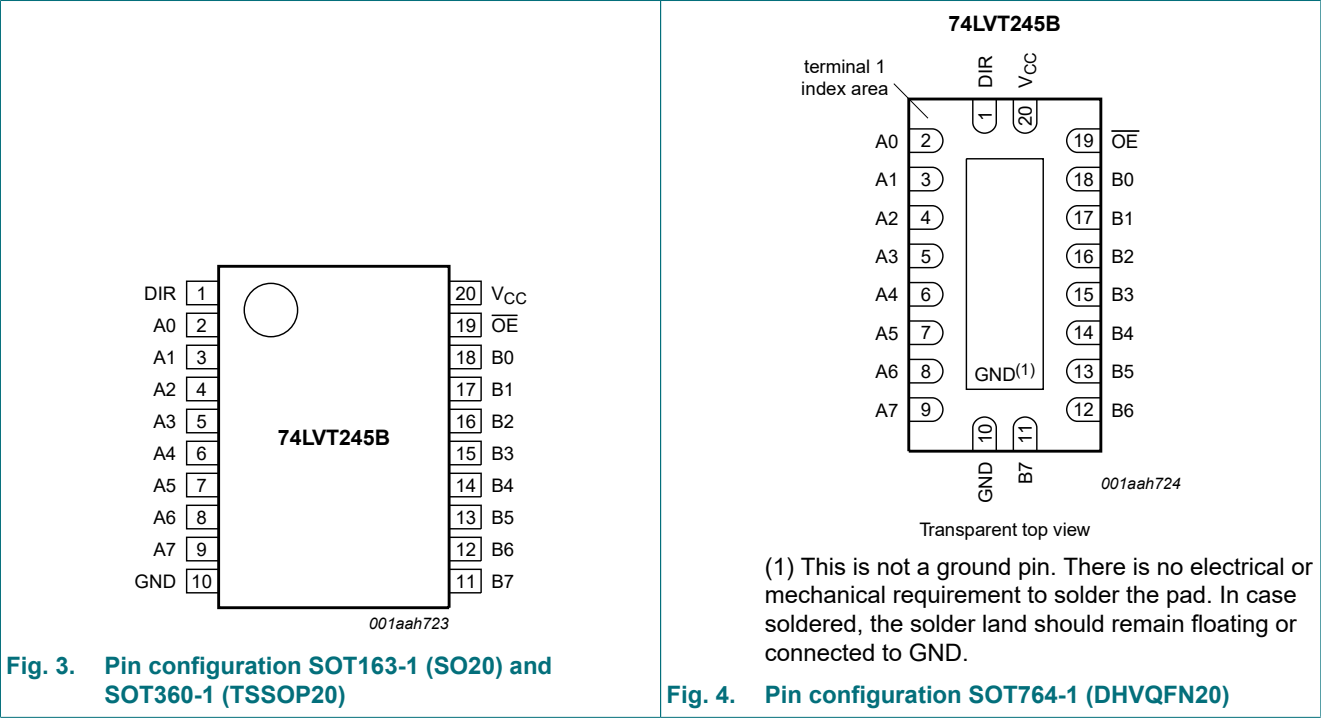
Type number	Package			
	Temperature range	Name	Description	Version
74LVT245BD	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVT245BPW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74LVT245BBQ	-40 °C to +85 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
DIR	1	direction control
A0, A1, A2, A3, A4, A5, A6, A7	2, 3, 4, 5, 6, 7, 8, 9	data input/output
GND	10	ground (0 V)
B0, B1, B2, B3, B4, B5, B6, B7	18, 17, 16, 15, 14, 13, 12, 11	data input/output
OE	19	output enable input (active LOW)
V _{CC}	20	supply voltage

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high impedance OFF-state.

Inputs		Inputs/outputs	
OE	DIR	An	Bn
L	L	An = Bn	inputs
L	H	inputs	Bn = An
H	X	Z	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage	[1]	-0.5	+7.0	V
V_O	output voltage	output in OFF or HIGH state [1]	-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < 0$	-50	-	mA
I_{OK}	output clamping current	$V_O < 0$	-50	-	mA
I_O	output current	output in LOW state	-	128	mA
		output in HIGH state	-64	-	mA
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature	[2]	-	150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C to }+85\text{ °C}$	-	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		2.7	3.6	V
V_I	input voltage		0	5.5	V
I_{OH}	HIGH-level output current		-	-32	mA
I_{OL}	LOW-level output current		-	32	mA
		current duty cycle $\leq 50\%$; $f_i \geq 1\text{ kHz}$	-	64	mA
T_{amb}	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	output enabled	0	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
V_{IK}	input clamping voltage	$V_{CC} = 2.7\text{ V}$; $I_{IK} = -18\text{ mA}$	-1.2	-0.9	-	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$; $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$	$V_{CC} - 0.1$	-	V
		$V_{CC} = 2.7\text{ V}$; $I_{OH} = -8\text{ mA}$	2.4	2.5	-	V
		$V_{CC} = 3.0\text{ V}$; $I_{OH} = -32\text{ mA}$	2.0	2.2	-	V

3.3 V octal transceiver with direction pin; 3-state

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
V _{OL}	LOW-level output voltage	V _{CC} = 2.7 V; I _{OL} = 100 µA		0.1	0.2	V
		V _{CC} = 2.7 V; I _{OL} = 24 mA	-	0.3	0.5	V
		V _{CC} = 3.0 V; I _{OL} = 16 mA	-	0.25	0.4	V
		V _{CC} = 3.0 V; I _{OL} = 32 mA	-	0.3	0.5	V
		V _{CC} = 3.0 V; I _{OL} = 64 mA	-	0.4	0.55	V
I _I	input leakage current	control pins				
		V _{CC} = 0 V or 3.6 V; V _I = 5.5 V	-	1	10	µA
		V _{CC} = 3.6 V; V _I = V _{CC} or GND	-	±0.1	±1	µA
		I/O data pins [2]				
		V _{CC} = 3.6 V; V _I = 5.5 V	-	1	20	µA
		V _{CC} = 3.6 V; V _I = V _{CC}	-	0.1	1	µA
		V _{CC} = 3.6 V; V _I = 0 V	-5	-1	-	µA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 0 V to 4.5 V	-	1	±100	µA
I _{LO}	output leakage current	V _O = 5.5 V; V _{CC} = 3.6 V; output HIGH	-	60	125	µA
I _{O(pu/pd)}	power-up/power-down output current	V _{CC} ≤ 1.2 V; V _O = 0.5 V to V _{CC} ; V _I = GND or V _{CC} ; $\overline{OE}$ = don't care [3]	-	15	±100	µA
I _{BHL}	bus hold LOW current	V _{CC} = 3.0 V; V _I = 0.8 V [4]	75	150	-	µA
I _{BHH}	bus hold HIGH current	V _{CC} = 3.0 V; V _I = 2.0 V	-150	-75	-	µA
I _{BHLO}	bus hold LOW overdrive current	V _{CC} = 0 V to 3.0 V; V _I = 3.6 V	500	-	-	µA
I _{BHHO}	bus hold HIGH overdrive current	V _{CC} = 0 V to 3.0 V; V _I = 3.6 V	-	-	-500	µA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A				
		outputs HIGH	-	0.13	0.19	mA
		outputs LOW	-	3	12	mA
		outputs disabled	-	0.13	0.19	mA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 3.0 V to 3.6 V; one input at V _{CC} - 0.6 V other inputs at V _{CC} or GND [5]	-	0.1	0.2	mA
C _I	input capacitance	DIR and $\overline{OE}$ inputs; V _I = 0 V or 3.0 V	-	4	-	pF
C _{I/O}	input/output capacitance	at input/output data pins, outputs disabled; V _{I/O} = 0 V or 3.0 V	-	10	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

[2] Unused pins at V_{CC} or GND.

[3] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms.

From V_{CC} = 1.2 V to V_{CC} = 3.6 V a transition time of 100 ms is permitted. This parameter is valid for T_{amb} = +25 °C only.

[4] This is the bus hold overdrive current required to force the input to the opposite logic state.

[5] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 7.

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
t _{PLH}	LOW to HIGH propagation delay	An to Bn or Bn to An; see Fig. 5				
		V _{CC} = 2.7 V	-	-	4.0	ns
		V _{CC} = 3.3 V ± 0.3 V	1.2	2.4	3.5	ns
t _{PHL}	HIGH to LOW propagation delay	An to Bn or Bn to An; see Fig. 5				
		V _{CC} = 2.7 V	-	-	4.0	ns
		V _{CC} = 3.3 V ± 0.3 V	1.2	2.4	3.5	ns
t _{PZH}	OFF-state to HIGH propagation delay	see Fig. 6				
		V _{CC} = 2.7 V	-	-	7.1	ns
		V _{CC} = 3.3 V ± 0.3 V	1.3	3.3	5.5	ns
t _{PZL}	OFF-state to LOW propagation delay	see Fig. 6				
		V _{CC} = 2.7 V	-	-	6.5	ns
		V _{CC} = 3.3 V ± 0.3 V	1.7	3.2	5.5	ns
t _{PHZ}	HIGH to OFF-state propagation delay	see Fig. 6				
		V _{CC} = 2.7 V	-	-	6.5	ns
		V _{CC} = 3.3 V ± 0.3 V	2.2	3.6	5.9	ns
t _{PLZ}	LOW to OFF-state propagation delay	see Fig. 6				
		V _{CC} = 2.7 V	-	-	5.1	ns
		V _{CC} = 3.3 V ± 0.3 V	2.2	3.4	5.0	ns

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 3.3 V

10.1. Waveforms and test circuit

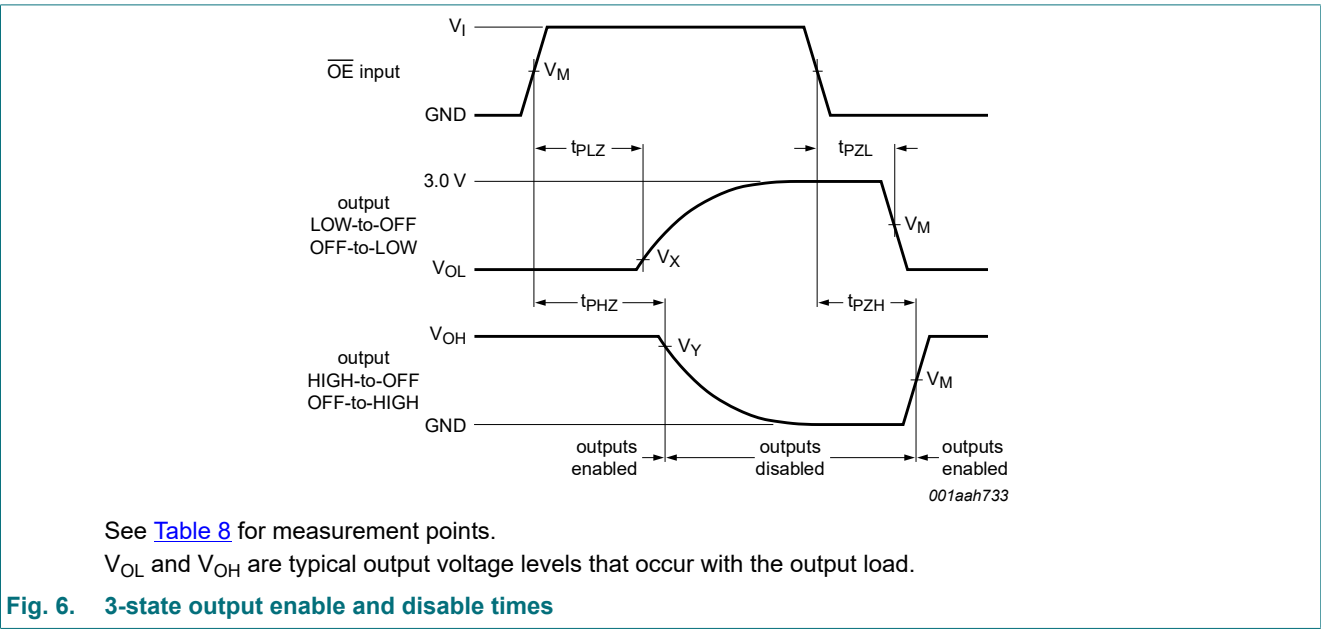
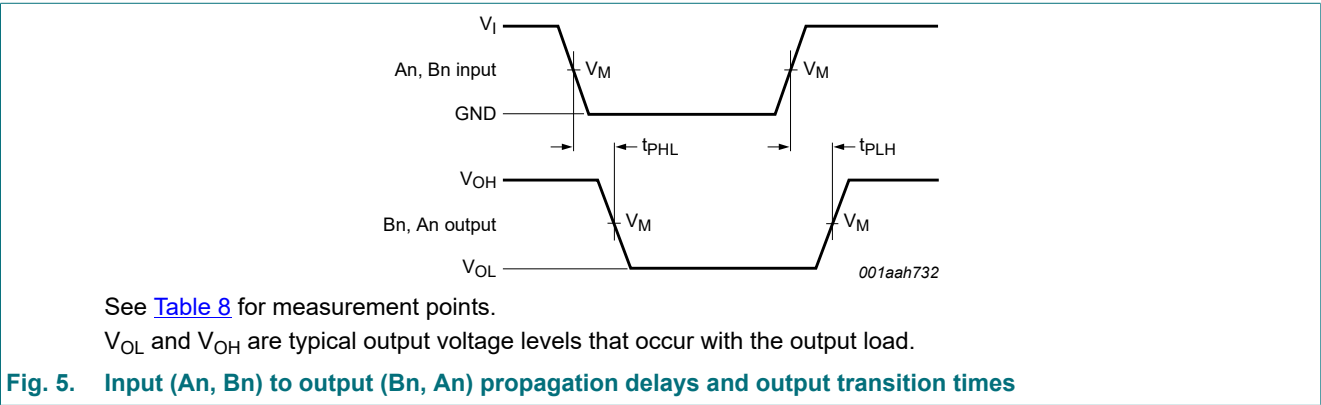
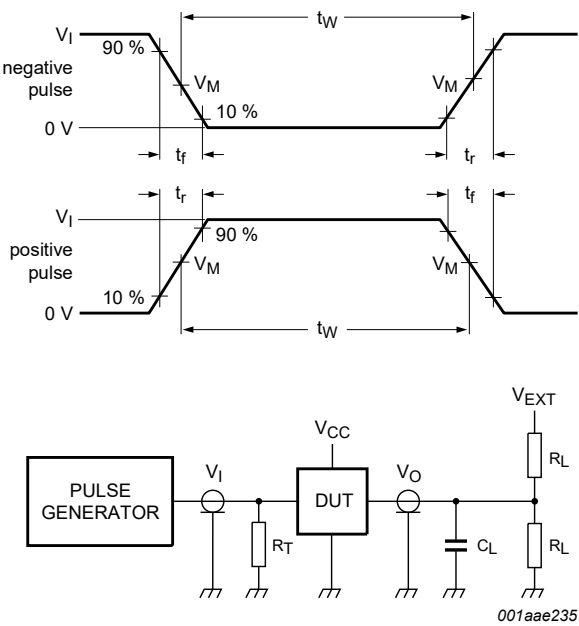


Table 8. Measurement points

V_{CC}	Input		Output		
	V_{IN}	V_M	V_M	V_x	V_y
2.7 V to 3.6 V	GND to 2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$



Test data is given in [Table 9](#).
Definitions test circuit:
 R_L = Load resistance;
 C_L = Load capacitance including jig and probe capacitance;
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;
 V_{EXT} = External voltage for measuring switching times.

Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	R_L	C_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	500 Ω	50 pF	GND	6 V	open

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

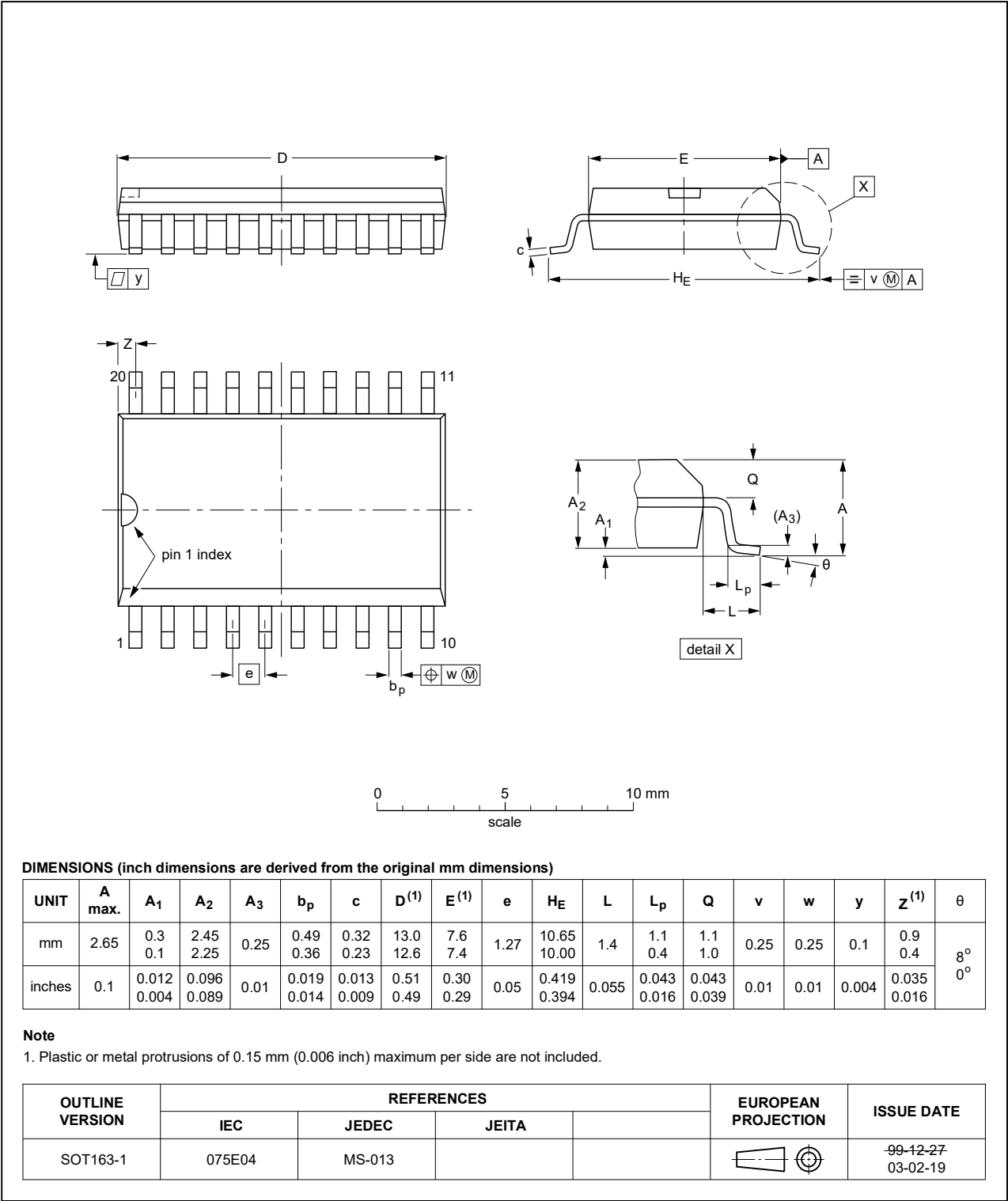


Fig. 8. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



Fig. 9. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

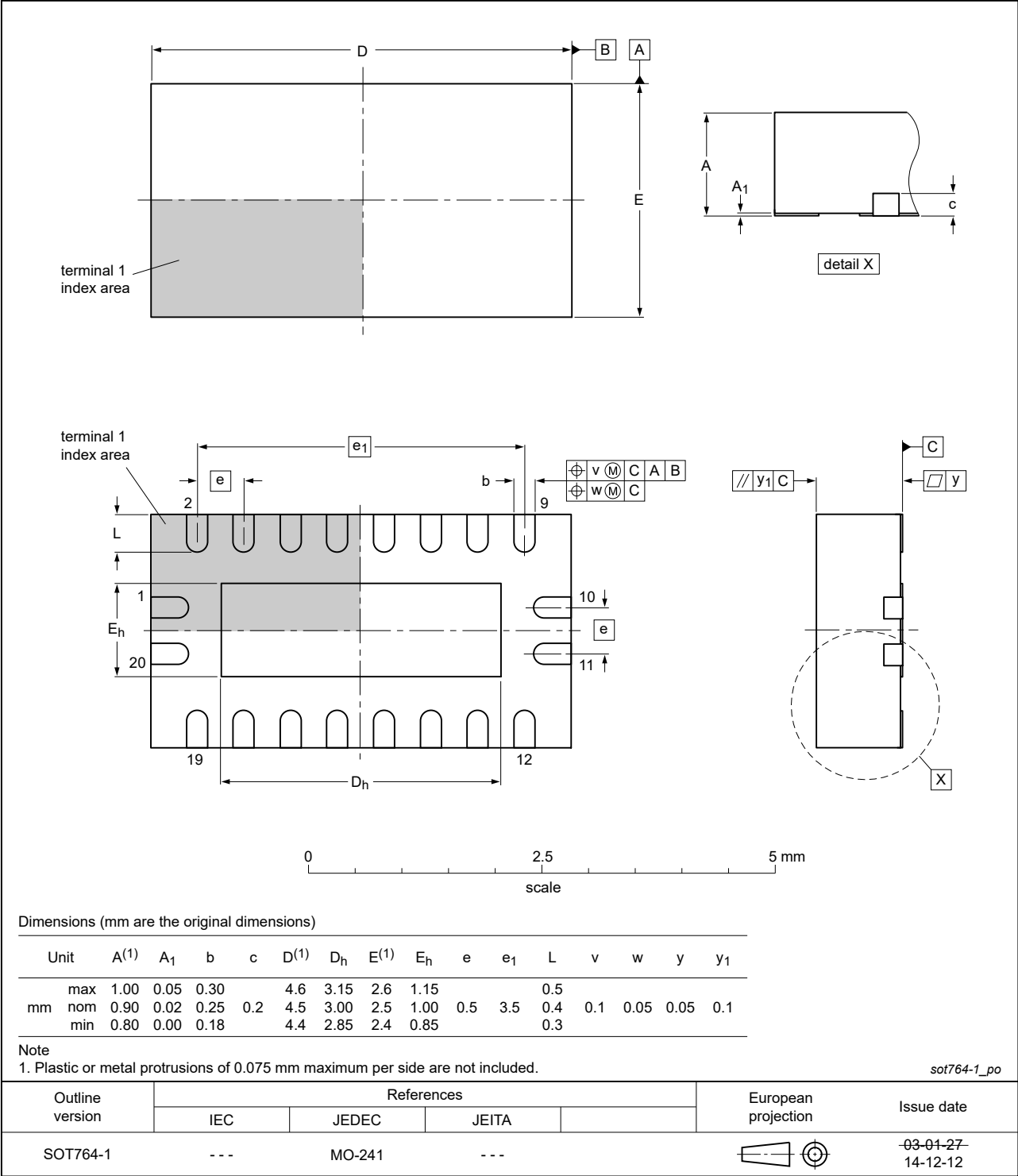


Fig. 10. Package outline SOT764-1 (DHVQFN20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT245B v.3	20210730	Product data sheet	-	74LVT245B v.2
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. - Type number 74LVT245BDB (SOT339-1/SSOP20) removed. Section 1 and Section 2 updated. Section 7: Derating values for P_{tot} total power dissipation removed. Fig. 10: Package outline drawing SOT764-1 (DHVQFN20) updated.			
74LVT245B v.2	20080508	Product data sheet	ECN07_046	74LVT245B v.1
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate. - DHVQFN20 package added to Section 3 "Ordering information" and Section 11 "Package outline".			
74LVT245B v.1	19990319	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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