FAIRCHILD SEMICONDUCTOR™

June 1988
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74F219
64-Bit Random Access Memory with 3-STATE Outputs

General Description

The 74F219 is a high-speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are 3-STATE and are in the high-impedance state whenever the Chip Select ($\overline{CS}$) input is HIGH. The outputs are active only in the Read mode. This device is similar to the 74F189 but features non-inverting, rather than inverting, data outputs.

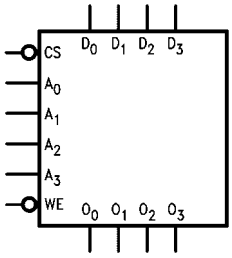
Features

- 3-STATE outputs for data bus applications
- Buffered inputs minimize loading
- Address decoding on-chip
- Diode clamped inputs minimize ringing
- Available in SOIC (300 mil only)

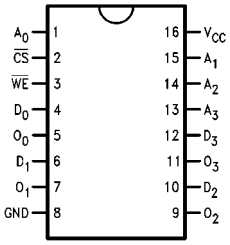
Ordering Code:

Order Number	Package Number	Package Description
74F219SC	M16B	16-Lead Small Outline Intergrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74F219PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Logic Symbol



Connection Diagram



Unit Loading/Fan Out

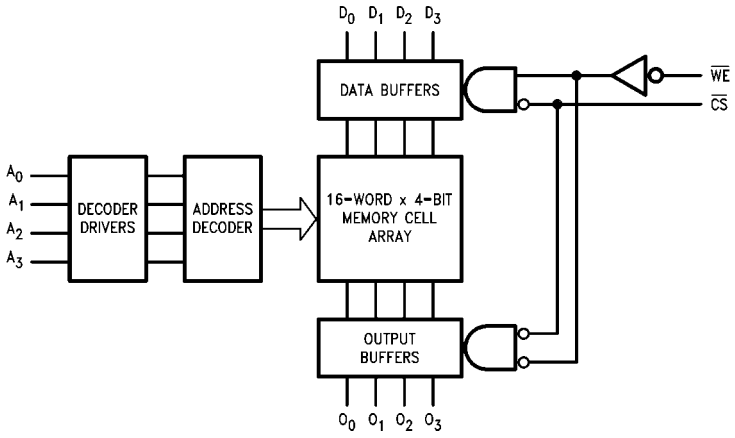
Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_0–A_3	Address Inputs	1.0/1.0	20 μA/–0.6 mA
$\overline{CS}$	Chip Select Input (Active LOW)	1.0/2.0	20 μA/–1.2 mA
$\overline{WE}$	Write Enable Input (Active LOW)	1.0/1.0	20 μA/–0.6 mA
D_0–D_3	Data Inputs	1.0/1.0	20 μA/–0.6 mA
O_0–O_3	3-STATE Data Outputs	150/40 (33.3)	–3 mA/24 mA (20 mA)

Function Table

Inputs		Operation	Condition of Outputs
$\overline{CS}$	$\overline{WE}$		
L	L	Write	High Impedance
L	H	Read	True Stored Data
H	X	Inhibit	High Impedance

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Block Diagram



Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH	10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
	Voltage	10% V_{CC}	2.4					I_{OH} = −3 mA
		5% V_{CC}	2.7					I_{OH} = −1 mA
		5% V_{CC}	2.7					I_{OH} = −3 mA
V_{OL}	Output LOW	10% V_{CC}			0.5	V	Min	I_{OL} = 24 mA
	Voltage							
I_{IH}	Input HIGH				5.0	µA	Max	V_{IN} = 2.7V
	Current							
I_{BVI}	Input HIGH Current				7.0	µA	Max	V_{IN} = 7.0V
	Breakdown Test							
I_{CEX}	Output HIGH				50	µA	Max	V_{OUT} = V_{CC}
	Leakage Current							
V_{ID}	Input Leakage		4.75			V	0.0	I_{ID} = 1.9 µA
	Test							All Other Pins Grounded
I_{OD}	Output Leakage				3.75	µA	0.0	V_{IOD} = 150 mV
	Circuit Current							All Other Pins Grounded
I_{IL}	Input LOW				−0.6	mA	Max	V_{IN} = 0.5V (A_n, $\overline{WE}$, D_n)
	Current				−1.2			V_{IN} = 0.5V ($\overline{CS}$)
I_{OZH}	Output Leakage Current				50	µA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current				−50	µA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test				500	µA	0.0V	V_{OUT} = 5.25V
I_{CC}	Power Supply Current			37	55	mA	Max	

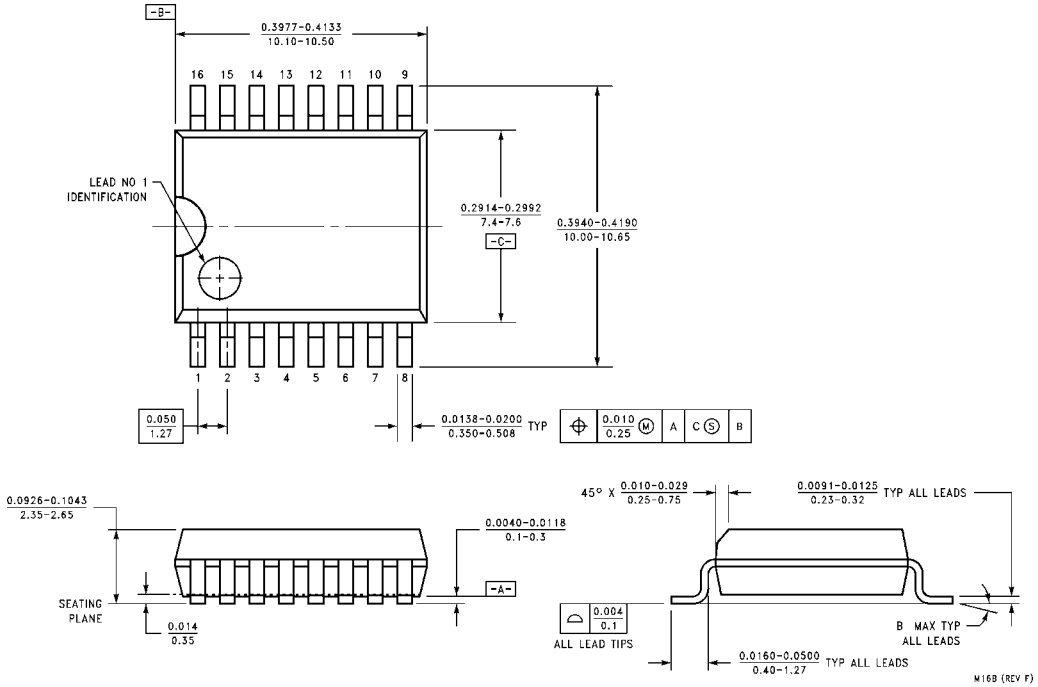
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = -55°C$ to $+125°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Access Time, HIGH or LOW	10.0	18.5	26.0	9.0	32.0	10.0	27.0	ns
t_{PHL}	A_n to O_n	8.0	13.5	19.0	8.0	23.0	8.0	20.0	
t_{PZH}	Access Time, HIGH or LOW	3.5	6.0	8.5	3.5	10.5	3.5	9.5	ns
t_{PZL}	$\overline{CS}$ to O_n	5.0	9.0	13.0	5.0	15.0	5.0	14.0	
t_{PHZ}	Disable Time, HIGH or LOW	2.0	4.0	6.0	2.0	8.0	2.0	7.0	
t_{PLZ}	$\overline{CS}$ to O_n	3.0	5.5	8.0	2.5	10.0	3.0	9.0	
t_{PZH}	Write Recovery Time	6.5	20.0	28.0	6.5	37.5	6.5	29.0	ns
t_{PZL}	HIGH or LOW, $\overline{WE}$ to O_n	6.5	11.0	15.5	6.5	17.5	6.5	16.5	
t_{PHZ}	Disable Time, HIGH or LOW	4.0	7.0	10.0	3.5	12.0	4.0	11.0	
t_{PLZ}	$\overline{WE}$ to O_n	5.0	9.0	13.0	5.0	15.0	5.0	14.0	

AC Operating Requirements

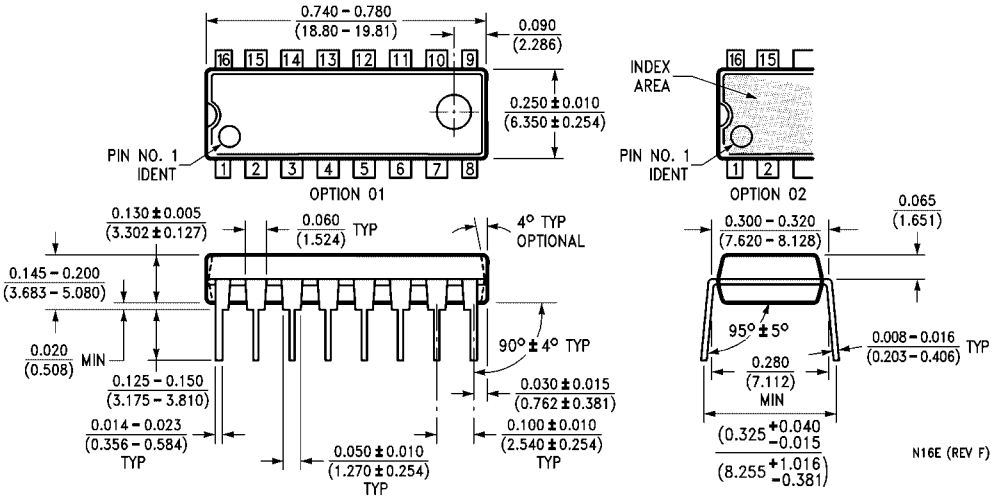
Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$		$T_A = -55°C$ to $+125°C$, $V_{CC} = +5.0V$		$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$		Units
		Min	Max	Min	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH or LOW	0		0		0		ns
$t_S(L)$	A_n to $\overline{WE}$	0		0		0		
$t_H(H)$	Hold Time, HIGH or LOW	2.0		2.0		2.0		
$t_H(L)$	A_n to $\overline{WE}$	2.0		2.0		2.0		
$t_S(H)$	Setup Time, HIGH or LOW	10.0		11.0		10.0		ns
$t_S(L)$	D_n to $\overline{WE}$	10.0		11.0		10.0		
$t_H(H)$	Hold Time, HIGH or LOW	0		2.0		0		
$t_H(L)$	D_n to $\overline{WE}$	0		2.0		0		
$t_S(L)$	Setup Time, LOW $\overline{CS}$ to $\overline{WE}$	0		0		0		ns
$t_H(L)$	Hold Time, LOW $\overline{CS}$ to $\overline{WE}$	6.0		7.5		6.0		
$t_W(L)$	$\overline{WE}$ Pulse Width, LOW	6.0		15.0		6.0		ns

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Intergrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M16B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E