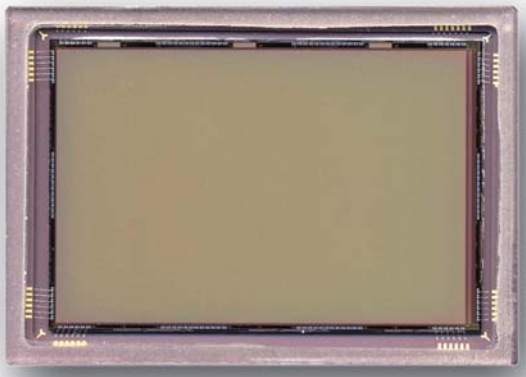
IBIS4-14000

14 M Pixel
Rolling shutter
CMOS image sensor



Datasheet

Document history record

Issue	*Date*	*Description of changes*
1.0	11-Aug-2003	Document created.
1.1	16-Sept-2003	p8: Table 1: power dissipation updated. p8: Table 2: QE*FF and SR*FF updated.
1.2	04-Jan-2005	Added Cypress equivalent part number, Part ordering table. Added Cypress Document # 38-05709 Rev ** in the document footer.

1. Preamble

1.1 Overview

This document describes the interfacing and the driving of the image sensor IBIS4-14000. The IBIS4-14000 is a monochrome CMOS active pixel image sensor. It is based on the high-fill factor active pixel sensor technology of FillFactory (US patent No. 6,225,670 and others).

This datasheet allows the user to develop a camera system based on the described timing and interfacing.

1.2 Main features

The main features of the image sensor are identified as:

- 8x8 μm^2 square pixels.
- 3048 x 4560 active pixels (13.9-mega-pixel).
- 36 x 24 mm^2 focal plane array (35 mm photographic film format).
- Frame rate: 3 full frames/s (4 outputs).
- Max. 15 MHz pixel clock rate.
- Random programmable windowing and sub-sampling modes.
- Electronic rolling shutter.
- 4 parallel analog outputs.
- Optical dynamic range of 65 dB.
- On-chip fixed pattern noise correction.

1.3 Part number

Name	***Package***	***Monochrome***
IBIS4-14000-M	49-pins PGA package	Monochrome
CYII4SM014KAA-GBC – (Preliminary)		
IBIS4-14000-C		
CYII4SC014KAA-GAC – (Preliminary)		

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2. Architecture

2.1 Architecture of the IBIS4-14000 – block diagram

The basic architecture of the sensor is shown in Figure 1.

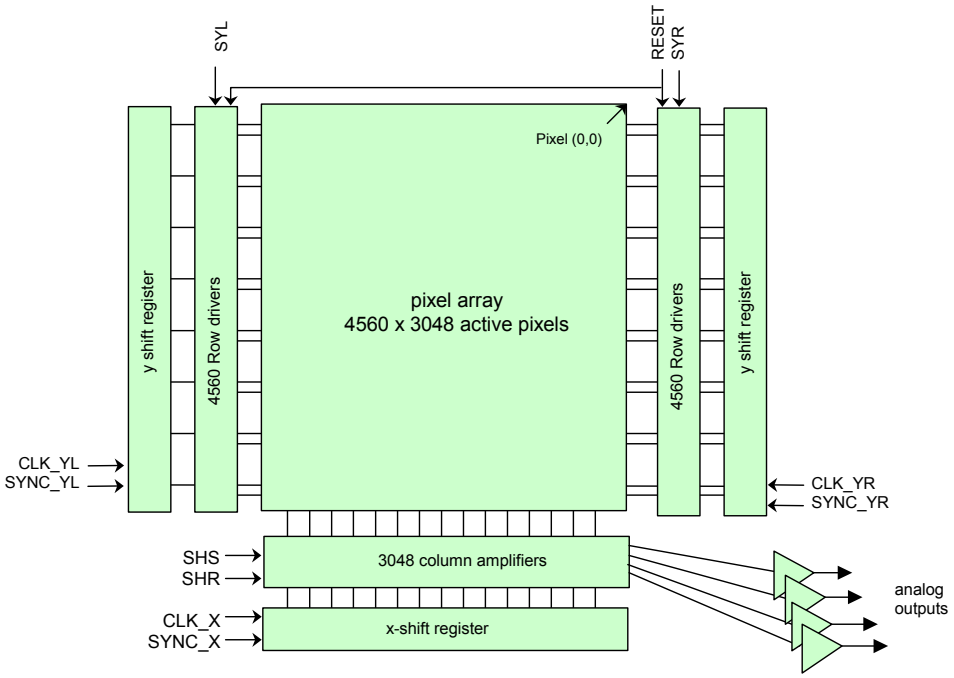
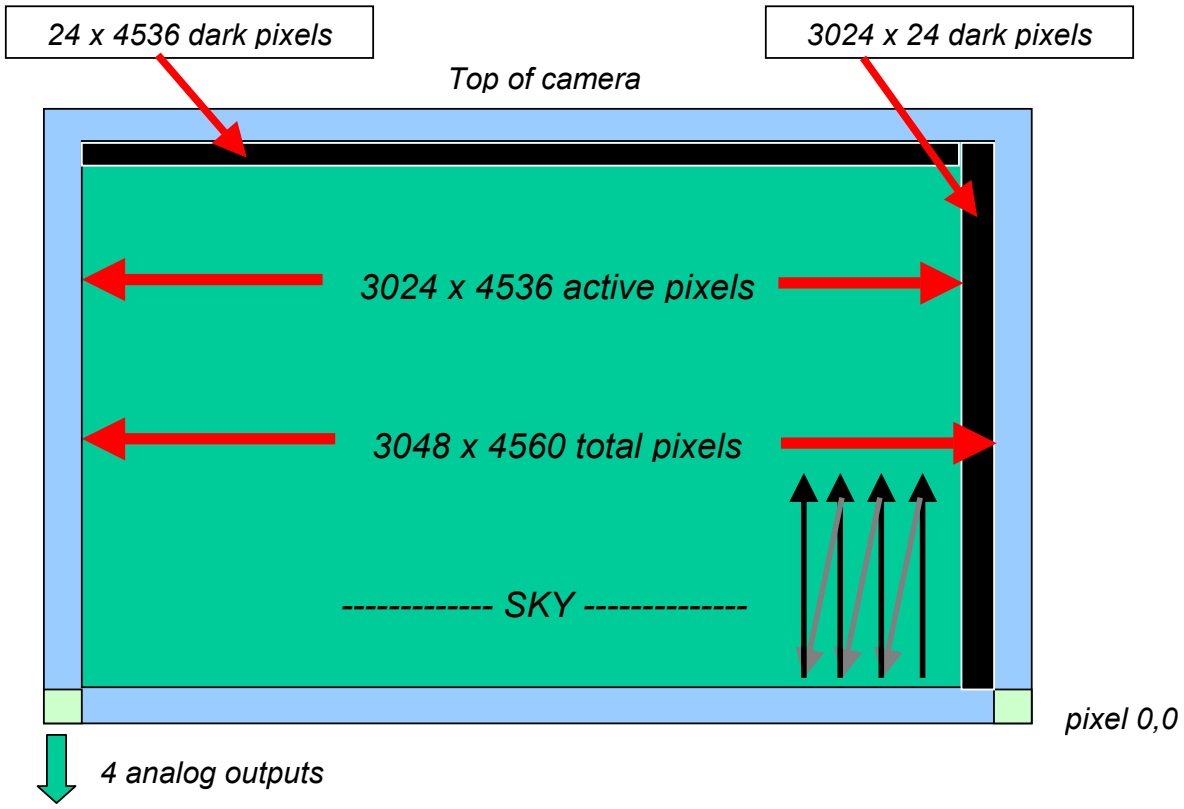


Figure 1: imager architecture

The Y shift registers point at a row of the imager array. This row is selected and/or reset by the row drivers. There are 2 Y shift registers: one points at the row that is read out and the second one points at the row to be reset. The second pointer may lead the first pointer by a specific number of rows. In that case, the time difference between both pointers is the integration time. Alternatively, both shift registers be point at the same row for reset and readout for a faster reset sequence. When the row is read out, it is also reset in order to do double sampling for fixed pattern noise reduction.

The pixel array of the IBIS4-14000 consists of 4536 x 3024 active pixels and 24 additional columns and rows, which can also be addressed (see Figure 2).

The column amplifiers read out the pixel information and perform the double sampling operation. They also multiplex the signals on the readout busses, which are buffered by the output amplifiers.



The shift registers can be configured for various sub-sampling modes. The output amplifiers can be individually powered down. And some other extra functions are foreseen. These options are configurable via a serial input port.

2.2 Pixel specifications

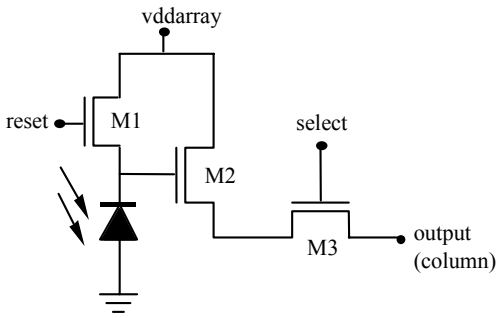


Figure 3: pixel schematic

The pixel is a classic 3-transistor active pixel. The photodiode is a high-fill factor n-well/p-substrate diode. Separate power supplies are foreseen: general power supply for the analog image core (VDD), power supply for the reset line drivers (VDDR) and a separate power supply for the pixel itself (VDDARRAY).

3. Specifications

3.1 General specifications

Table 1: IBIS4-14000 general specifications

Parameter	*Value*	*Remark*
Pixel architecture	*3T pixel*	
Technology	*CMOS*	
Pixel size	*8 x 8 µm²*	
Resolution	*3048 x 4560*	13.9 mega pixels
Power supply	*3.3V*	
Shutter type	*Electronic rolling shutter*	
Pixel rate	*15 MHz nominal*	20 MHz with extra power dissipation.
Power dissipation	*176 mW* *53 mA*	

3.2 Electro-optical specifications

Table 2 lists the electro-optical specifications. All parameters are set using the default settings (see recommended operating conditions), unless otherwise specified.

Table 2: IBIS4-14000 electro-optical specifications.

Parameter	*Value*	*Remark*
Effective conversion gain	*18.5 µV/e-*	See note 1.
Spectral response * fill factor	*0.22 A/W (peak)*	
Peak Q.E. * fill factor	*40%*	Between 500 and 700 nm.
Full Well charge	*64865 electrons*	See note 1.
Linear range	*90 % of full well charge*	Linearity definition: < 3% deviation from straight line through zero point.
Temporal noise (kTC noise limited)	*35 electrons*	kTC noise, being the dominant noise source in the dark at short integration times.
Dynamic range	*1871:1 (65.4 dB)*	See note 1.
Linear dynamic range	*1688:1 (64.5 dB)*	See note 1. 3% deviation.
Average dark current	*55 pA/cm²*	Average value At 24 °C lab temperature.
Dark current signal	*223 electrons/s*	Average value At 24 °C lab temperature.

Parameter	Value	Remark
	4.13 mV/s (average) *Limit TBD (10 mV/s)*	
MTF at Nyquist	*0.55 in X* *0.57 in Y*	Measured at 600 nm.
Fixed pattern noise (local)	*0.11 % Vsat RMS*	Average value of RMS variation on local 32 x 32 pixel windows.
Fixed pattern noise (global)	*0.15% Vsat RMS*	
PRNU	*<1% RMS of signal*	
Anti-blooming	10^5	Charge spill-over to neighboring pixels (= CCD blooming mechanism)

Notes:

1. Settings: VDD=3.3 V, VDDR =4V and VDD_ARRAY = 3V.

3.3 Spectral response curve

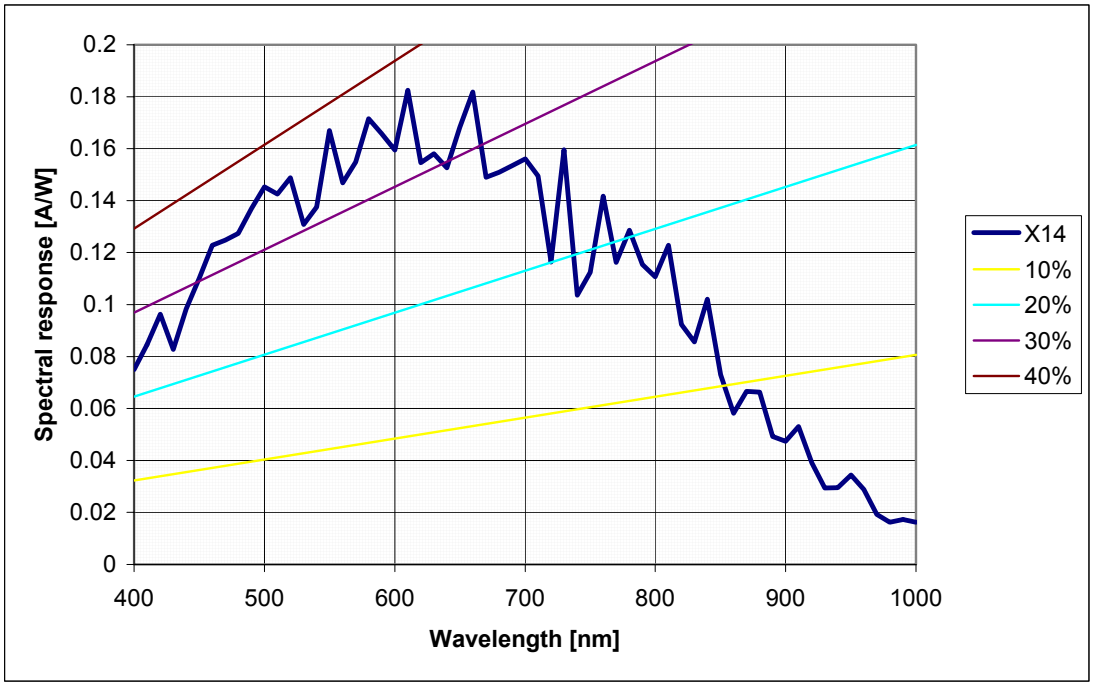


Figure 3: Spectral response curve

3.4 Electrical specifications

3.4.1 Output stage

Unity gain buffers are implemented as output amplifiers. These amplifiers can directly be DC coupled to the analog-digital converter or coupled to an external programmable gain amplifier.

The (dark reference) offset of the output signal is adjustable between 1.7 and 3 V. The amplifier output signal is negative going with increasing light levels, with a max. amplitude of 1.2 V (at 4V reset voltage, in hard reset mode). Table 3 summarizes the electrical specifications.

Table 3: Electrical specifications

Parameter	*Value*	*Remark*
Nominal power supply	*3.3 V*	
Frame rate	*3.25 frames/s (1)*	(1): 4 parallel analog outputs. (excluded readout of "reset black" pixels).
Output signal amplitude	*1.2 V*	Negative signal polarity (lower signal for increasing light levels).
Output signal range	*0.5 – 3 V*	Offset adjustable with DARKREF input pin
Slew rate	*To be measured*	Can be tuned by resistor connected to OBIAS pin
Settling time (stable output within 500 µV from final value)	*To be measured*	

Notes on analog video signal and output amplifier specifications:

1. Video polarity: the video signal is negative going with increasing light level.

2. Signal offset: the analog offset of the video signal is settable by an external DC bias (pin 12 DARKREF). The settable range is between 1.7 and 3 V, with 2.65 V being the nominal expected set point. The output range (including 1.2 V video signal) is thus between 3 V and 0.5V.

3. Power control: the output amplifiers can be switched between an "operating" mode and a "standby" mode via the serial port of the imager (see SPI register configuration).

4. Coupling: the IBIS4-14000 can be DC or AC coupled to the AD converter.

3.4.2 Absolute maximum ratings

Table 4: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DC}	DC supply voltage	-0.5 to +4.5	V
V_{IN}	DC input voltage	-0.5 to V_{DC} + 0.5	V
V_{OUT}	DC output voltage	-0.5 to V_{DC} + 0.5	V
I	DC current per pin; any single input or output.	± 50	mA
T_{STG}	Storage temperature range.	-10 to 66 (@ 15% RH) -10 to +38 (@ 86% RH) (RH = relative humidity)	°C
Altitude		8000	feet

Note: Absolute Ratings are those values beyond which damage to the device may occur.

3.4.3 Recommended operating specifications

Table 5: Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Nominal power supply.		3.3		V
VDDRL VDDRR	Reset power supply level.		4		V
VDD_ARRAY	Pixel supply level.		3		V
DARKREF	Dark reference offset level.	1.7	2.65	3	V
GNDAB	Anti-blooming ground level.	0	0	1	V
V_{OUT}	Analog output level.	0.5		3	V
V_{IH}	Logic input high level.	2.5		3.3	V
V_{IL}	Logic input low level.	0		1	V
T_A	Commercial operating temperature.	0		50	°C (@ 15% RH)
T_A	Commercial operating temperature.	0		38	°C (@ 86% RH)

3.4.4 Bias currents and references

Table 6: bias input currents

Pin number	*Pin name*	*Connection*	*Input current*	*Pin voltage*
1	OBIAS	10 kΩ to VDD	179 uA	1.51 V
36	CBIAS	22 kΩ to VDD	91 uA	1.29 V
37	PCBIAS	22 kΩ to VDD	91 uA	1.29 V
48	XBIAS	10 kΩ to VDD	181uA	1.49 V
49	ABIAS	Gnd or open (or 10M to VDD)		0.8 V in case of 10 M

Tolerance on bias reference voltages: +/- 150 mV

3.4.5 Handling

3.4.5.1 ESD

Though not as sensitive as CCD sensors, the IBIS4-14000 is vulnerable to ESD like other standard CMOS devices. Take into account standard ESD procedures when manipulating the device.

1) Always discharge static electricity by grounding the human body and the instrument to be used. To ground the human body, provide a resistance of 1 MOhm between the human body and the ground to be on the safe side.

2) When directly handling the device with the fingers, hold the part without the leads and do not touch any lead.

3) To avoid generating static electricity:

   i. do not scrub the glass surface with cloth or plastic

   ii. do not attach any tape or labels

   iii. do not clean the glass surface with dust-cleaning tape

4) When storing or transporting the device, put it in a container of conductive material.

3.4.5.2 Dust and Contamination

Dust or contamination of the glass surface could deteriorate the output characteristics or cause a scar. In order to minimize dust or contamination on the glass surface, take the following precautions:

1) handle the device in a clean environment such as a cleaned booth (the cleanliness should be, if possible, class 100)

2) Do not touch the glass surface with the fingers.

3) Use gloves to manipulate the device

3.4.5.3 Soldering

Soldering should be manually performed with 5 seconds at 350 °C maximum at the tip of the soldering iron

Avoid mechanical stress when mounting the device.

4. Operation

4.1 Readout and sub-sampling modes

The sub-sampling modes available on the IBIS4-14000 are summarized in Table 7.

Table 7: Sub-sample modes

Subsampling modes programmed into SPI register		
X shift register subsampling settings		
Bitcode	*Mode*	*Use*
000 001 010	1:1 Full resolution (all columns)	Full resolution (4 outputs) 4:1 subsampling
011	24:1 Select 4 columns/ skip 20	24:1 subsampling (2 outputs)
100	8:1 Select 4 columns / skip 4s	8:1 subsampling (2 outputs)
101	12:1 Select 4 columns / skip 8	12:1 subsampling (2 outputs)
Y shift register subsampling settings		
Bitcode	*Mode*	*Use*
000 010 100	4:1 Select 2 rows / skip 2	4:1 subsampling
001	1:1 Full resolution (all rows)	Full resolution
011	6:1 Select 2 rows / skip 4	6:1 subsampling
101	12:1 Select 2 rows / skip 10	12:1 subsampling

Each mode is selected independently for the X and Y shift registers. The sub-sampling mode is configured via the serial input port of the chip. The Y and X shift

registers have some different sub-sampling modes, due to constraints in the design of the chip.

The baseline full resolution operation mode uses 4 outputs to read out the entire image. 4 consecutive pixels of a row are put in parallel on the 4 parallel outputs.

Sub-sampling is implemented by a shift register with hard-coded sub-sample modes. Depending on the selected mode, the shift register skips the required number of pixels when shifting the row or column pointer.

The X shift register always selects 4 consecutive columns in parallel. Sub sampling in X can be done by activating one of the modes wherein a multiple of 4 consecutive columns is skipped on a CLK_X pulse. The Y shift register selects a single row. It will consecutively select 2 adjacent rows and then skip an amount of rows set by the sub sample mode. This implementation is chosen for easy sub sampling of color images through a 2-channel readout. In this way color data from 2x2 pixels is made available in all sub sample modes. On monochrome sensors this is not required, only one output can be used and the each second row selected by the Y shift register can be skipped. This doubles the frame rate. Note that for 2 or 1 channel readout, the not-used output amplifiers can be powered down through the SPI shift register.

Rows can also be skipped by extra CLK_Y pulses. It is not required to apply additional control pulses to rows that are skipped. This is a way to implement extra sub-sampling schemes. For example, to support the 24:1 X shift register mode also vertically, the Y shift register can be set to the 12:1 mode and an additional CLK_Y pulse needs to be given at the start of each row.

Table 8 lists the frame rates of the IBIS4-14000 in various sub-sample modes with only one output. The row blanking time (dead time between readout of successive rows) has been set to 17.5 µs.

Table 8: frame rates and resolution of theIBIS4-14000 in various sub-sampling modes

Ratio	***#outputs***	***Image Resolution***	***Frame rate frames/s***	***Frame readout time [s]***
1:1	4	3024 x 4536	3.25	0.308
4:1	1	756 x 1134	12.99	0.077
8:1	1	378 x 567	41.30	0.024
12:1	1	252 x 378	77.13	0.013

Note that the 24 additional columns and rows (see Figure 2) do not sub sample.

4.2 Sensor output stage

4.2.1 Amplifier specifications

Unity gain buffers are implemented as output amplifiers. Paragraph 3.4 lists the specifications of the output amplifier stage.

4.2.2 Output amplifier crossbar switch (multiplexer)

A crossbar switch is available that routes the green pixels always to the same output (for a color device). The switch can be controlled automatically (with a toggle on every CLK_Y rising edge) or manually (through the SPI register).

Figure 6 shows how it works. A pulse on SYNC_Y resets the crossbar switch. The initial state after reset of the switchboard is read from the SPI control register. When the automatic toggling of the switchboard is enabled, it toggles on every rising edge of the CLK_Y clock. Separate pins are used for the SYNC_Y and CLK_Y signals on the crossbar logic these pins can be connected to the SYNC_YL and CLK_YL pins of the shift register that is used for readout.

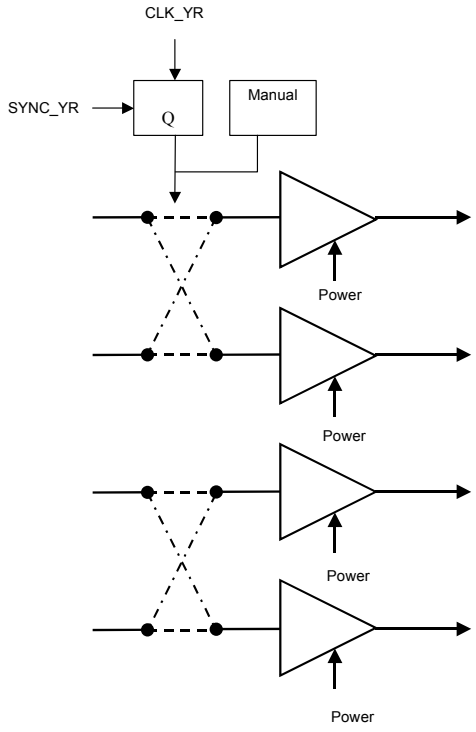


Figure 4: output amplifier crossbar switch

4.3 Sensor readout timing diagrams

4.3.1 Row sequencer

The row sequencer controls pulses to be given at the start of each new line. Figure 7 shows the timing diagram for this sequence.

The signals to be controlled at each row are:

- CLK_YL and CLK_YR: these are the clocks of the YL and YR shift register. They can be driven by the same signals and at a continuous frequency. At every rising edge, a new row is being selected.
- SELECT: this signal selects the line that is currently sampled. It is important that PC and SELECT are never active together.
- PC: an initialization pulse that needs to be given after the selection of a new row.
- SHS (Sample & Hold pixel Signal): this signal controls the track & hold circuits in the column amplifiers. It is used to sample the pixel signal in the columns. (0=track ; 1=hold)
- RESET: this pulse resets the pixels of the row that is currently being selected. In rolling shutter mode, the RESET signal is pulsed a second time to reset the row selected by the YR shift register. For “reset black” dark reference signals, the reset pulse can be pulsed also during the first PC pulse. Normally, RESET and PC have a rising edge at the same position. The falling edge of RESET lags behind the falling PC edge.
- SHR (Sample & Hold pixel Reset level): this signal controls another track & hold circuit in the column amplifiers. It is used to sample the pixel reset level in the columns (for double sampling). (0=track ; 1=hold)
- SYL (Select YL register): Selects the YL shift register to drive the reset line of the pixel array
- SYR (Select YR register): Selects the YR shift register to drive the reset line of the pixel array. For rolling shutter applications, SYL and SYR are complimentary. In full frame readout, both registers may be selected together, only if it is guaranteed that both shift registers point to the same row. This can reduce the row blanking time.
- SYNC_YR and SYNC_YL: Synchronization pulse for the YR and YL shift registers. The SYNC_YR/SYNC_YL signal is clocked in during a rising edge

on CLK_YR/CLK_YL and resets the YR/YL shift register to the first row. Both pulses are pulsed only once each frame. The exact pulsing scheme depends on the mode of use (full frame/ rolling shutter). A 200 ns set-up time applies. See further.

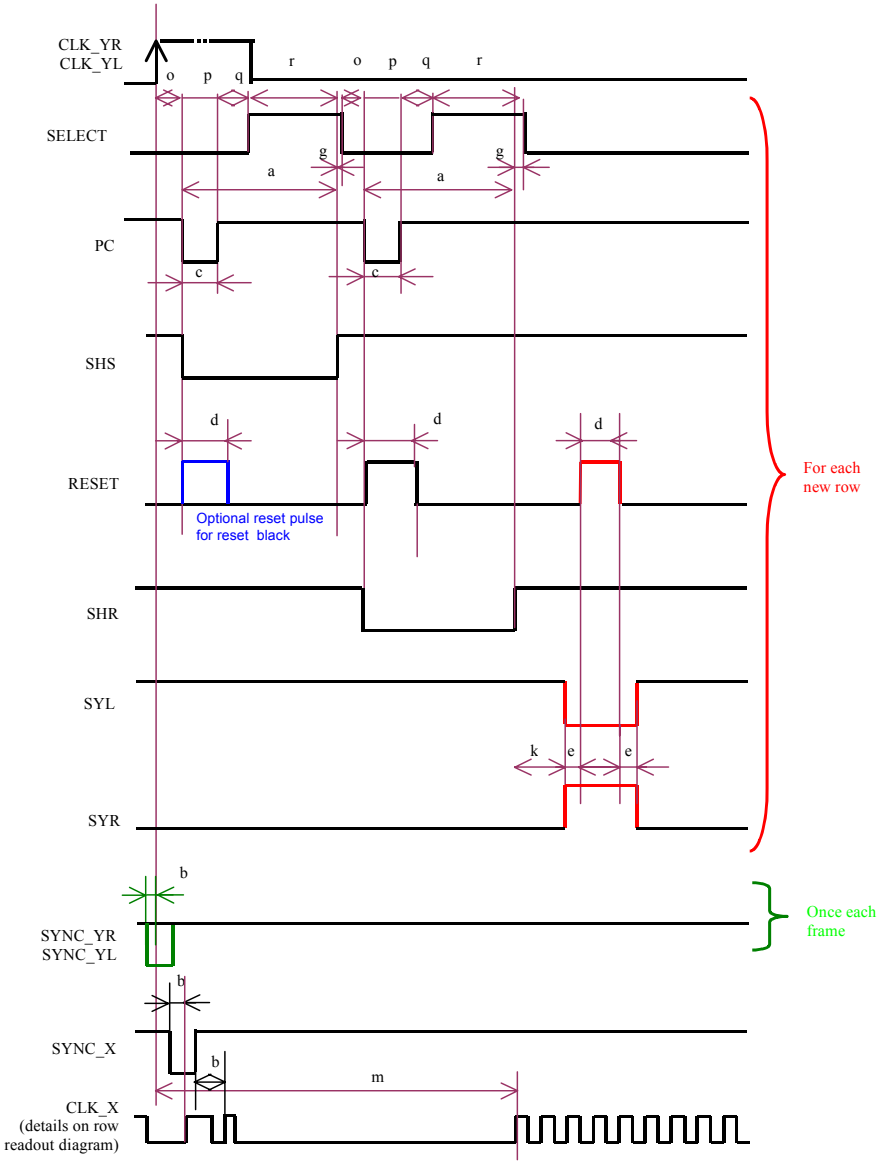


Figure 5: row sequencer timing diagram

- SYNC_X: resets the column pointer to the first row. This has to be done before the end of the first PC pulse, in case when the previous line has not been read out completely.

Figure 5 shows the basic timing diagram of the IBIS4-14000 image sensor and Table 10 shows the timing specifications of the clocking scheme.

Table 9: Timing specifications

Symbol	Min	Typ	Description
a		6.8 us	Delay between falling edge on PC and rising edge on SHS/SHR. Duration of SHS/SHR pulse.
b	200 ns	600 ns	Min. SYNC setup times. SYNC_Y is clocked in on rising edge on CLK_Y. SYNC_Y pulse must overlap CLK_Y by one clock period. Setup times of 200 ns apply after SYNC edges. Within this setup time no rising CLK edge may occur.
c		2.7 us	Duration of PC pulse.
d		4 us	Duration of RESET pulse.
e	d + 2 * CLK	0.5 us	SYL and SYR pulses must overlap second RESET pulse at both sides by one clock cycle.
f	0us		Delay between rising edge on CLK_YR and falling edge on SELECT.
g	1 CLK	0.1 us	Delay between rising edge on SHS and falling edge on SELECT.
k	1 CLK	0.1 us	Delay between rising edge on SHR and rising edge on SYR
m		17.5 us	Minimal total idle time between readout of two rows (vertical interval time).
o		1.4 us	Delay between falling edge SELECT and PC.
p		5.4 us	Total SELECT pulse duration (low period).
q		1.3 us	Delay between rising edge on PC and rising edge on SELECT.
r		6.6 us	Delay between rising edge on SELECT and rising edge on SHS/SHR.

Notes:

- CLK = one clock period of the master clock, shortest system time period available.

- Red items apply each row; green items apply once each frame. Blue is for the additional reset for reset black pixels.

In the above timing diagram, the YR shift register is used for the electronic shutter. The CLK_YR is driven identically as CLK_YL. The SYNC_YR pulse leads the SYNC_YL pulse by a given number of rows. Relative to the row timing, both SYNC pulses are given at the same time position.

SYNC_YR and SYNC_YL are only pulsed once each frame, SYNC_YL is pulsed when the first row will be read out and SYNC_YR is pulsed for the electronic shutter at the appropriate moment in time.

This timing assumes that the registers that control the sub-sampling modes have been loaded in advance (through the SPI interface), before the pulse on SYNC_YL or SYNC_YR.

The second reset pulse and the pulses on SYL and SYR (all pulses drawn in red) are only applied when the rolling electronic shutter is used. For full frame integration, these pulses are skipped.

The SYNC_Y pulse is also used to initialise the switchboard (output multiplexer). This is also done by a synchronous reset on the rising edge of CLK_Y. Normally the switchboard is controlled by the shift register used for readout (this is the YL shift register). This means that pin SYNC_Y can be connected to SYNC_YL, and pin CLK_Y can be connected to CLK_YL.

The additional RESET BLACK pulse (indicated in blue in Figure 5) can be given to make one or more lines black. This can be useful to generate a dark reference signal.

4.3.2 Timing pulse pattern for readout of a pixel

Figure 6 shows the timing diagram to preset (sync) the X shift register, read out the image row, and analog-digital conversion. There are 3 tasks:

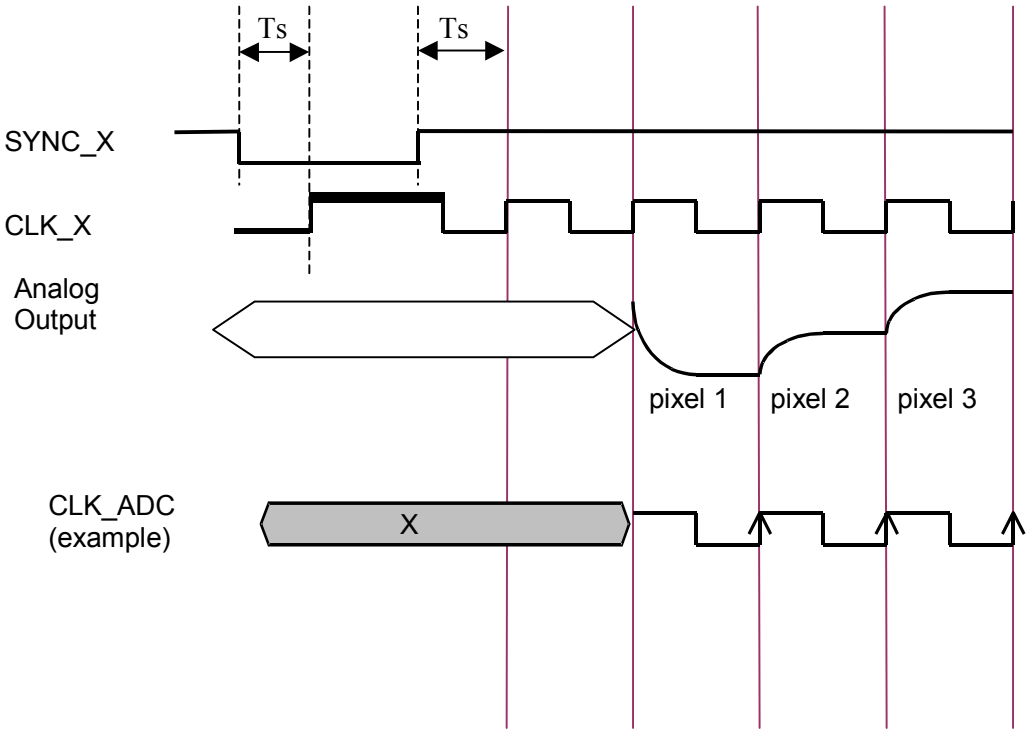


Figure 6: Pixel row read-out timing

- preset the X shift register : apply a low level to SYNC_X during a rising edge on CLK_X at the start of a new row
- readout of the image row : pulse CLK_X
- analog-digital conversion : clock the ADC

The SYNC pulses perform a synchronous reset of the shift registers to the first row/column on a rising edge on CLK. This is identical for all shift registers (YR, YL and X).

Important : The SYNC_X signal has a set-up time Ts of 150 ns. For the YR and YS shift registers, the set-up time is 200 ns. CLK_X must be stable at least during this set-up time.

In case where a partial row readout has been performed, 2 CLK_X pulses (with SYNC_X = LOW) are required to fully deselect the column where the X pointer has been stopped. A single CLK_X will leave the column partially selected, which will then have a different response when read out in the next row. When full row readout has been performed, the last column will be fully deselected by a single CLK_X pulse (with SYNC_X=LOW). The X-register is reset by a single CLK_X pulse (with SYNC_X=LOW). In case of partial row readout, the SYNC_X pulse has to be given before the sample pulses (SHR and SHS) of the row sampling process, in order to avoid a different response of the last column of the previous window.

For the X shift register, the analog signal is delayed by 2 clock periods before it becomes available at the output (due to internal processing of the signal in the columns and output amplifier). The figure gives an example of an ADC clock for an ADC that samples on the rising edge.

4.3.3 Fast frame reset timing diagram

Figure 9 shows the reset timing for a fast frame reset.

SYL and SYR can be kept both high to make the reset mechanism faster and reduce propagation delays. PC, SHS, SHR can be kept high since they don't interact with the pixel reset mechanism. Table 10 lists timing specifications for RESET, CLK_Y and SELECT.

Table 10: timing specifications for fast reset (preliminary)

Symbol	*Typical*	*Description*
a	0 us	Delay between rising CLK_Y edge and Reset.
b	4 us	Reset pulse width.
c	0	Reset hold time.
d	1.6 us	Select pulse width.
e	1 us	Setup hold time. CONSTRAINT : a + e > 1 us due to propagation delay on pixel select line.

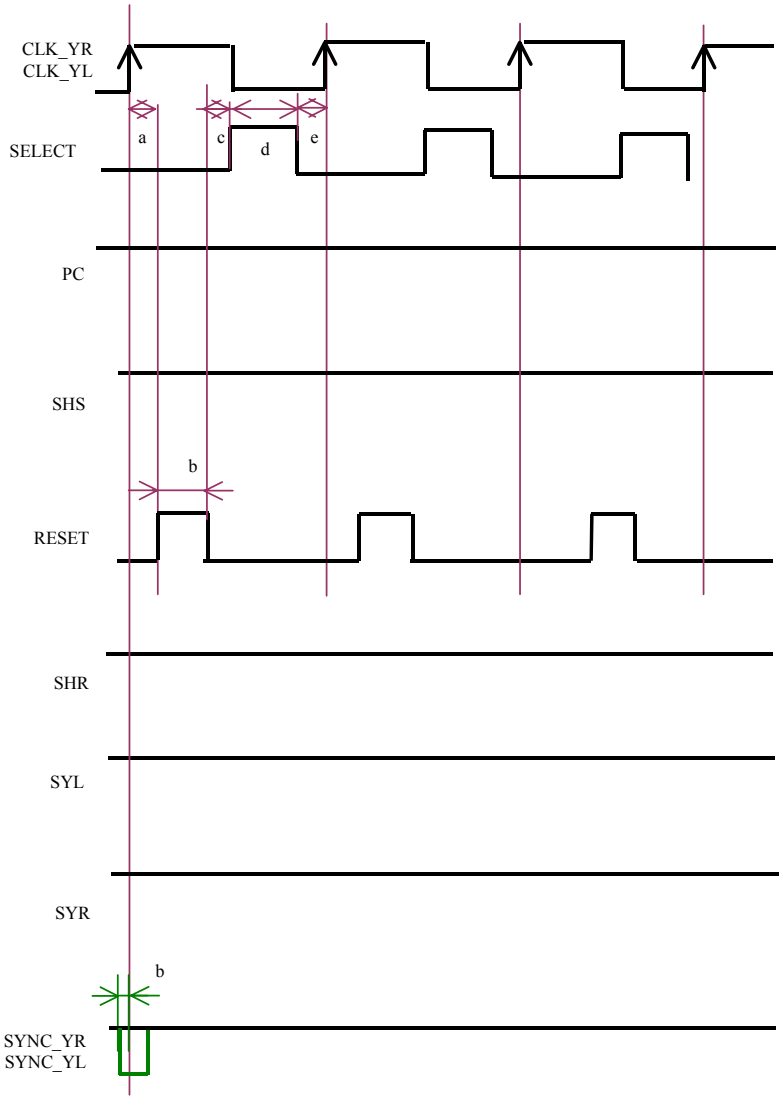


Figure 7: fast frame reset timing

4.4 SPI register

4.4.1 SPI Interface architecture

The elementary unit cell of the serial to parallel interface consists of two D-flip-flops. The architecture is shown in Figure 10. 16 of these cells connected in parallel, having a common /CS and SCLK form the entire uploadable parameter block, where D_{in} is connected to D_{out} of the next cell. The uploaded settings are applied to the sensor on the rising edge of signal /CS.

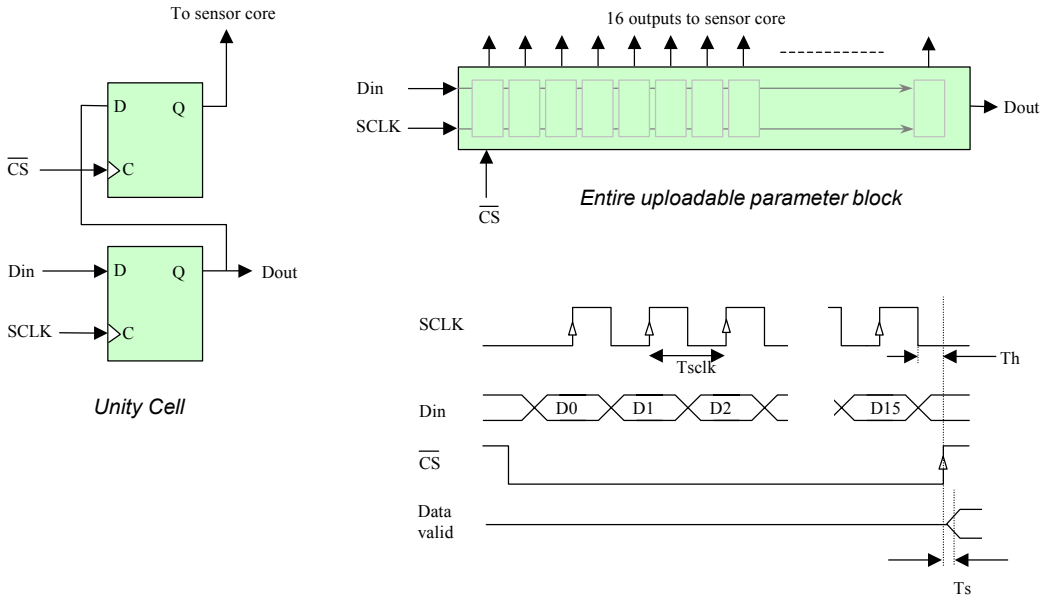


Figure 8: Uploadable parameter part

Table 11: Timing requirements serial-parallel interface

Parameter	*value*
Tsclk	100ns
Ts	50ns
Th	50ns

4.4.2 SPI register definition

Sensor parameters can be serially uploaded inside the sensor at the start of a frame. The parameters are :

- Sub-sampling modes for X and Y shift registers (3-bit code for 6 sub-sampling modes)
- Sensor test mode and electrical black pixel mode
- Power control of the output amplifiers, column amps and pixel array. Each amplifier can be individually powered up/down
- Output crossbar switch control bits. The crossbar switch is used to route the green pixels to the same output amplifiers at all time. A first bit controls the crossbar. When a second bit is set, the first bit will toggle on every CLK_Y edge in order to automatically route the green pixels of the bayer filter pattern.

The code is uploaded serially as a 16-bit word (LSB uploaded first). Table 12 lists the register definition. The default code for a full resolution readout is 33342 (decimal) or 1000 0010 0011 1110

Table 12: serial sensor parameters register bit definitions

BIT	***Description***
0 (LSB)	set to zero (0)
1	1= power on sensor array ; 0= power down
2	1 = power up output amplifier 4; 0 = power down
3	1 = power up output amplifier 3; 0 = power down
4	1 = power up output amplifier 2; 0 = power down
5	1 = power up output amplifier 1; 0 = power down
6	3 –bit code for sub-sampling mode of X shift register:
7	000 = full resolution 011 = select 4, skip 20 001 = full resolution 100 = select 4, skip 4
8	010 = full resolution 101 = select 4, skip 8
9	3 –bit code for sub-sampling mode of Y shift registers:
10	000 = select 2, skip 2 011 = select 2, skip 4 001 = full resolution 100 = select 2, skip 2
11	010 = select 2, skip 2 101 = select 2, skip 2

BIT	Description
12	Crossbar switch (output multiplexer) control bit initial value. This initial value is clocked into the crossbar switch at a SYNC_YR rising edge pulse (when the array pointers jump back to row 1). The crossbar switch control bit selects the correspondence between multiplexer busses and output amplifiers. Bus-to-output correspondence is according to the following table: **Bus** / **when bit set to 0** / **when bit set to 1** 1 / output 1 / output 2 2 / output 2 / output 1 3 (4 outputs) / output 3 / output 4 4 (4 outputs) / output 4 / output 3
13	1 = Toggle crossbar switch control bit on every odd/even line. In order to let green pixels always use the same output amplifier automatically, this bit must be set to 1. On every CLK_Y rising edge (when a new row is selected), the crossbar switch control bit will toggle. Initial value (after SYNC_Y) is set by bit 12.
14	Not used.
15 (MSB)	1=Power up sensor array ; 0 = Power down

3 pins are used for the serial data interface. This interface converts the serial data into an (internal) parallel data bus (Serial-Parallel Interface or SPI). The control lines are:

- DATA : the data input. LSB is clocked in first.
- CLK : clock, on each rising edge, the value of DATA is clocked in
- CS : chip select, a rising edge on CS loads the parallelized data into the on-chip register.

The initial state of the register is undefined. However, no state exists that destroys the device.

5. Pin configuration

Table 13 lists the pin configuration of the IBIS4-14000. Figure 9 shows the assignment of pin numbers on the package.

Table 13: Pin list

Pin nr.	Name	Function	Comment
1	OBIAS	Bias current output amplifiers.	Connect with 20kΩ to VDD and decouple with 100 nF to GND.
2	GND	Ground for output 3.	
3	OUT3	Output 3.	
4	GND	Ground for output 4.	
5	OUT4	Output 4.	
6	VDD	Power supply.	Nominal 3.3 V
7	GND	Ground.	0 V
8	OUT2	Output 2.	
9	GND	Ground for output 2.	
10	OUT1	Output 1.	
11	GND	Ground for output 1.	
12	DARKREF	Offset level of output signal.	Typ. 2.6 V. min. 1.7 V max. 3 V
13	TEMP1	Temperature sensor. Located near the output amplifiers (pixel 4536, 0) near the stitch line).	Any voltage above GND forward biases the diode. Connect to GND if not used.
14	PHDIODE	Photodiode output. Yields the equivalent photocurrent of 250 x 50 pixels. Diode is located right under the pad.	Reverse biased by any voltage above GND Connect to GND if not used.
15	CLK_Y	Y clock for switchboard.	Clocks on rising edge Connect to CLK_YL (or drive identically)
16	SYNC_Y	Y SYNC pulse for switchboard.	Low active: synchronous sync on rising edge of CLK_Y Connect to SYNC_YL (or drive identically)
17	TEMP2	Temperature sensor. Located near pixel (24,0).	Any voltage above GND forward biases the diode. Connect to GND if not used.

Pin nr.	Name	Function	Comment
18	GNDAB	Anti-blooming reference level (=pin 33).	Typ. 0 V. Set to 1.5 V for improved anti-blooming.
19	GND	Ground.	0 V
20	VDD	Power supply.	Nominal 3.3 V
21	VDDR	Power supply for reset line drivers =	Nominal 4 V Connected on-chip to pin 30
22	CLK_YR	Clock of YR shift register.	Shifts on rising edge.
23	SYR	Activate YR shift register for driving of reset and select line of pixel array.	High active. Exact pulsing pattern see timing diagram. Both SYR = 1 and SYL = 1 is not allowed, except when the same row is selected!
24	SYNC_YR	Sets the YR shift register to row 1.	Low active. Synchronous sync on rising edge of CLK_YR 200 ns setup time
25	VDDARRAY	Pixel array power supply (= pin 26).	3 V
26	VDDARRAY	Pixel array power supply (= pin 25).	3 V
27	SYNC_YL	Sets the YL shift register to row 1.	Low active. Synchronous sync on rising edge of CLK_YL 200 ns setup time.
28	SYL	Activate YL shift register for driving of reset and select line of pixel array.	High active. Exact pulsing pattern see timing diagram. Both SYR = 1 and SYL = 1 is not allowed, except when the same row is selected!
29	CLK_YL	Clock of YL shift register.	Shifts on rising edge.
30	VDDR	Power supply for reset line drivers.	Nominal 4 V. Connected on-chip to pin 21.
31	VDD	Power supply.	Nominal 3.3 V
32	GND	Ground.	0 V
33	GNDAB	Anti-blooming reference level (=pin 33).	Typ. 0 V. Set to 1V for improved anti-blooming.
34	SELECT	Control select line of pixel array.	High active. See timing diagrams.
35	RESET	Reset of the selected row of pixels.	High active. See timing diagrams.
36	CBIAS	Bias current column	Connect with 22 kΩ to VDD

Pin nr.	Name	Function	Comment
		amplifiers.	and decouple with 100 nF to GND.
37	PCBIAS	Bias current.	Connect with 22 kΩ to VDD and decouple with 100 nF to GND.
38	DIN	Serial data input.	16-bit word. LSB first.
39	SCLK	SPI interface clock.	Shifts on rising edge.
40	CS	Chip select.	Data copied to registers on rising edge.
41	PC	Row initialization pulse.	See timing diagrams.
42	SYNC_X	Sets the X shift register to row 1.	Low active. Synchronous sync on rising edge of CLK_X 150 ns setup time.
43	GND	Ground.	0 V
44	VDD	Power supply.	Nominal 3.3 V
45	CLK_X	Clock of YR shift register.	Shifts on rising edge.
46	SHR	Row track & hold reset level (1=hold; 0=track).	See timing diagram.
47	SHS	Row track & hold signal level (1=hold; 0=track).	See timing diagram.
48	XBIAS	Bias current X multiplexer.	Connect with 10 kΩ to VDD and decouple with 100 nF to GND.
49	ABIAS	Bias current pixel array.	Connect with 10 MΩ to VDD and decouple with 100 nF to GND. NOT USED. MAY ALSO BE DISCONNECTED OR GROUNDED

6. Geometry & mechanical

6.1 Die geometry

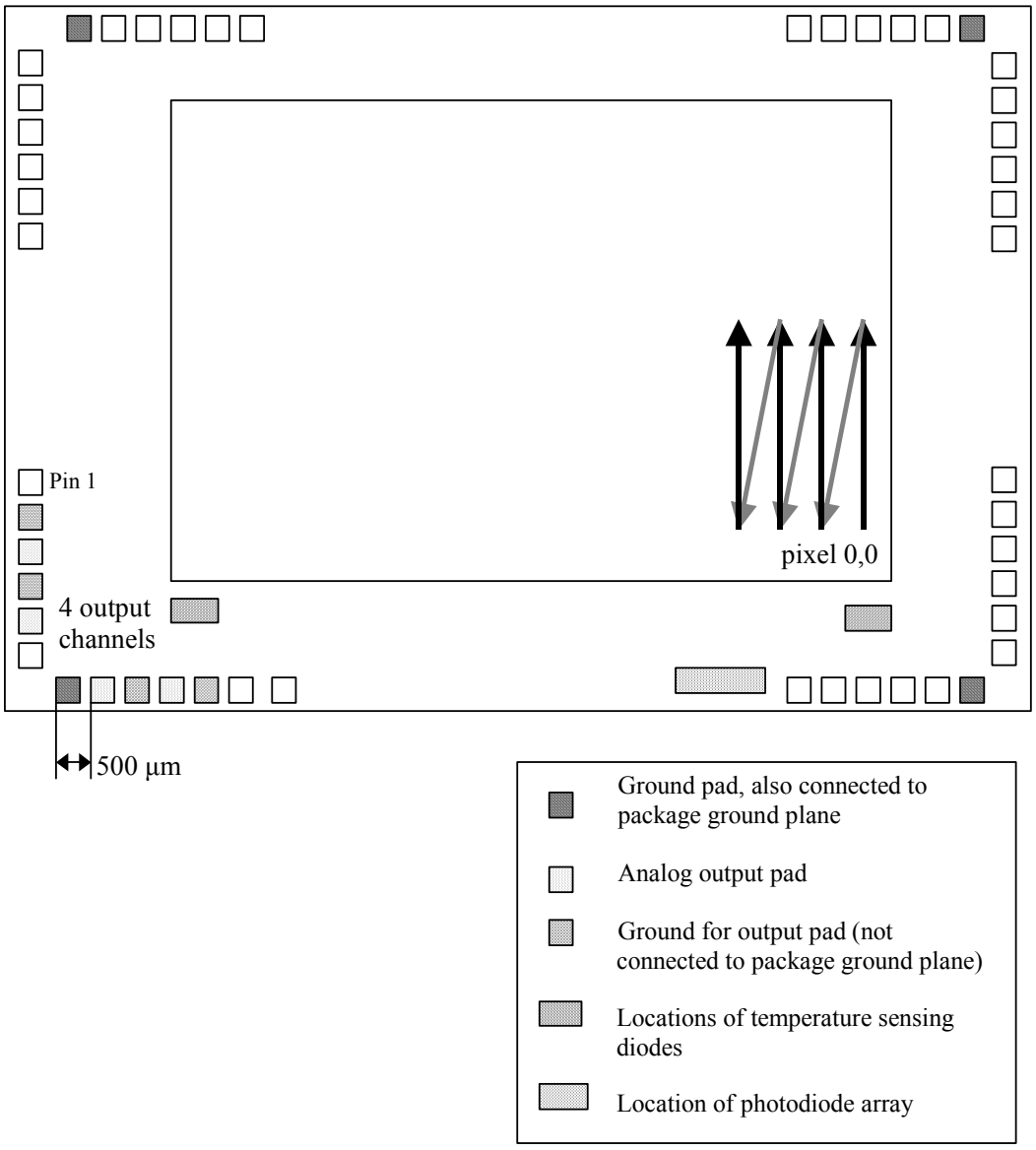


Figure 9: Die geometry and location of pixel (0,0)

6.2 Pin number assignment

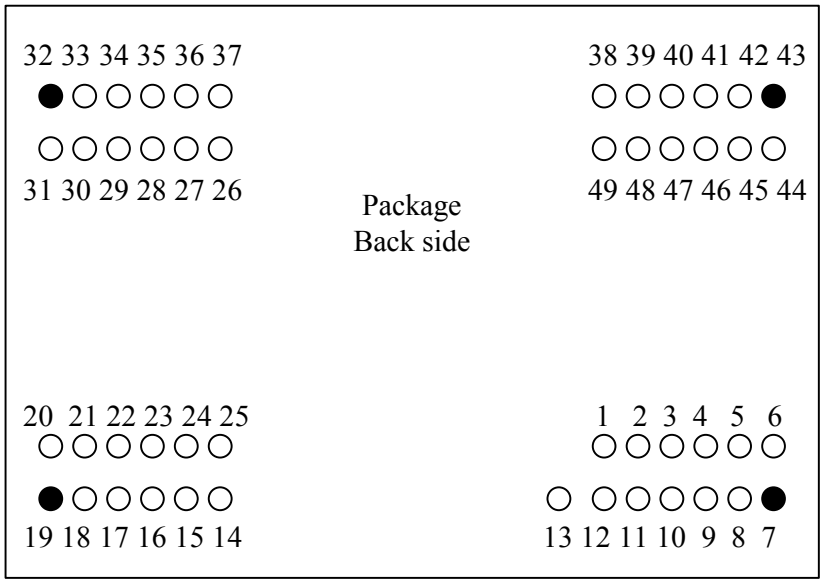
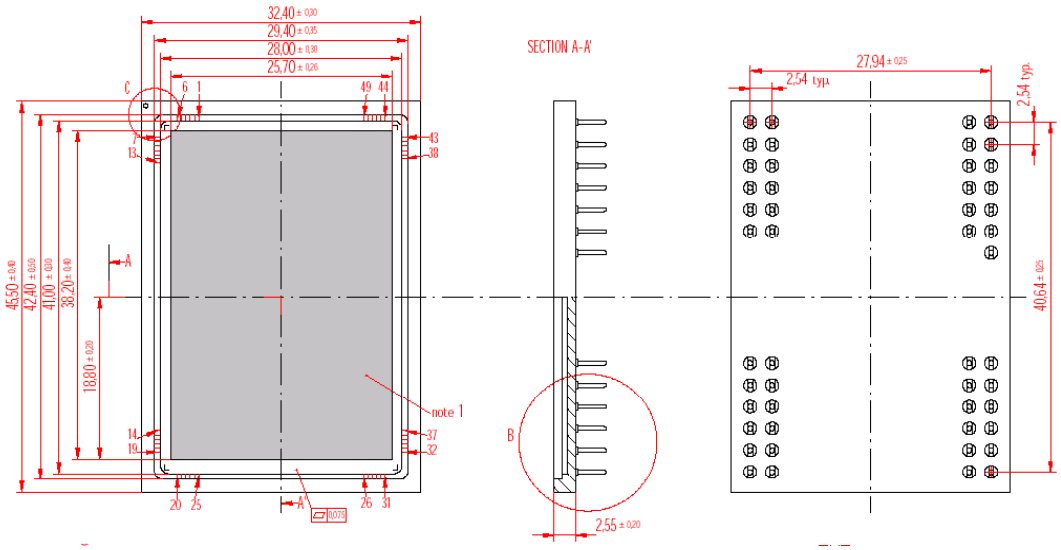
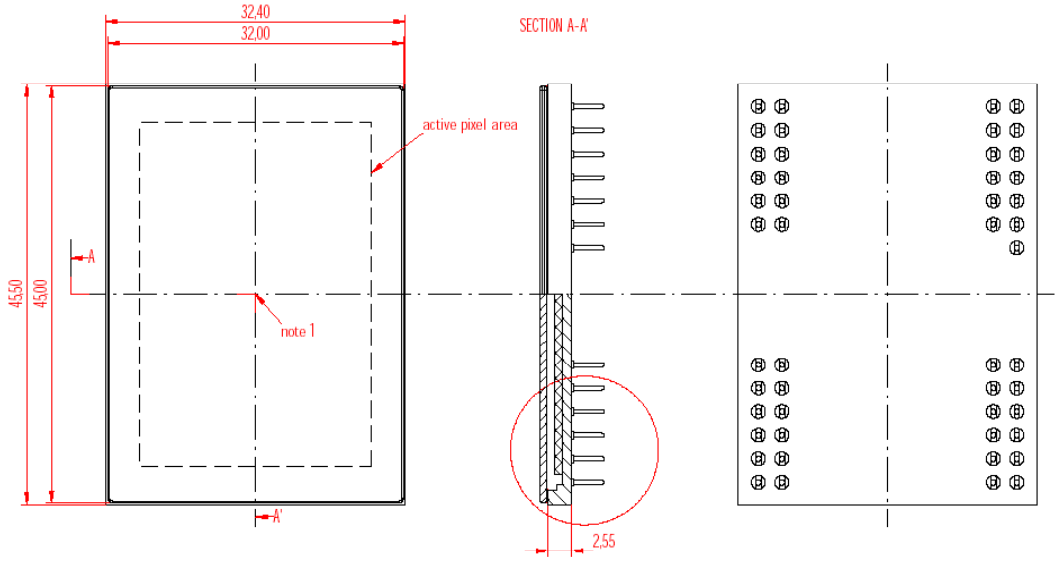


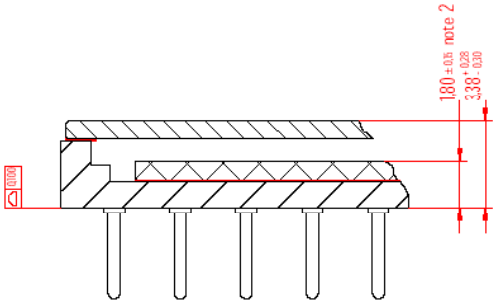
Figure 10: pin number assignment. "Solid" drawn pins are connected to die attach area for a proper ground plane.

6.3 Package drawings



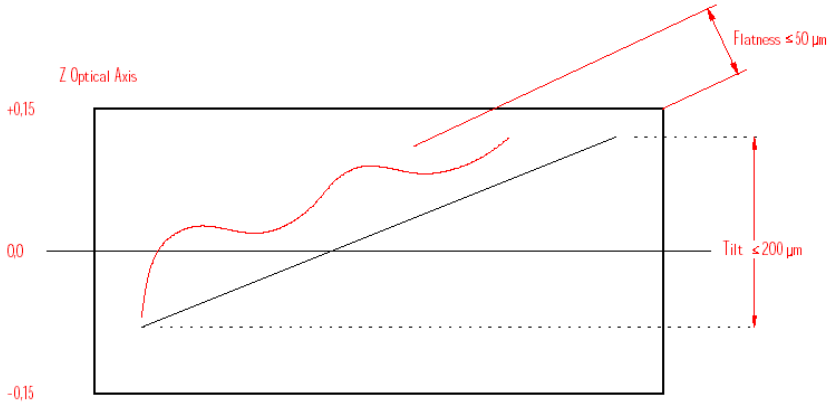
6.4 Die placement dimensions and accuracy





note:
1. CL of the active pixel area to be ±0,13 in the X & Y of CL of the package
   CL of the coverglass to be ±0,30 in the X & Y of CL of the package
2. Flatness and tilt of die surface (sheet 3)
3. Barcode label 128B, max 100 µm on the bottom of package

all dimensions in mm



6.5 Cover glass

Schott D-263 plain glass will be as cover glass of the IBIS4-14000.

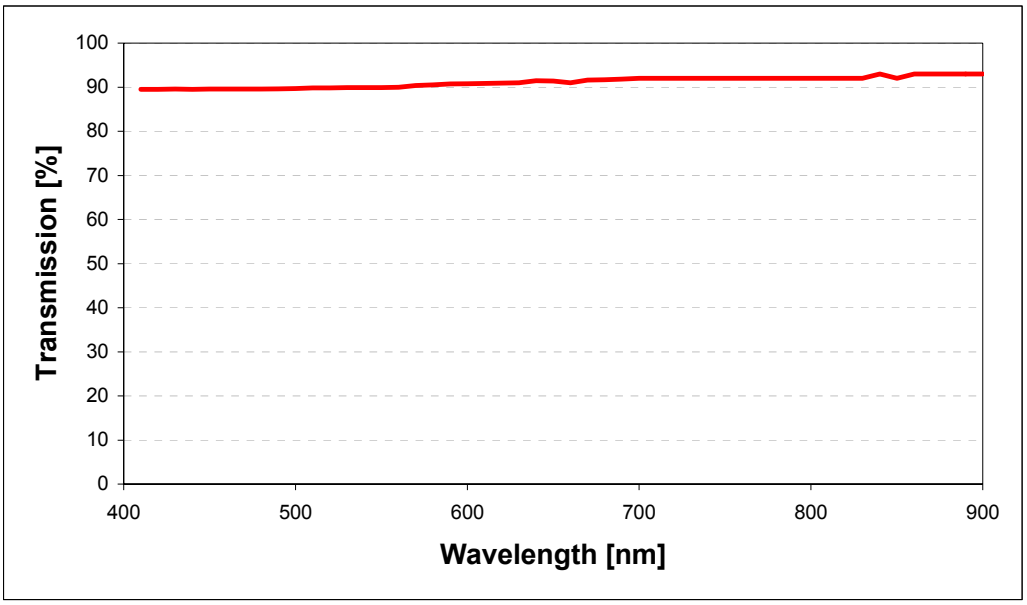


Figure 10: D-263 transmittance curve

7. Ordering Information

Table 14: FillFactory and Cypress part numbers

FillFactory Part Number	*Cypress Semiconductor Part Number*
IBIS4-14000-C	CYII4SC014KAA-GAC – (Preliminary)
IBIS4-14000-M	CYII4SM014KAA-GBC – (Preliminary)

Disclaimer

FillFactory image sensors are only warranted to meet the specifications as described in the production data sheet. FillFactory reserves the right to change any information contained herein without notice.

Please contact info@FillFactory.com for more information.

Document History Page

Document Title: IBIS4-14000 14M Pixel Rolling Shutter CMOS Image Sensor

Document Number: 38-05709

Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	310213	See ECN	SIL	Initial Cypress release

(EOD)