FAIRCHILD SEMICONDUCTOR™

August 1986
Revised April 2000

DM74LS169A
Synchronous 4-Bit Up/Down Binary Counter

General Description

This synchronous presettable counter features an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs all change at the same time when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising edge of the clock waveform.

This counter is fully programmable; that is, the outputs may each be preset either HIGH or LOW. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry permits cascading counters for n-bit synchronous applications without additional gating. Both count-enable inputs ($\overline{P}$ and $\overline{T}$) must be LOW to count. The direction of the count is determined by the level of the UP/DOWN input. When the input is HIGH, the counter counts UP; when LOW, it counts DOWN. Input $\overline{T}$ is fed forward to enable the carry outputs. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting UP, and approximately equal to the low portion of the Q_A output when counting DOWN. This low-level overflow carry pulse can be used to enable successively cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode clamped to minimize transmission-line effects, thereby simplifying system design.

This counter features a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, UP/DOWN), which modify the operating mode, have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

Features

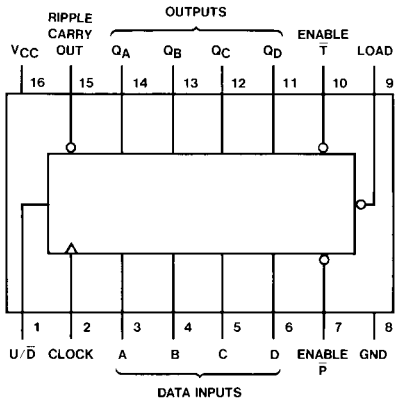
- Fully synchronous operation for counting and programming.
- Internal look-ahead for fast counting.
- Carry output for n-bit cascading.
- Fully independent clock circuit

Ordering Code:

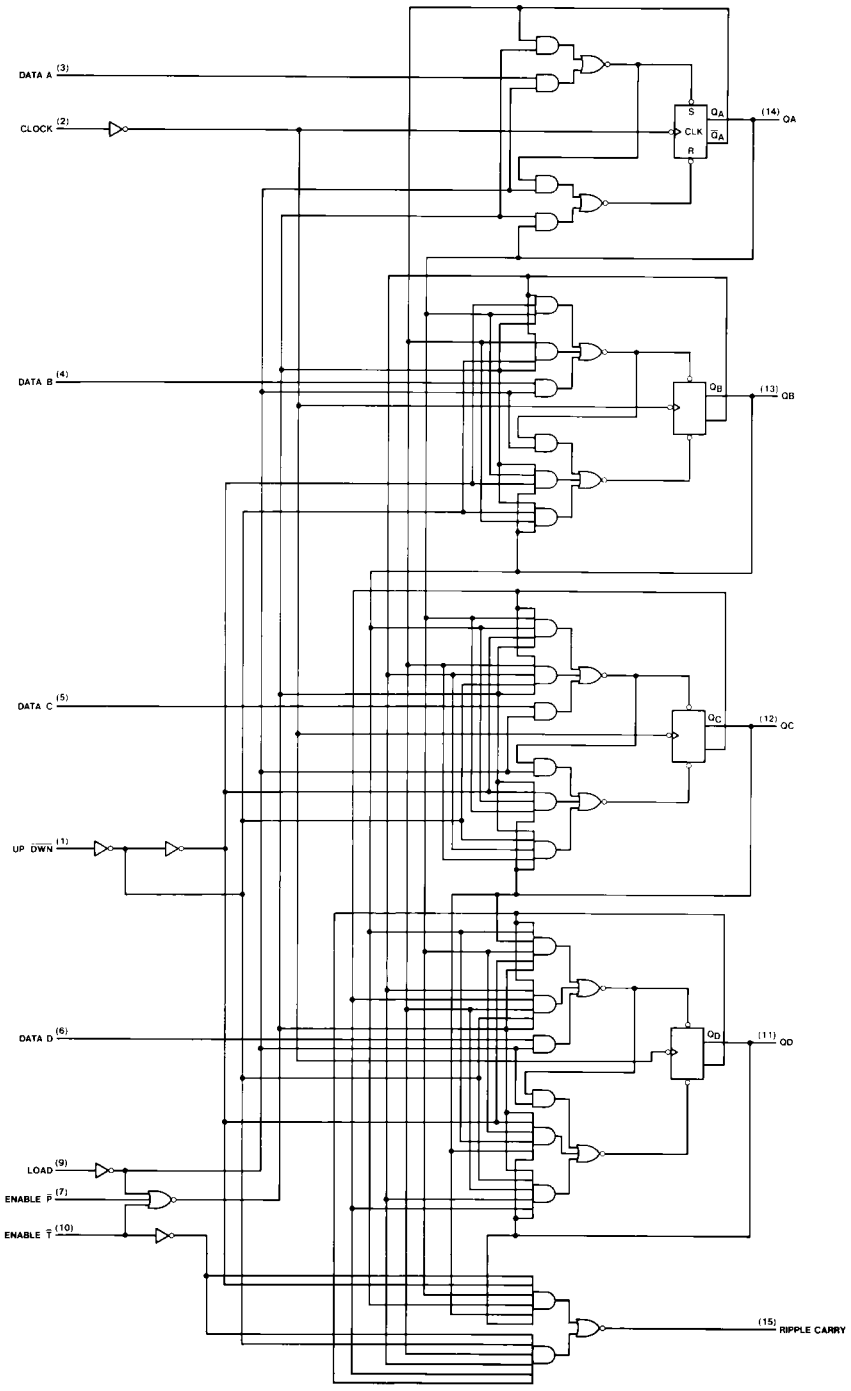
Order Number	Package Number	Package Description
DM74LS169AM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS169AN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

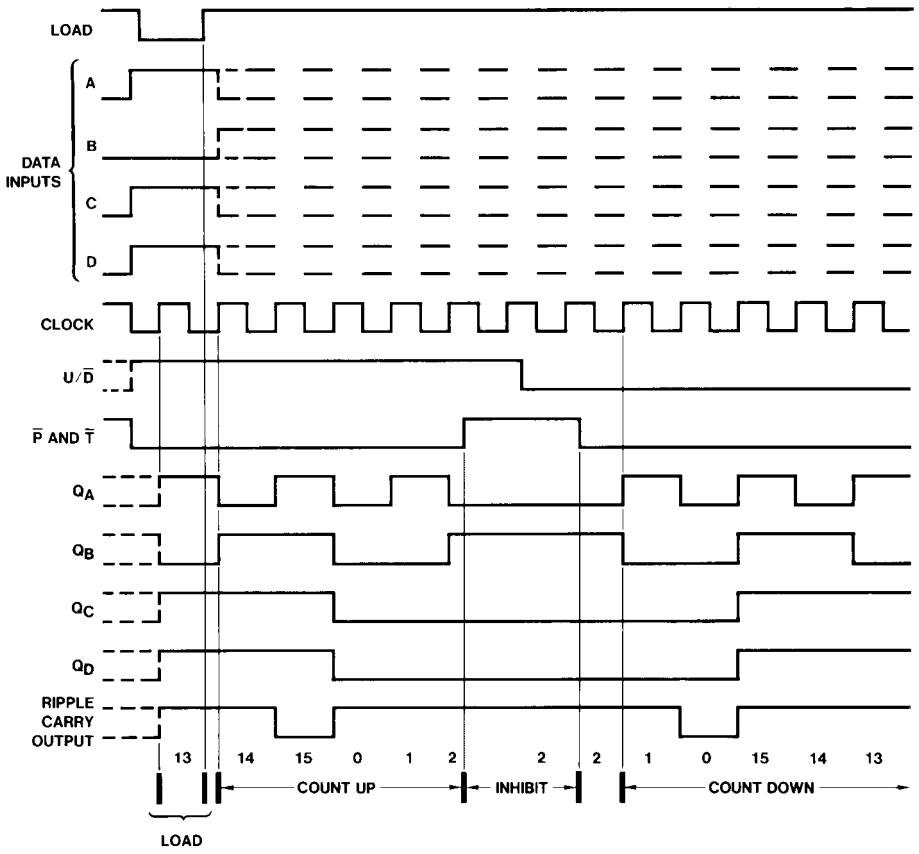
Connection Diagram



Logic Diagram



Timing Diagram



Typical Load, Count, and Inhibit Sequences

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current				−0.4	mA
I_{OL}	LOW Level Output Current				8	mA
f_{CLK}	Clock Frequency (Note 2)		0		25	MHz
	Clock Frequency (Note 3)		0		20	MHz
t_W	Clock Pulse Width (Note 4)		25			ns
t_{SU}	Setup Time (Note 4)	Data	20			ns
		Enable $\overline{T}$ or $\overline{P}$	20			
		Load	25			
		U/D	30			
t_H	Hold Time (Note 4)		0			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 2: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 4: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 5)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 7V	Enable $\overline{T}$			0.2	mA
			Others			0.1	
I_{IH}	HIGH Level Input Current	V_{CC} = Max V_I = 2.7V	Enable $\overline{T}$			40	μA
			Others			20	
I_{IL}	LOW Level Input Current	V_{CC} = Max V_I = 0.4V	Enable $\overline{T}$			−0.8	mA
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 6)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 7)			20	34	mA

Note 5: All typicals are at V_{CC} = 5V and T_A = 25°C.

Note 6: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 7: I_{CC} is measured after a momentary 4.5V, then ground, is applied to the CLOCK with all other inputs grounded and all the outputs OPEN.

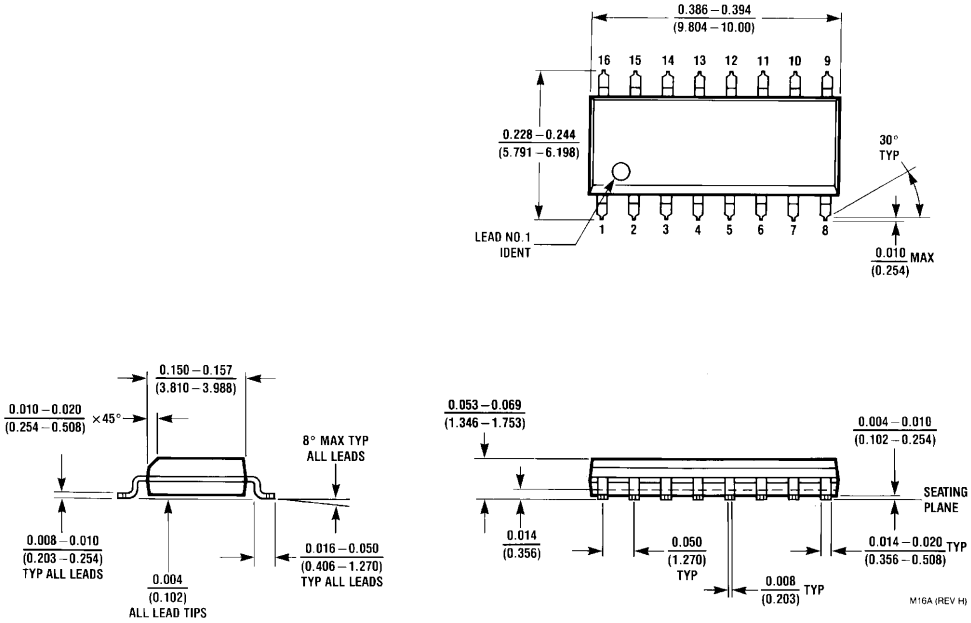
Switching Characteristic

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Ripple Carry		35		39	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Ripple Carry		35		44	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Any Q		20		24	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Any Q		23		32	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Enable $\overline{T}$ to Ripple Carry		18		24	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Enable $\overline{T}$ to Ripple Carry		18		28	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Up/Down to Ripple Carry (Note 8)		25		30	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Up/Down to Ripple Carry (Note 8)		29		38	ns

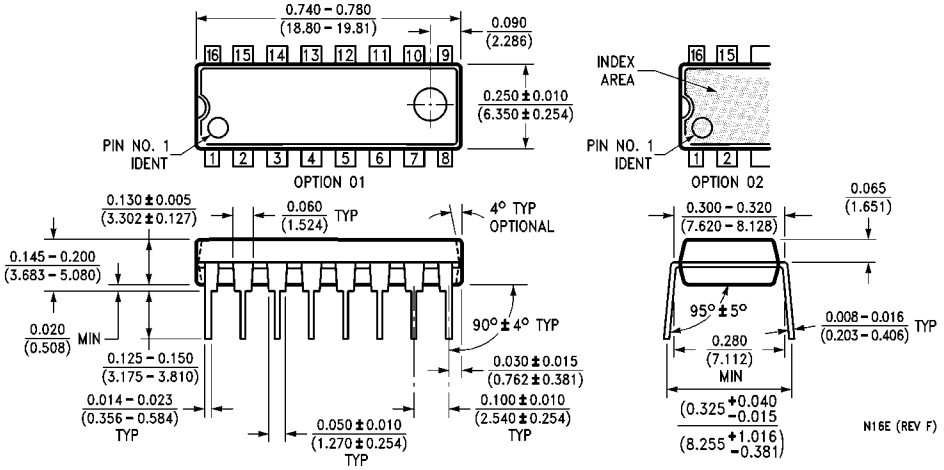
Note 8: The propagation delay from UP/DOWN to RIPPLE CARRY must be measured with the counter at either a minimum or a maximum count. As the logic level of the UP/DOWN input is changed, the ripple carry output will follow. If the count is minimum, the RIPPLE CARRY output transition will be in phase. If the count is maximum, the RIPPLE CARRY output will be out of phase.

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E