

DrMOS Product Family

DrMOS 5x5
TDA21231

Data Sheet

Rev. 2.2
Final

Power Management and Multimarket



1 Applications

- Desktop and Server VR buck-converter
- Single Phase and Multiphase POL
- CPU/GPU Regulation in Notebook, Desktop Graphics Cards, DDR Memory, Graphic Memory
- High Power Density Voltage Regulator Modules (VRM)

2 Features

- For synchronous buck converter step down voltage applications
- Maximum average current of 55 A
- Input voltage range +4.5 V to +16 V
- Power MOSFETs rated 25 V
- Fast switching technology for improved performance at high switching frequencies (> 500 kHz)
- Remote driver disable function
- Includes bootstrap diode
- Undervoltage lockout
- Shoot through protection
- +5 V high side and low side MOSFETs driving voltage
- Compatible to standard +3.3 V PWM controller integrated circuits
- Tri-state PWM input functionality
- Small package: PG-IQFN-31-2 (5 x 5 x 0.8 mm³)
- RoHS compliant
- Thermal warning

Table 1 Product Identification

| Part Number | Temp Range | Package | Marking |
|-------------|--------------|---|---------|
| TDA21231 | -40 to 125°C | PG-IQFN-31-2 (5 x 5 x 0.8 mm ³) | DA21231 |

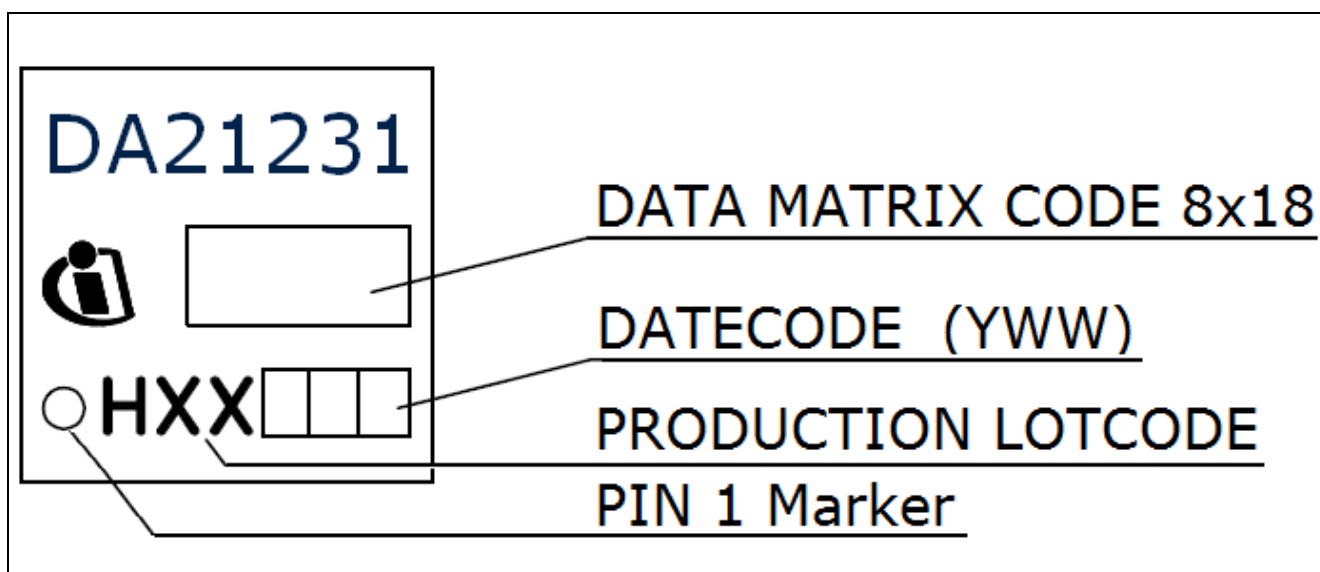


Figure 1 Picture of the Product

3 Description

3.1 Pinout

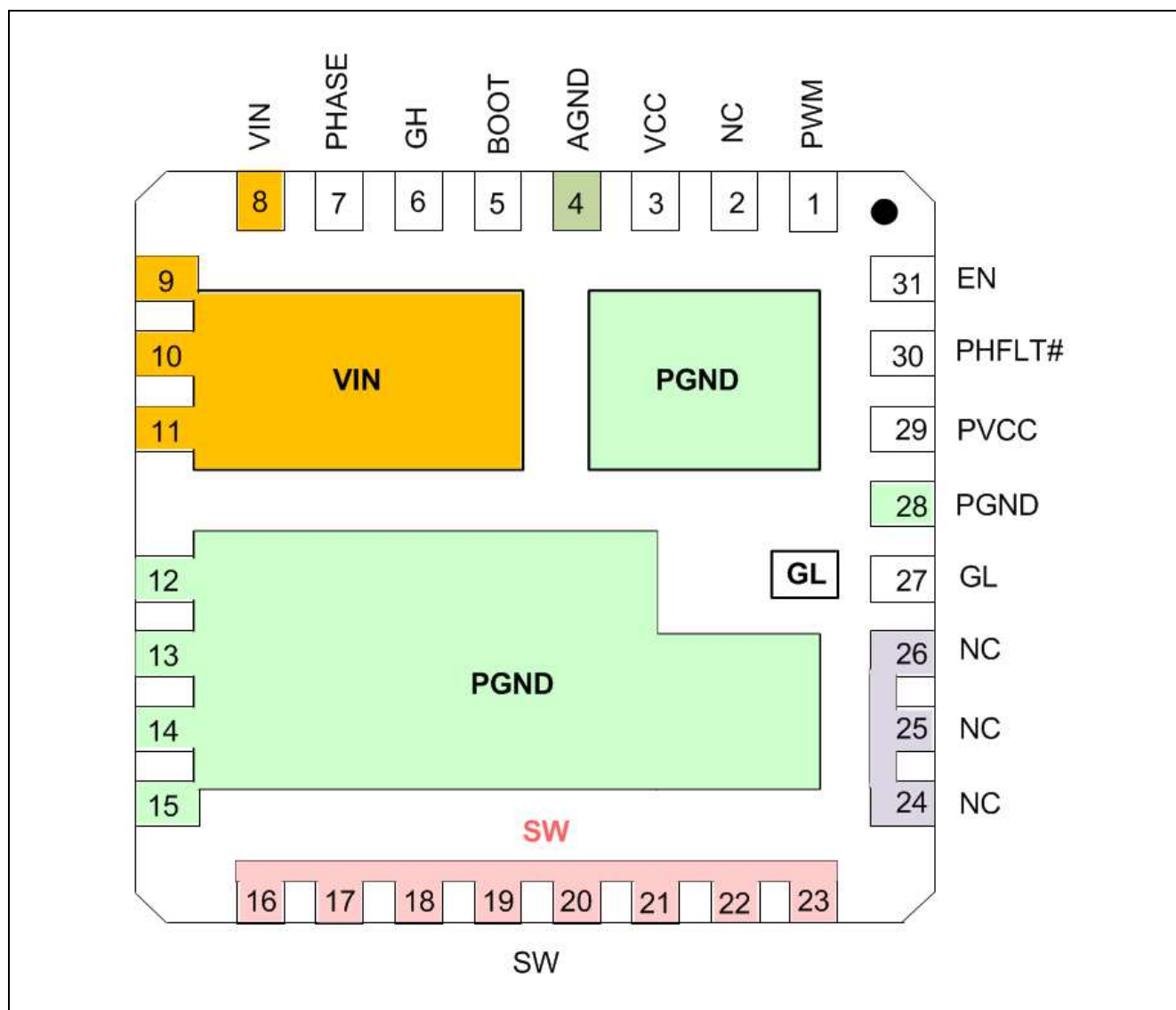


Figure 2 Pinout, Numbering and Name of Pins (transparent top view)

**Table 2 I/O Signals**

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---------|--------|----------|--------------|---|
| 1 | PWM | I | +3.3 V logic | PWM drive logic input The tri-state PWM input is compatible with 3.3 V. |
| 5 | BOOT | I | Analog | Bootstrap voltage pin Connect to BOOT capacitor |
| 6 | GH | O | Analog | High-Side Gate Test point for High Side MOSFET gate signal |
| 7 | PHASE | I | Analog | Switch node (reference for Boot voltage) internally connected to SW pin, connect to BOOT capacitor |
| 16 – 23 | SW | O | Analog | Switch node output High current output switching node |
| 27 | GL | O | Analog | Low-Side Gate Test point for Low Side MOSFET gate signal |
| 30 | PHFLT# | O | +3.3 V logic | Thermal Warning Connect through a resistor to 3.3V. When the thermal protection threshold is tripped, the PHFLT# pin is being pulled low. Leave open if not used. |
| 31 | EN | I | +3.3 V logic | Enable signal (active high) Connect to GND to disable the IC. |

Table 3 Power Supply

| Pin No. | Name | Pin Type | Function |
|------------------|------|----------|--|
| 8 to 11, Vin pad | VIN | POWER | Input voltage Supply of the drain of the high-side MOSFET |
| 29 | PVCC | POWER | FET gate supply voltage High- and low-side gate drive supply |
| 3 | VCC | POWER | Logic supply voltage Bias voltage for the internal logic |

Table 4 Ground Pins

| Pin No. | Name | Pin Type | Function |
|---------------------------|------|----------|--|
| 4 | AGND | GND | Control signal ground Should be connected to PGND externally |
| 12 – 15, 28, PGND pads | PGND | GND | Power ground All these pins must be connected to the power GND plane through multiple low inductance vias. |

Table 5 Not Connected

| Pin No. | Name | Pin Type | Function |
|------------|------|----------|--|
| 2 | NC | – | No internal connection Leave pin floating or tie to noise-free voltage of 0 (GND) ... 7 V. |
| 24, 25, 26 | NC | – | No internal connection Options: Leave floating, tie to GND or SW |

3.2 General Description

The Infineon TDA21231 is a multichip module that incorporates Infineon's premier MOSFET technology for a single high-side and a single low-side MOSFET coupled with a robust, high performance, high switching frequency gate driver in a single PG-IQFN-31-2 package. The optimized gate timing allows for significant light load efficiency improvements over discrete solutions.

When combined with Infineon's family of digital multi-phase controllers, the TDA21231 forms a complete core-voltage regulator solution for advanced micro and graphics processors as well as point-of-load applications.

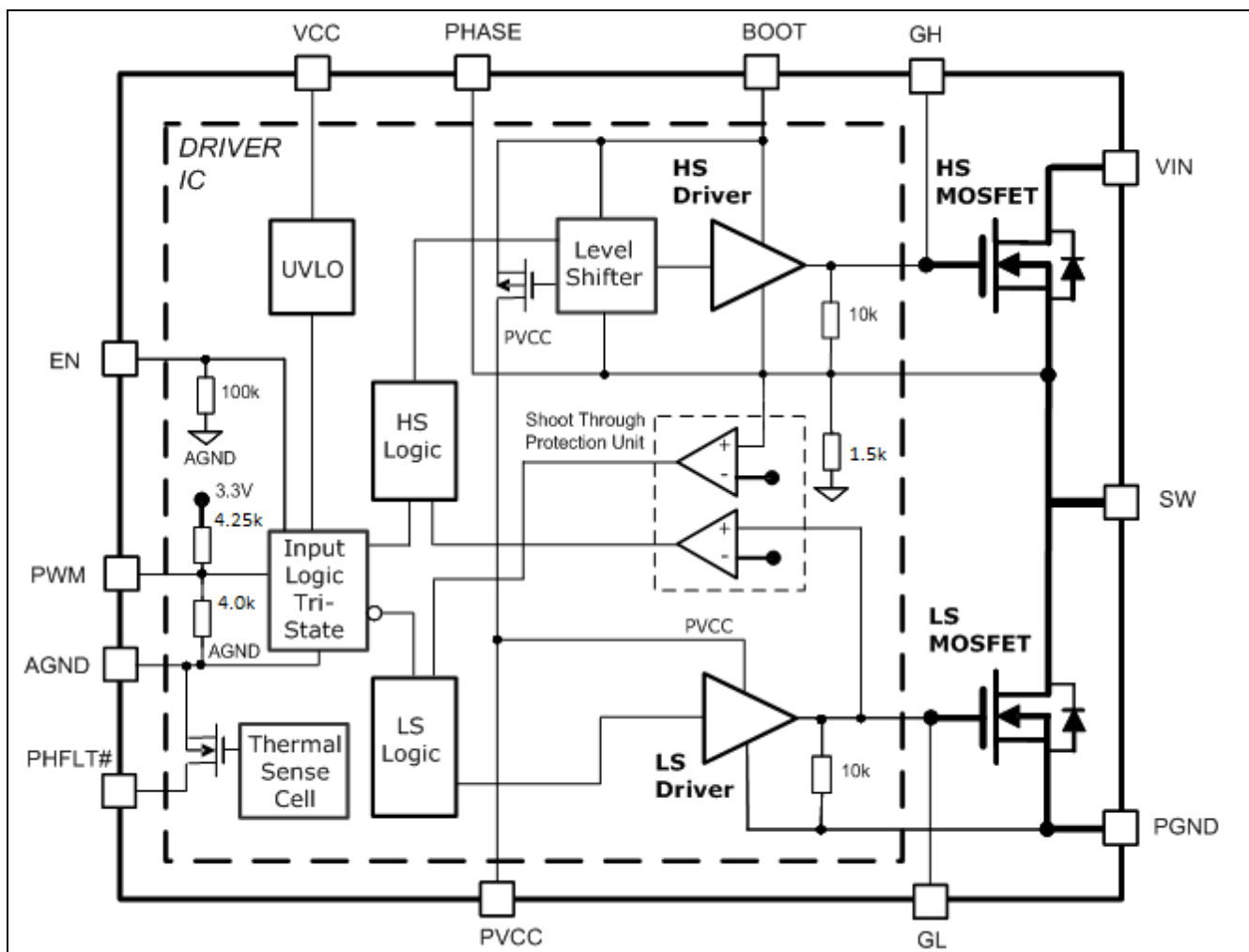


Figure 3 Simplified Block Diagram



4 Electrical Specification

4.1 Absolute Maximum Ratings

Note: $T_A = 25^\circ\text{C}$

Stresses above those listed in Table 6 “Absolute Maximum Ratings” may cause permanent damage to the device. These are absolute stress ratings only and operation of the device is not implied or recommended at these or any other conditions in excess of those given in the operational sections of this specification. Exposure over values of the recommended ratings (Table 8) for extended periods may adversely affect the operation and reliability of the device.

Table 6 Absolute Maximum Ratings

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-----------------------------------|---|-----------------|------|-----------------|------------------|--|
| | | Min. | Typ. | Max. | | |
| Maximum average load current | I_{OUT} | – | – | 55 | A | |
| Input Voltage | V_{IN} (DC) | -0.30 | – | 21 | V | |
| Logic supply voltage | V_{VCC} (DC) | -0.30 | – | 8 | | |
| High- and low-side driver voltage | V_{PVCC} (DC) | -0.30 | – | 8 | | |
| Switch node voltage | V_{SW} (DC) | -1 | – | 25 | | |
| | V_{SW} (AC) | -8 ¹ | – | – | | |
| PHASE node voltage | V_{PHASE} (DC) | -1 | – | 25 | | |
| | V_{PHASE} (AC) | -8 ¹ | – | – | | |
| MOSFET voltage spike | $V_{\text{IN}} - V_{\text{PHASE}}$ (AC) | – | – | 32 ² | | 2 ns above 25 V |
| | $V_{\text{PHASE}} - V_{\text{PGND}}$ (AC) | – | – | 32 ² | | |
| BOOT voltage | V_{BOOT} (DC) | -0.3 | – | 25 | | |
| | V_{BOOT} (AC) | – | – | 30 ¹ | | |
| | $V_{\text{BOOT-PHASE}}$ (DC) | -0.3 | – | 8 | | |
| EN voltage | V_{EN} | -0.3 | – | 4 | | Maximum value valid for operation up to 1h accumulated over lifetime, else the maximum value is 3.6V |
| PWM voltage | V_{PWM} | -0.3 | – | 4 | | |
| PHFLT# | $V_{\text{PHFLT\#}}$ | -0.3 | – | 4 | | |
| Junction temperature | T_{Jmax} | -40 | – | 150 | $^\circ\text{C}$ | |
| Storage temperature | T_{STG} | -55 | – | 150 | | |

Note: All rated voltages are relative to voltages on the AGND and PGND pins unless otherwise specified.

¹ AC is limited to 10 ns

² AC is limited to 2 ns



4.2 Thermal Characteristics

Table 7 Thermal Characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|------------------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Thermal resistance to case (soldering point) | θ_{JC} | – | – | 2 | K/W | – |
| Thermal resistance to top of package | θ_{JCtop} | – | – | 30 | | – |
| Thermal resistance to ambient ($P_{loss} = 4.5\text{ W}$, $T_A = 70\text{ °C}$, 8 layer server board with 2 oz copper per layer) | θ_{JA} | – | 11.5 | – | | Still air |
| | | – | 8.9 | – | | 200 lfm airflow |
| | | – | 8.8 | – | | 300 lfm airflow |

4.3 Recommended Operating Conditions and Electrical Characteristics

Note: $V_{DRV} = V_{CIN} = 5\text{ V}$, $T_A = 25\text{ °C}$

Table 8 Recommended Operating Conditions

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-----------------------|------------|--------|------|-----------------|------|-------------------------------------|
| | | Min. | Typ. | Max. | | |
| Input voltage | V_{IN} | 5 | – | 16 ³ | V | For telecom applications see note 3 |
| MOSFET driver voltage | V_{PVCC} | 4.5 | 5 | 7 | | |
| Logic supply voltage | V_{VCC} | 4.5 | 5 | 7 | | |
| Frequency of the PWM | f_{SW} | – | – | 1.2 | MHz | |
| Junction temperature | T_{JOP} | -40 | – | 125 | °C | |

³ In telecom applications the recommended maximum voltage for V_{IN} is 13.2V unless a boot resistor is used (see Figure 6) to limit the voltage spike $V_{PHASE}-V_{PGND}$ (AC) to 26V.

**Table 9 Voltage Supply And Biasing Current**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|----------------------|---------------------|--------|------|------|---------|--------------------------------|
| | | Min. | Typ. | Max. | | |
| UVLO BOOT rising | $V_{UVLOBOOT_R}$ | – | 4.0 | – | V | $V_{BOOT}-V_{SW}$ rising |
| UVLO BOOT falling | $V_{UVLOBOOT_F}$ | – | 3.8 | – | | $V_{BOOT}-V_{SW}$ falling |
| UVLO rising | V_{UVLO_R} | – | – | 4.2 | V | VCC rising |
| UVLO falling | V_{UVLO_F} | 3.7 | – | – | | VCC falling |
| Driver current | I_{PVCC_300kHz} | – | 12.5 | – | mA | EN = 3.3 V, $f_{SW} = 300$ kHz |
| | I_{PVCC_1MHz} | – | 42 | – | | EN = 3.3 V, $f_{SW} = 1$ MHz |
| | I_{PVCC_PWML} | – | 710 | – | μA | EN = 3.3 V, PWM = 0V |
| | I_{PVCC_PWMH} | – | 210 | – | | EN = 0V, PWM=3.3V, |
| IC current (control) | I_{VCC_PWML} | – | 1 | – | mA | EN = 3.3 V, PWM = 0 V |
| | I_{VCC_O} | – | 630 | – | | EN = 3.3 V, PWM = Open |
| IC quiescent | $I_{CC} + I_{PVCC}$ | – | 840 | – | μA | EN = 0V, PWM = Open |
| Pre-Bias at SW | V_{SW_0} | – | 160 | 180 | mV | VCC and PVCC present |

Table 10 Logic Inputs And Threshold

| Parameter | | Symbol | Values | | | Unit | Note / Test Condition |
|-----------|--|-------------------|--------|------|------|-------------|-----------------------|
| | | | Min. | Typ. | Max. | | |
| EN | Input low | V_{EN_L} | – | – | 0.8 | V | V_{EN} falling |
| | Input high | V_{EN_H} | 2.0 | – | – | | V_{EN} rising |
| | Sink current | I_{EN} | – | 10 | – | μA | $V_{EN} = 1$ V |
| PWM | Input low | V_{PWM_L} | – | – | 0.6 | V | V_{PWM} falling |
| | Input high | V_{PWM_H} | 2.6 | – | – | | V_{PWM} rising |
| | Input resistance | R_{IN-PWM} | – | 2 | – | k Ω | $V_{PWM} = 1$ V |
| | Open voltage | V_{PWM_O} | – | 1.6 | – | V | V_{PWM_O} |
| | Tri-state shutdown window ⁴ | V_{PWM_S} | 1.2 | – | 2.0 | | |
| PHFLT# | Warning Temperature ⁵ | $T_{PHFLT\#_T}$ | – | 140 | – | $^{\circ}C$ | |
| | Thermal warning accuracy ⁵ | $dT_{PHFLT\#_T}$ | -10 | – | 10 | K | |
| | Hysteresis ⁵ | $T_{PHFLT\#_H}$ | – | 10 | – | | |
| | On resistance | $R_{PHFLT\#_PD}$ | – | 37.5 | 80 | Ω | $I_{LOAD} = 8mA$ |
| | Leakage current | $I_{PHFLT\#_LK}$ | – | 0.1 | 5 | μA | |

⁴ Maximum voltage range for tri-state⁵ The thresholds for temperature warning are verified by design and not subject to production test.

**Table 11** Timing Characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|---------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| PWM tri-state to SW rising delay | t_pts | – | 15 | – | ns | |
| PWM tri-state to SW falling delay | t_pts2 | – | 15 | – | | |
| SW Shutdown hold-Off time from PWM low | t_tsshd | – | 50 | – | | |
| SW Shutdown hold-Off time from PWM high | t_tssh | – | 50 | – | | |
| PWM to SW turn-off propagation delay | t_pdlu | – | 20 | – | | |
| PWM to SW turn-on propagation delay | t_pdll | – | 10 | – | | |
| DR_EN turn-off propagation delay falling | t_pdl_DR_EN | – | 20 | – | | |
| DR_EN turn-on propagation delay rising | t_pdh_DR_EN | – | 20 | – | | |
| UVLO-BOOT-on time | t_UVLOBOOTon | – | 200 | – | | Pulse pattern issued to GL in UVLO-BOOT |
| UVLO-BOOT-off time | t_UVLOBOOToff | – | 200 | – | | |
| PWM minimum pulse width | ton_min_PWM | – | 25 | – | | When PWM change is recognized, the output remains in the new state for these minimum times. |
| PWM minimum off time | toff_min_PWM | – | 30 | – | | |

5 Theory of Operation

The TDA21231 incorporates a high performance gate driver, one high-side power MOSFET and one low-side power MOSFET in a single PG-IQFN-31-2 package. The advantages of this arrangement are found in the areas of increased performance, increased efficiency and lower overall package and layout inductance. This module is ideal for use in Synchronous Buck Regulators.

The power MOSFETs are optimized for 5 V gate drive enabling excellent high load and light load efficiency. The gate driver is a robust high-performance driver rated at the switching node for DC voltages ranging from -1 V to +21 V. The power density for transmitted power of this approach is approximately 90 W within a 25 mm² area.

5.1 Driver Characteristics

The gate driver of the TDA21231 has 2 voltage inputs, VCC and PVCC. VCC is the 5 V logic supply for the driver. PVCC sets the driving voltage for the high side and low side MOSFETs. The reference for the gate driver control circuit (VCC) is AGND. To decouple the sensitive control circuitry (logic supply) from a noisy environment a ceramic capacitor must be placed between VCC and AGND close to the pins. PVCC needs also to be decoupled using a ceramic capacitor (MLCC) between PVCC and PGND in close proximity to the pins. PGND serves as reference for the power circuitry including the driver output stage.

Referring to the block diagram page 4, VCC is internally connected to the UVLO circuit. It will force shut-down for insufficient VCC voltage. PVCC supplies the floating high-side drive – consisting of an active boot circuit - and the low side drive circuit. During undervoltage both GH and GL are driven low actively; further passive pull-down ($10\text{ k}\Omega$) is placed across gate-source of both FETs.

An additional UVLO circuitry, sensing the BOOT voltage level, is implemented to enable a recharge of the boot capacitor when its voltage is too low for a complete turn-on of the HS-MOSFET.

Proper response of the driver to the PWM signal is only guaranteed when UVLO and UVLO BOOT have been cleared by their respective supply voltages (Table 9). Therefore, it is strongly recommended to only issue pulses to PWM when no UVLO conditions are present. The power down sequence should set PWM to HiZ with regard to the internal threshold before ramping down VIN, PVCC and VCC respectively.

5.2 Inputs to the Internal Control Circuits

The **PWM** is the control input to the IC from an external PWM controller and is compatible with 3.3 V.

The PWM input has tri-state functionality. When the voltage remains in the specified PWM-shutdown-window for at least the PWM-shutdown-holdoff time t_{tsshd} , the operation will be suspended by keeping both MOSFET gate outputs low. Once left open, the pin is held internally at a level of $V_{\text{PWM}_O} = 1.6\text{ V}$ level.

Table 12 PWM Pin Functionality

| PWM logic level | Driver output |
|---|---------------------|
| Low | GL= High, GH = Low |
| High | GL = Low, GH = High |
| Open (left floating, or High impedance) | GL = Low, GH = Low |

The PWM threshold voltages V_{PMW_O} , V_{PWM_H} , V_{PWM_L} do not vary over the wide range of VCIN supply voltages (4.5 V to 8 V).

EN is an active high signal. When EN is being pulled low, the power stage will be disabled.

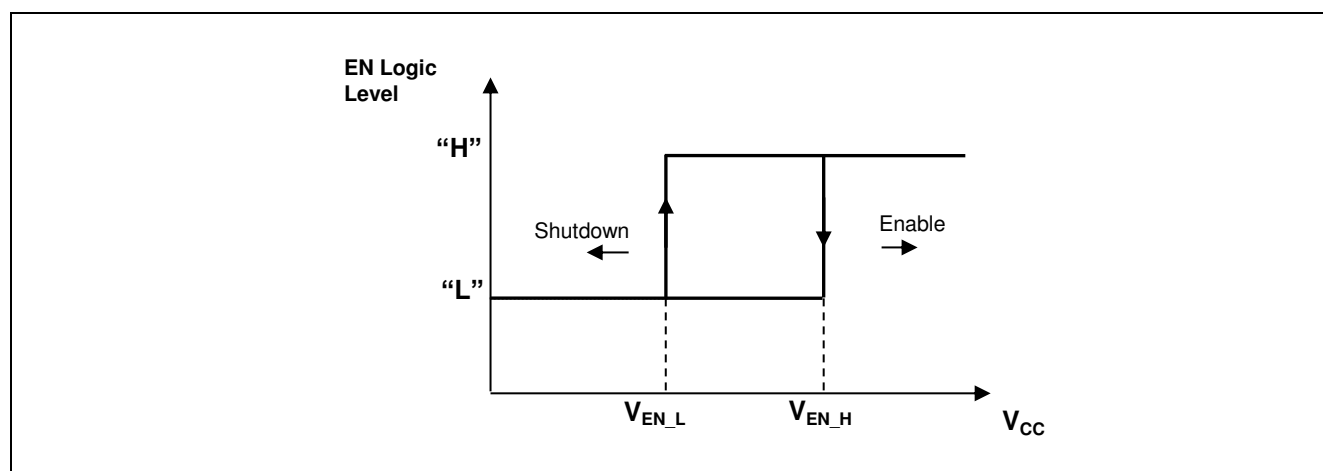


Figure 4 Enable (EN) signal logic levels

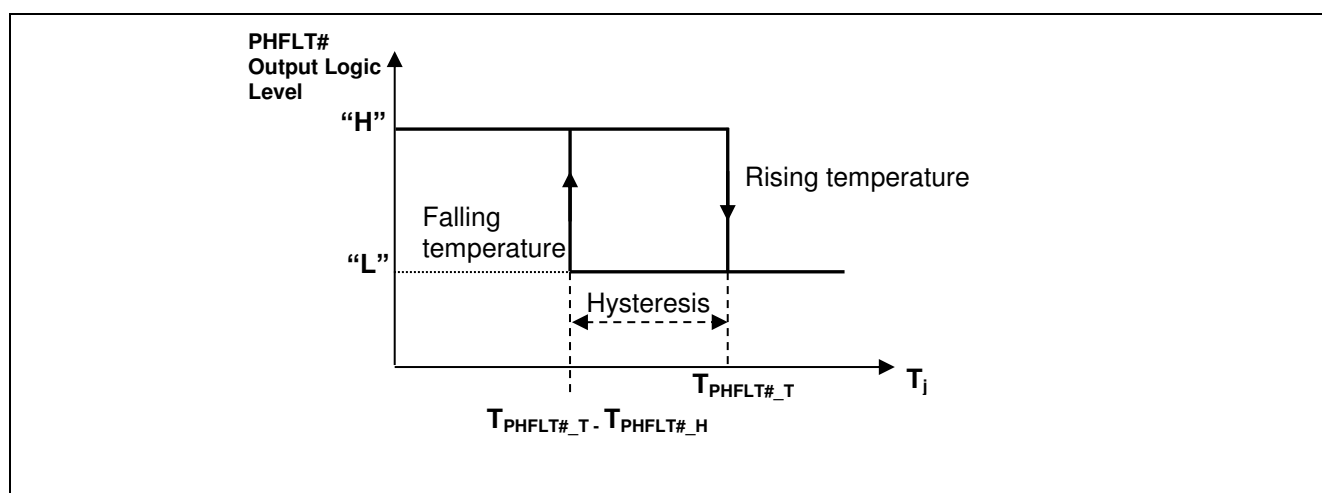
Table 13 EN Pin Functionality

| EN logic level | Driver output |
|---|-----------------------------------|
| Low | Shutdown : GL = GH = Low |
| High | Enable : GL = Active, GH = Active |
| Open (left floating, or High impedance) | Shutdown : GL = GH = Low |

5.3 Thermal protection

The **PHFLT#** pin is a digital monitoring output for the thermal warning. It does not affect the operation of the driver nor does it shut down the device.

When the driver junction temperature exceeds the thermal warning threshold of 140 °C (typ) the open drain output PHFLT# will be pulled low. Externally PHFLT# has to be connected to a supply (e.g. +3.3 V) by a resistor in the range of 10 kΩ. When the temperature of the driver junction decreases below the level of thermal warning threshold minus hysteresis (10 K typ.), the pin **PHFLT#** is released. $V_{PHFLT\#}$ is being pulled up by the external resistance. If the thermal warning feature is not used the pin can be left floating.

**Figure 5 Thermal warning**

5.4 Shoot Through Protection

The TDA21231 driver includes gate drive functionality to protect against shoot through. In order to protect the power stage from overlap, both high-side and low-side MOSFETs being on at the same time, the adaptive control circuitry monitors specific voltages. When the PWM signal transitions to low, the high-side MOSFET will begin to turn off after the propagation delay time t_{pdlu} . When V_{GS} of the high-side MOSFET is discharged below 1 V (a threshold below which the high-side MOSFET is off), a secondary delay t_{pdhl} is initiated. After that delay the low-side MOSFET turns on regardless of the state of the "SW" pin. It ensures that the converter can sink current efficiently and the bootstrap capacitor will be refreshed appropriately during each switching cycle. See Figure 8 for more detail.

5.5 UVLO – BOOT Protection

After long tristate conditions the voltage of the boot capacitor may be too small to completely enhance the HS-MOSFET when PWM enables GH directly after. Therefore, a monitoring circuit is being implemented to detect a lower threshold at which GH can safely be turned on. If the voltage across the boot capacitor has been dropping to this threshold a boot refresh circuit engages until an upper threshold has been reached.

The recharge is being done by intervals of repetitively pulling GL high for $t_{UVLOBOOTon}$ followed by $t_{UVLOBOOToff}$ driving GL low to reset the output current to zero. When the voltage across the boot capacitor has reached an upper threshold the recharge cycles stop.

The PWM input always takes priority over the boot refresh circuit when it is logic “H” or logic “L”.

6 Application

6.1 Implementation

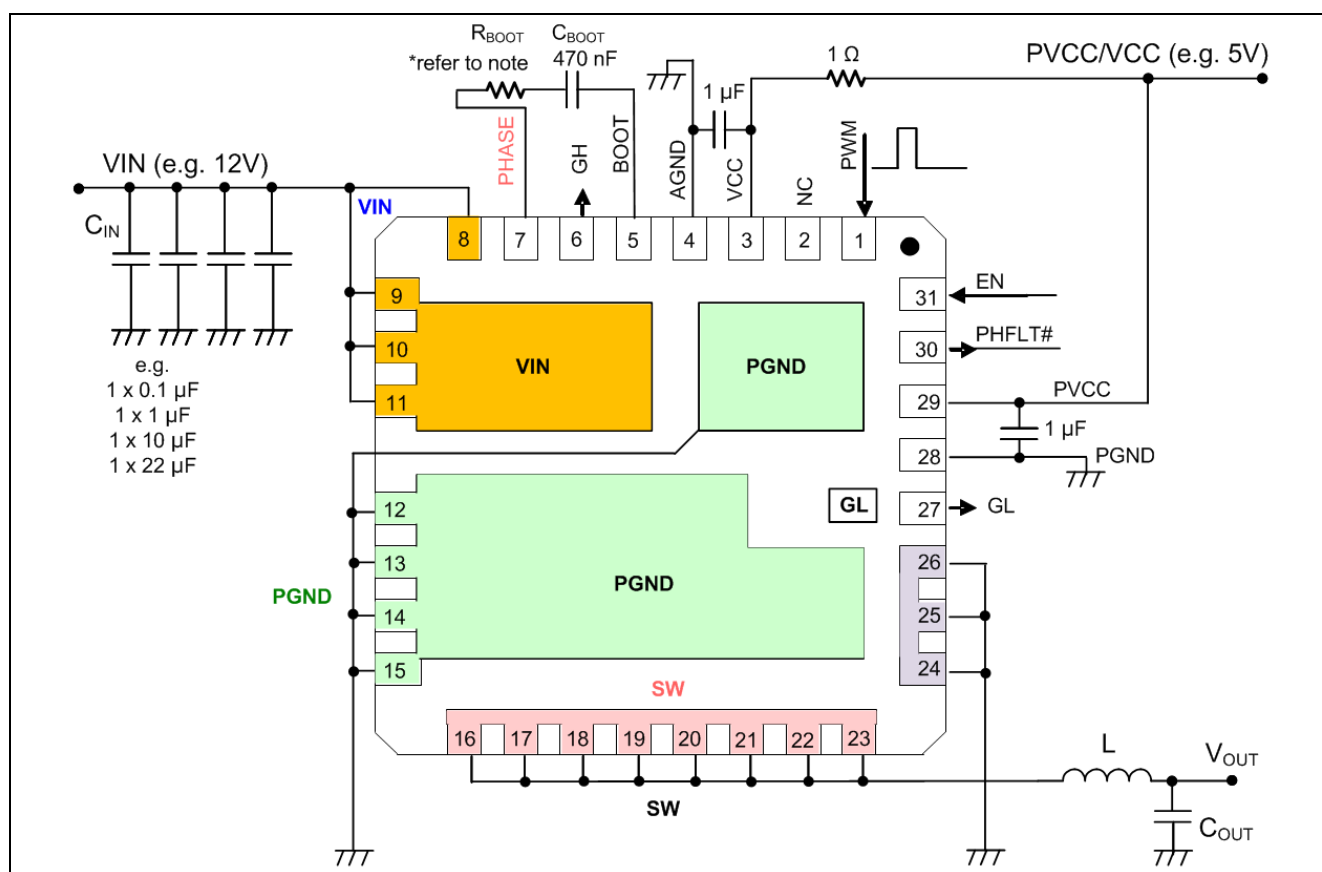


Figure 6 Pin Interconnection Outline (example, transparent top view)

Note:

1. Pin PHASE is internally connected to SW node
2. It is recommended to place a RC filter between VCC and PVCC as shown.
3. Pins 24, 25 and 26 are not internally connected. One can leave them open or connect to GND or to SW.
4. R_{BOOT} is only required for telecom applications with $V_{IN} > 13.2V$ (see Table 8). If necessary, its value should be selected to limit the voltage spike $V_{PHASE} - V_{PGND}$ (AC) to 26V.

The diagram illustrates the connection of a PX8847 microcontroller to five TDA21231 op-amp modules. The PX8847 is connected to various power rails (VDRV +5V, VIN +12V, +3.3V) and has its I2C and SVID interfaces shown. Each TDA21231 module is configured with a Cboot capacitor, a boot resistor, and a feedback network (R1, R2, C1, C2). The output of the op-amp modules is connected to a CPU/Mem block.

Figure 7 Six-phase voltage regulator - typical application (simplified schematic)

7 Gate Driver Timing Diagram

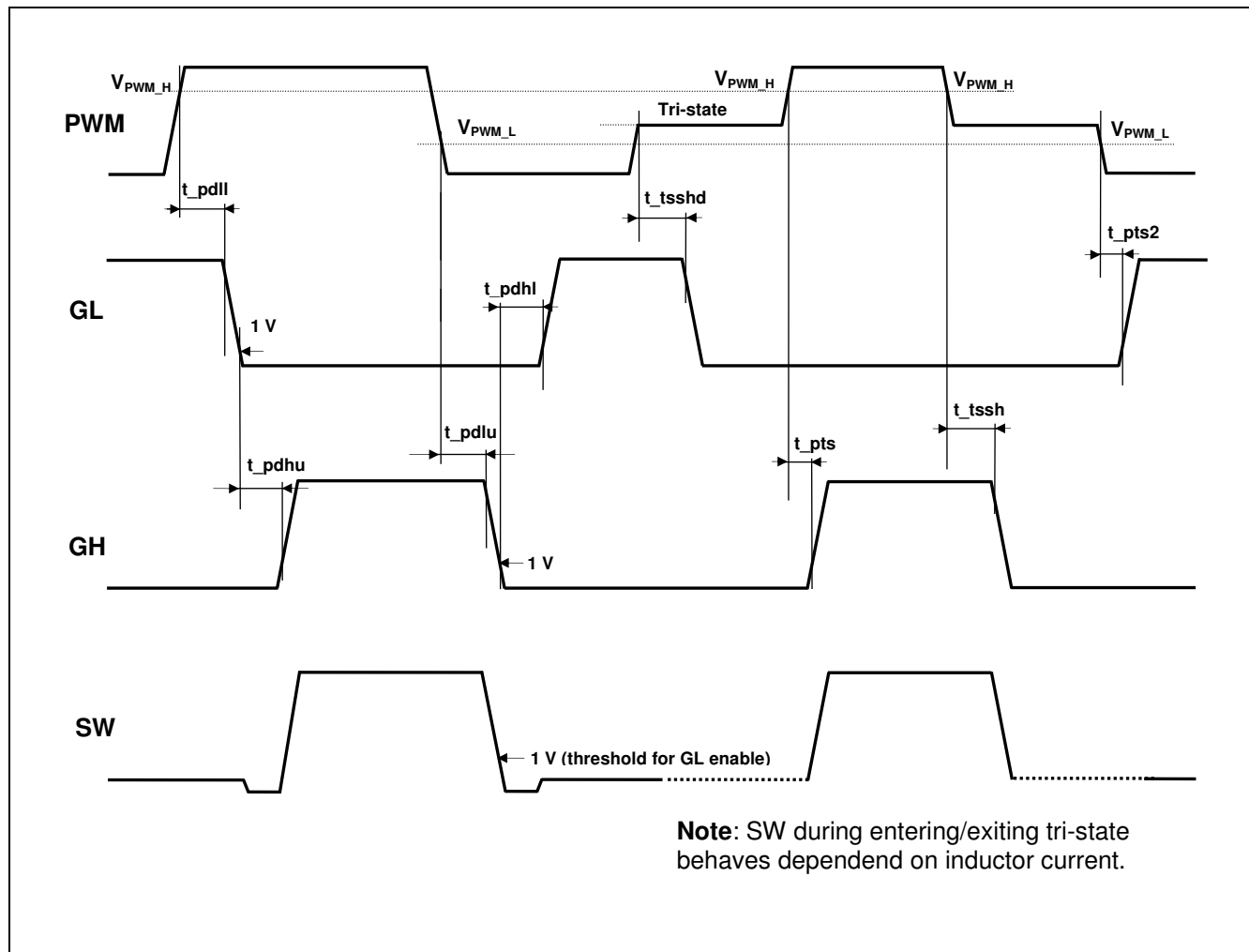


Figure 8 Adaptive Gate Driver Timing Diagram

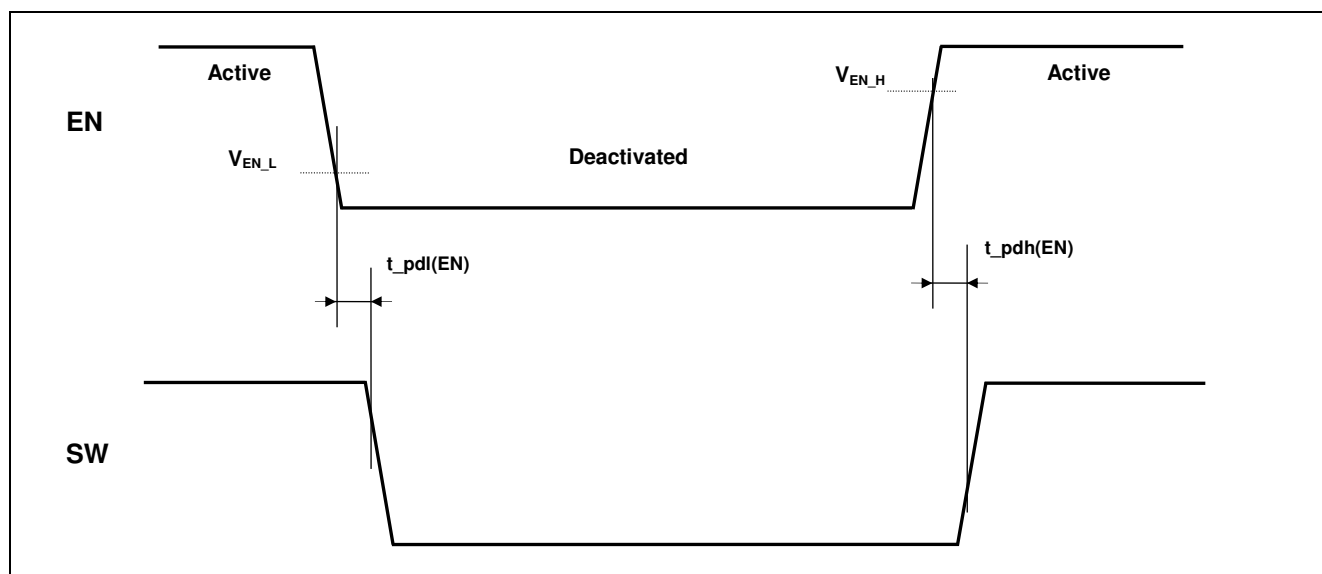


Figure 9 EN Timing Diagram

8 Performance Curves – Typical Data

Operating conditions (unless otherwise specified): $V_{IN} = +12\text{ V}$, $V_{CC} = PV_{CC} = +5\text{ V}$, $V_{OUT} = +1.8\text{ V}$, $f_{sw} = 600\text{ kHz}$, 150nH (Cooper, FP0906R1-R15, DCR = 0.29 m Ω) inductor, $T_A = 25\text{ }^{\circ}\text{C}$, airflow = 300 LFM, no heatsink. Efficiency and power loss reported herein include only TDA21231 losses for a single phase obtained within a 5 phase multiphase operation (CCM to zero load current) on an 8-layer server board.

8.1 Driver Current versus Switching Frequency

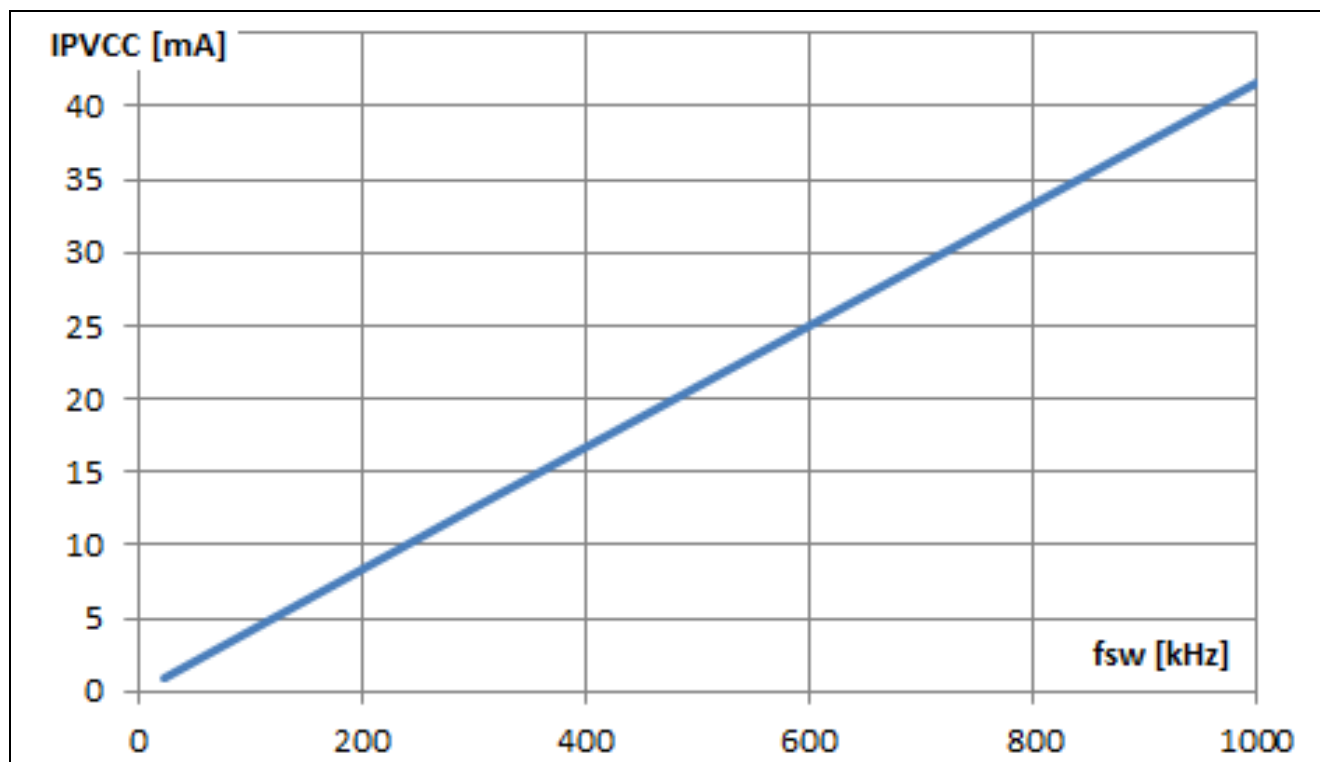


Figure 10 Driver Current over Switching Frequency in CCM Operation

8.2 Efficiency and Power Loss

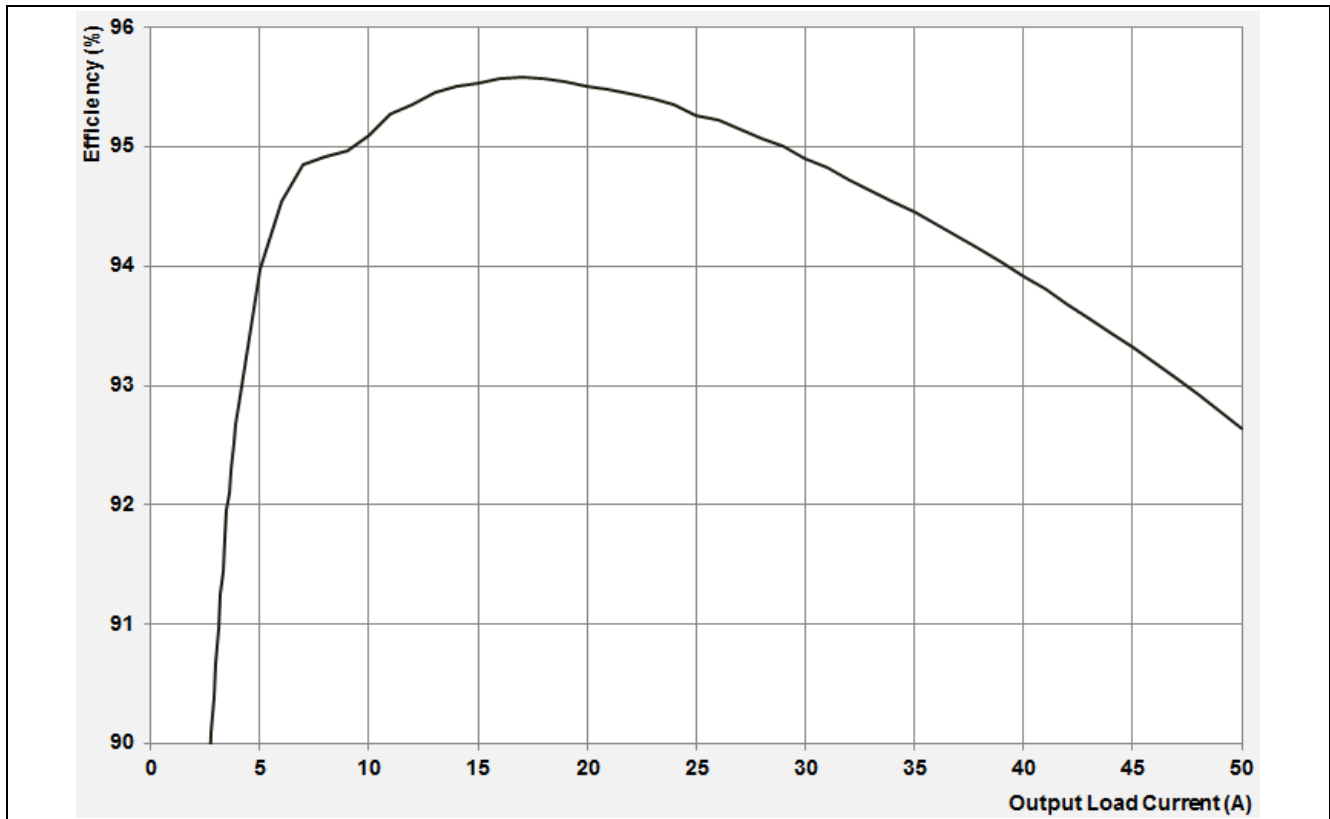


Figure 11 Efficiency at $V_{IN} = 12\text{ V}$, $V_{CC} = PV_{CC} = 5\text{ V}$, $f_{SW} = 600\text{ kHz}$, $V_{OUT} = 1.8\text{ V}$

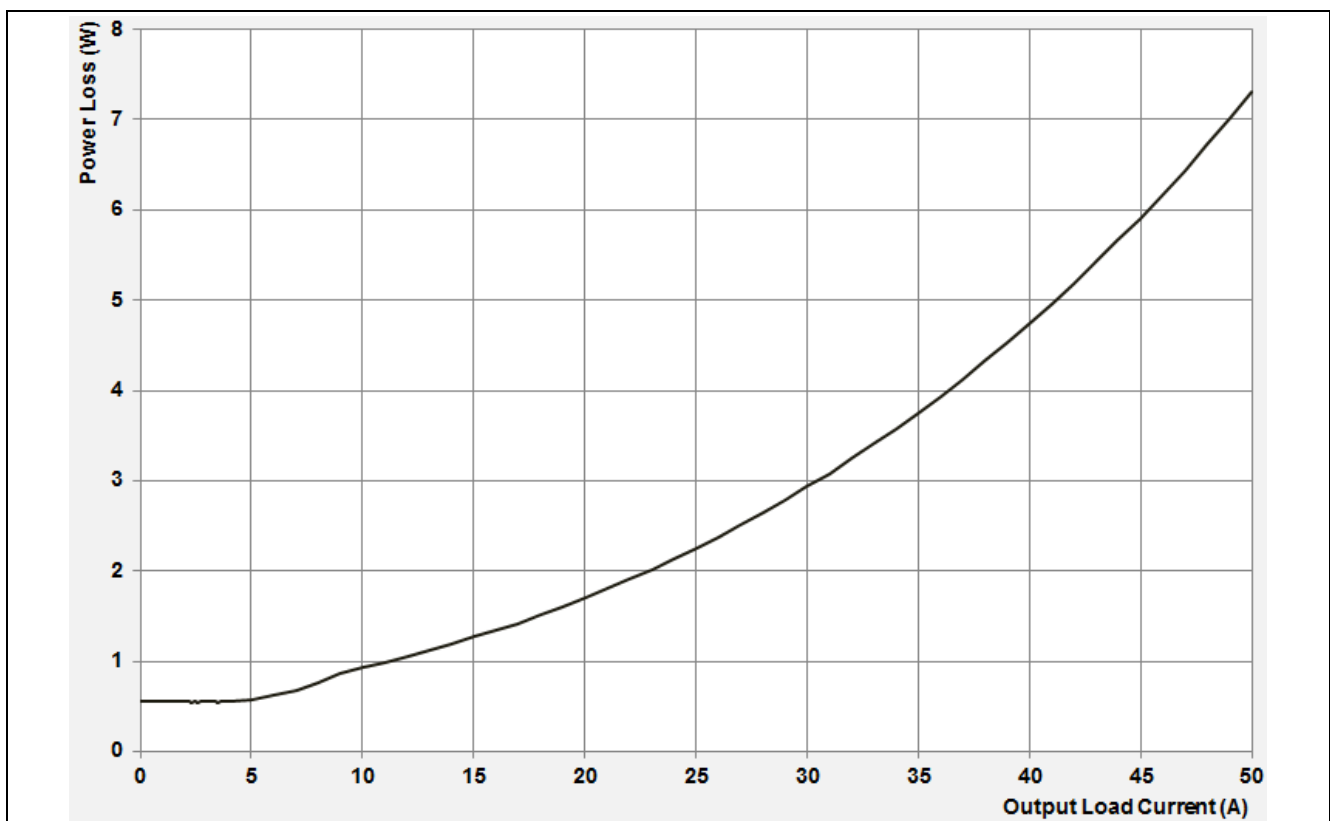


Figure 12 Power Loss at $V_{IN} = 12\text{ V}$, $V_{CC} = PV_{CC} = 5\text{ V}$, $f_{SW} = 600\text{ kHz}$, $V_{OUT} = 1.8\text{ V}$

9 Mechanical Drawing PG-IQFN-31-2

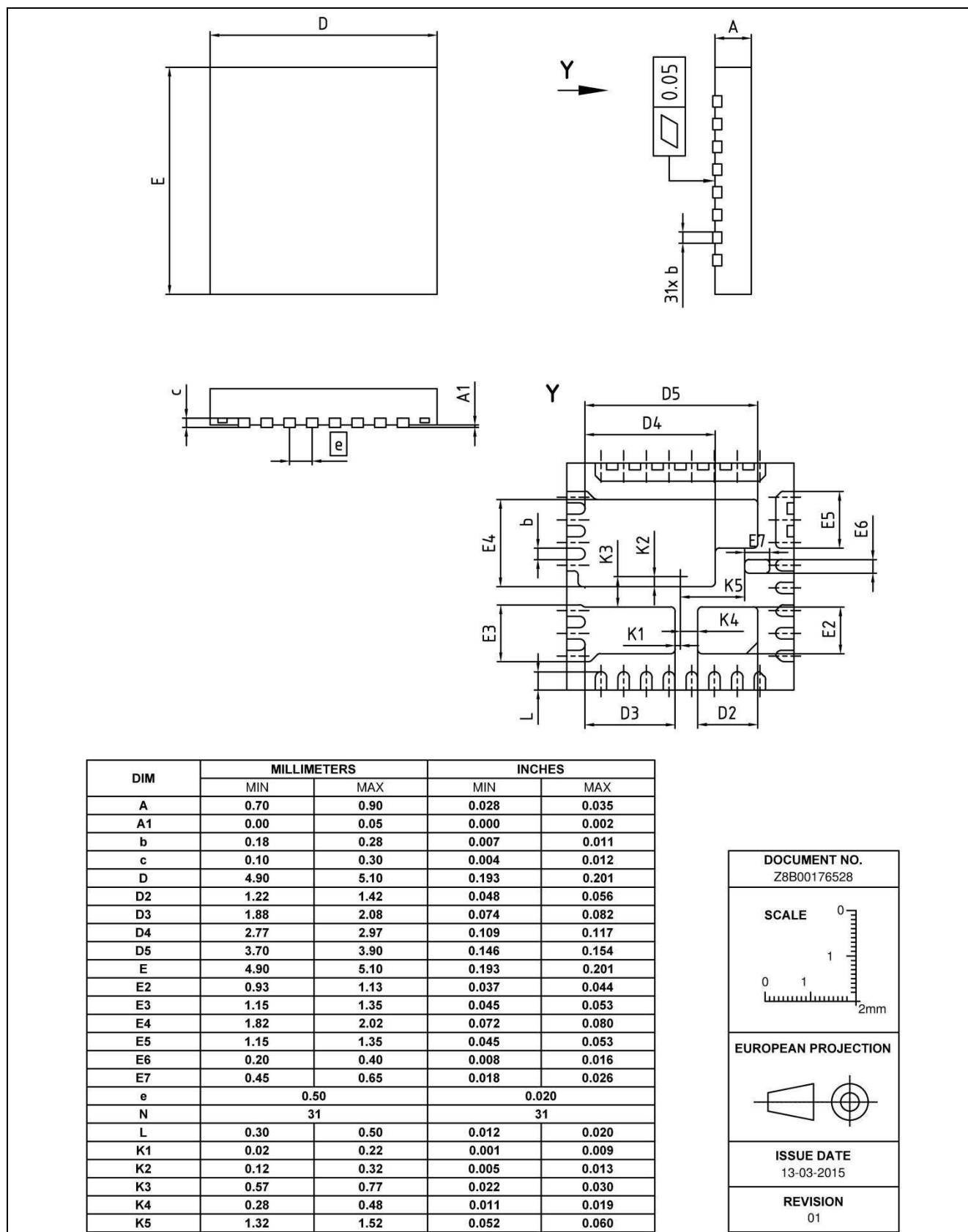


Figure 13 Mechanical Dimensions (in mm)



10 Board Layout Recommendations

The PCB (printed circuit board) layout design follows the listed industry standards:

- Recommended vias: 10 mil⁶ hole with 20 mil via pad diameter, 12 mil hole with 24 mil via pad diameter
- Minimum (typical) via to via center distance: 25 mil (30 ... 35 mil)
- Minimum feature width: 5 mil
- Minimum (typical) clearance: 5 mil (15 ... 20 mil)

Commonly, 10 mil via drill diameters are used for PCBs up to 150 mil thicknesses (usually 22 layers). For thicker boards, 12 mil vias are recommended. To reduce voltage spikes caused by parasitic circuit inductance, all primary decoupling capacitors for VIN, PVCC, BOOT and VCC should be of MLCC type, X6S or X7R rated and located at the same board side as the powerstage close to their respective pins. This is especially important for the VIN to PGND MLCCs.

Electrical and thermal connection of the powerstage to the PCB is crucial for achieving high efficiency. Therefore, vias in VIN and PGND pads are required in the pad areas to connect most effectively to other power and PGND layers. Bigger value MLCC input capacitors should be placed at the bottom side of the PCB close to the vias of the powerstage's VIN and PGND pads. To reduce the stray inductance in the current commutation loop it is strongly recommended to have the 2nd layers from the top and the bottom of the board to be monolithic ground planes. All logic and signal connections between powerstage and controller should be embedded between two ground layers. The routing of the current sense lines back to the controller has to be done differentially, for example with 5 mil spacing and 10 – 15 mil distances to other potentials. If the PCB features more than 10 layers, the passive components associated with the current sense lines should be located only at the top side of the board. All resistors and capacitors near the powerstage should be in 0402 case size. For minimizing distribution loss to the load and maintaining signal integrity, have multiple layers/planes in parallel and ensure that the copper cross section for PGND is at least as big as it is for Vout.

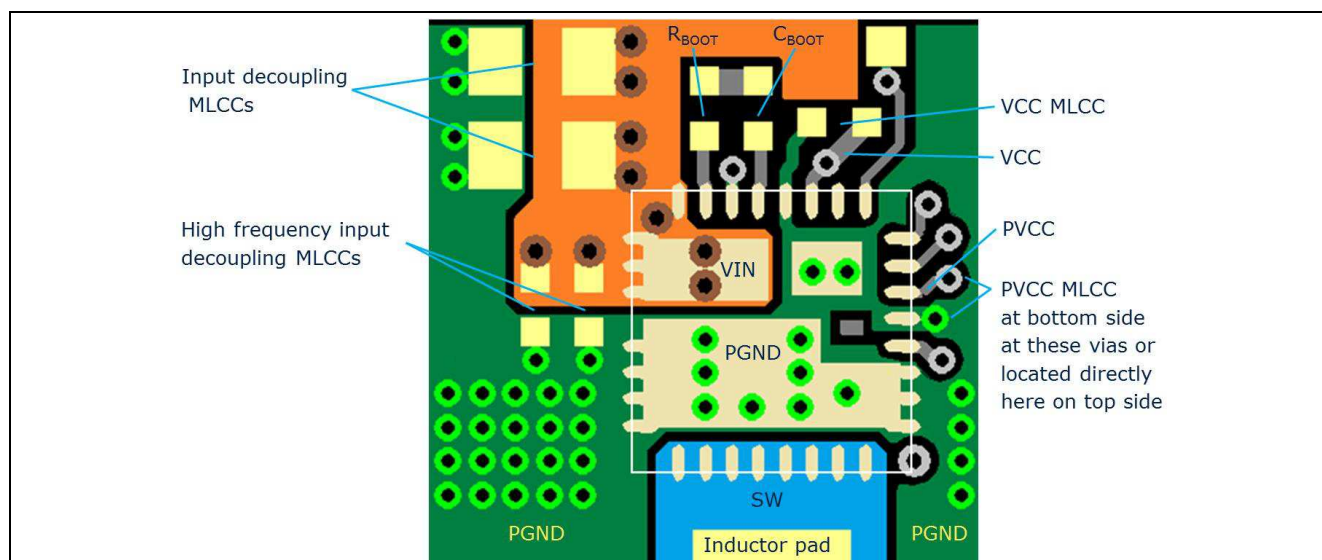


Figure 15 Generic Board Design

⁶ Unit conversion: 1 mil = 25.4 µm

Revision History

TDA21231

Revision: 2015-10-16, Rev. 2.2

Previous Revision

| Revision | Date | Subjects (major changes since last revision) |
|----------|------------|--|
| 1.0 | 2015-03-24 | Release of preliminary version |
| 2.0 | 2015-04-23 | Release of final version |
| 2.1 | 2015-06-04 | updated IPVCC, added performance data |
| 2.2 | 2015-10-16 | updated section 5.1 (driver) |

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