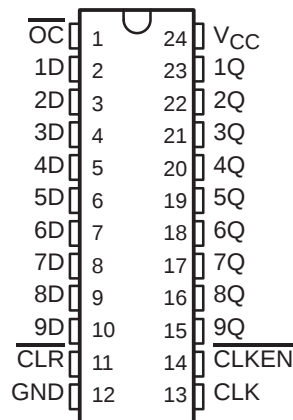


SN54AS823, SN54AS824, SN74AS823, SN74AS824 9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

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- Functionally Equivalent to AMD's AM29823 and AM29824
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses With Parity
- Outputs Have Undershoot Protection Circuitry
- Powerup High-Impedance State
- Buffered Control Inputs to Reduce DC Loading Effects
- Package Options Include Plastic Small Outline Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54AS823 . . . JT PACKAGE
SN74AS823 . . . DW OR NT PACKAGE
(TOP VIEW)

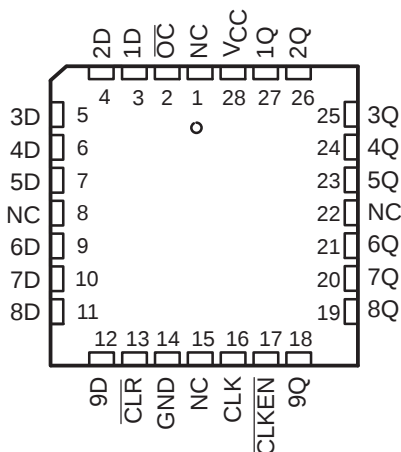


description

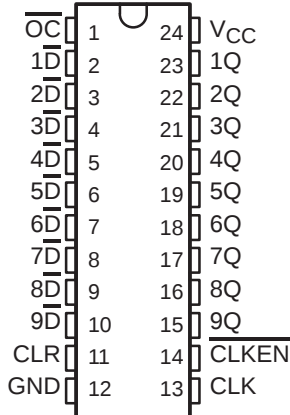
These 9-bit flip-flops feature 3-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing, and working registers.

With the clock enable ($\overline{\text{CLKEN}}$) low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{\text{CLKEN}}$ high will disable the clock buffer, thus latching the outputs. The 'AS823 has noninverting D inputs and the 'AS824 has inverting D inputs. Taking the $\overline{\text{CLR}}$ input low causes the nine Q outputs to go low independently of the clock.

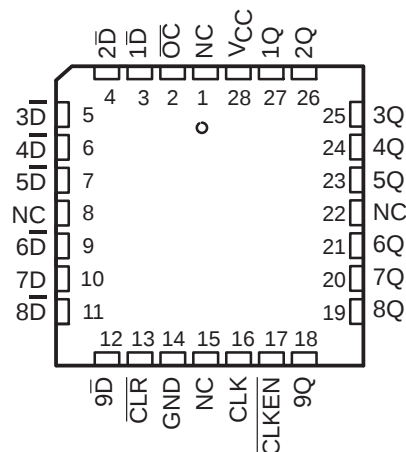
SN54AS823 . . . FK PACKAGE
SN74AS823 . . . FN PACKAGE
(TOP VIEW)



SN54AS824 . . . JT PACKAGE
SN74AS824 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS824 . . . FK PACKAGE
SN74AS824 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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5BASIC

SN54AS823, SN54AS824, SN74AS823, SN74AS824

9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

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description (continued)

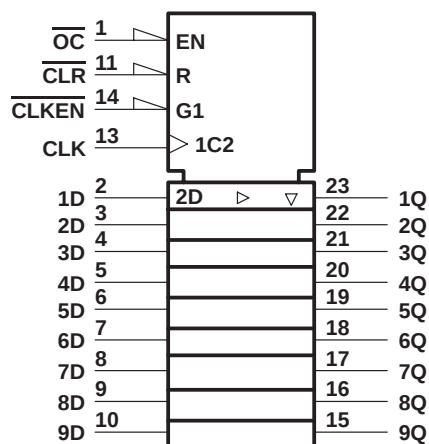
A buffered output-control input $\overline{OC}$ can be used to place the nine outputs in either normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pullup components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AS' family is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS' family is characterized for operation from 0°C to 70°C .

'AS823 FUNCTION TABLE

INPUTS					OUTPUT Q
$\overline{OC}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	
L	L	X	X	X	L
L	H	L	$\uparrow$	H	H
L	H	L	$\uparrow$	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

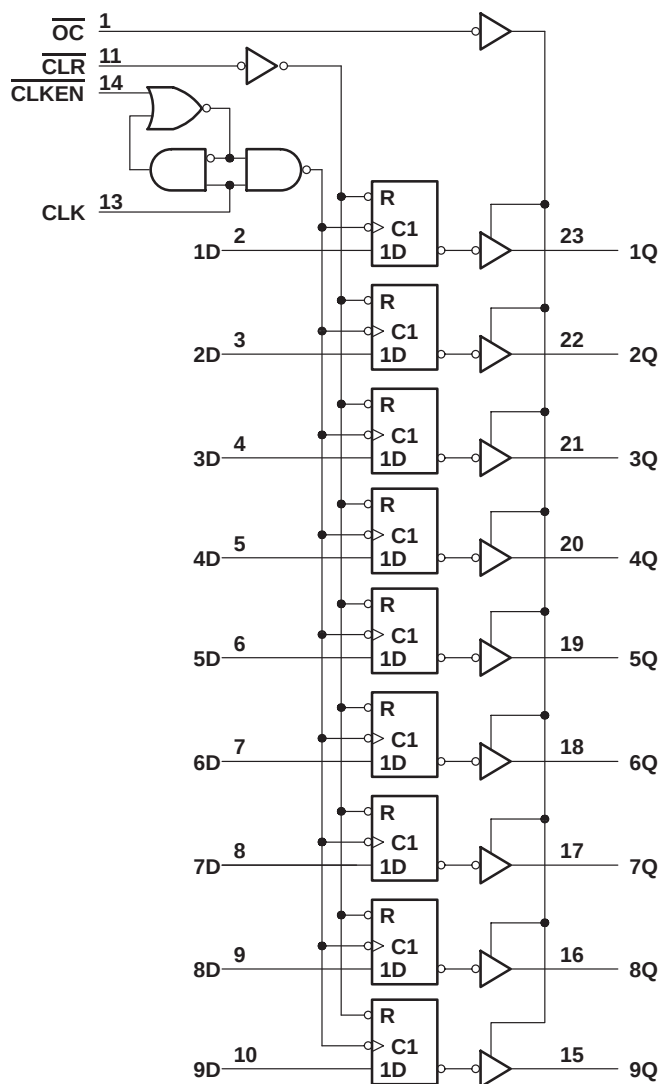
'AS823 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

'AS823 logic diagram (positive logic)



SN54AS824, SN74AS824

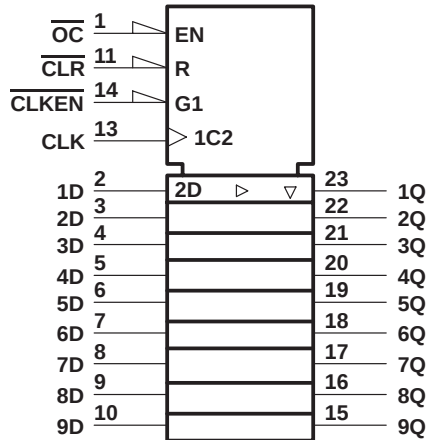
9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS231 – D2825, JUNE 1984 – REVISED JANUARY 1986

'AS824 FUNCTION TABLE†

INPUTS					OUTPUT Q
OC	CLR	CLKEN	CLK	D	
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q ₀
H	X	X	X	X	Z

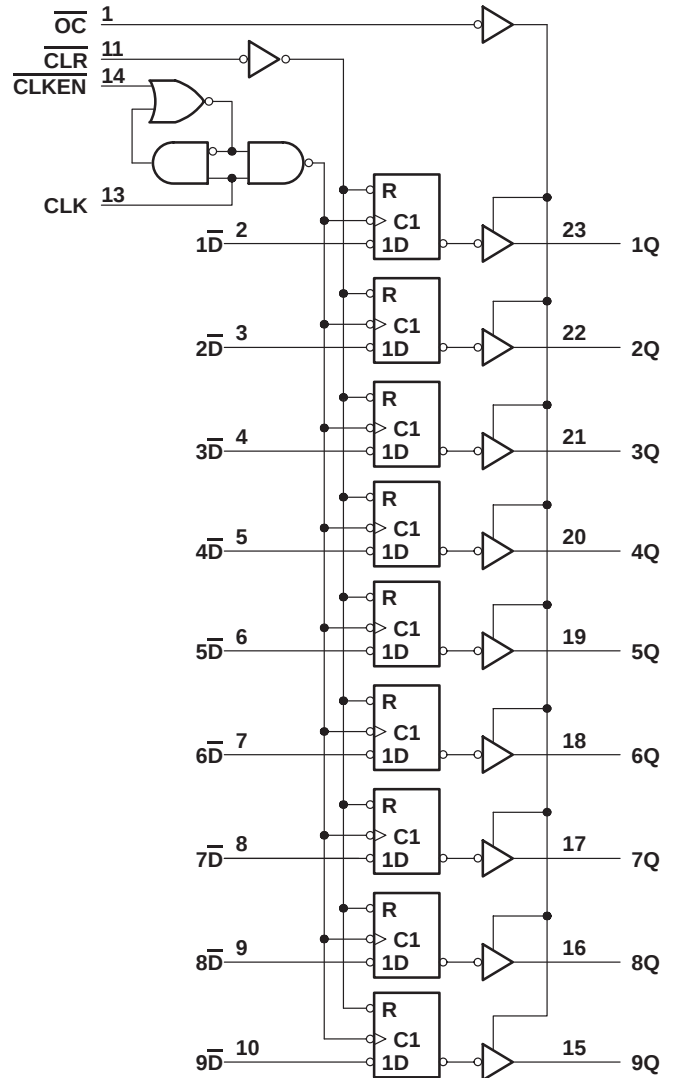
'AS824 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

'AS824 logic diagram positive logic



SN54AS823, SN54AS824, SN74AS823, SN74AS824

9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54AS823, SN54AS824	–55°C to 125°C
SN74AS823, SN74AS824	0°C to 70°C
Storage temperature range	–65°C to 150°C

recommended operating conditions

			SN54AS823 SN54AS824			SN74AS823 SN74AS824			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage		0.8			0.8			V
I _{OH}	High-level output current		−24			−24			mA
I _{OL}	Low-level output current		32			48			mA
t _w	Pulse duration	CLR low	5			4			ns
		CLK high or low	9			8			
t _{su}	Setup time before CLK↑	CLR high	8			8			ns
		Data	7			6			
		CLKEN high or low	7			6			
t _h	Hold time, CLKEN low after CLK↑		0			0			ns
T _A	Operating free-air temperature		−55			125			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS823 SN54AS824			SN74AS823 SN74AS824			UNIT
				MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V _{IK}		V _{CC} = 4.5 V,	I _I = −18 mA	−1.2			−1.2			V
V _{OH}		V _{CC} = 4.5 V to 5.5 V,	I _{OH} = −2 mA	V _{CC} − 2			V _{CC} − 2			V
		V _{CC} = 4.5 V,	I _{OH} = −15 mA	2.4	3.2	2.4	3.2			
		V _{CC} = 4.5 V,	I _{OH} = −24 mA	2		2				
V _{OL}		V _{CC} = 4.5 V,	I _{OL} = 32 mA	0.3 0.5						V
		V _{CC} = 4.5 V,	I _{OL} = 48 mA				0.35 0.5			
I _{OZH}		V _{CC} = 5.5 V,	V _O = 2.7 V	50			50			μA
I _{OZL}		V _{CC} = 5.5 V,	V _O = 0.4 V	−50			−50			μA
I _I		V _{CC} = 5.5 V,	V _I = 7 V	0.1			0.1			mA
I _{IH}		V _{CC} = 5.5 V,	V _O = 2.7 V	20			20			μA
I _{IL}		V _{CC} = 5.5 V,	V _I = 0.4 V	−0.5			−0.5			mA
I _O [‡]		V _{CC} = 5.5 V,	V _O = 2.25 V	−30		−112	−30		−112	mA
I _{CC}	'AS823	V _{CC} = 5.5 V	Outputs high	49 80		49 80				mA
			Outputs low	61 100		61 100				
			Outputs disabled	64 103		64 103				
	'AS824	V _{CC} = 5.5 V	Outputs high	49 80		49 80				mA
			Outputs low	61 100		61 100				
			Outputs disabled	64 103		64 103				

[†] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .



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SN54AS823, SN54AS824, SN74AS823, SN74AS824

9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX †				UNIT
			SN54AS823 SN54AS824		SN74AS823 SN74AS824		
			MIN	MAX	MIN	MAX	
t _{PLH}	CLK	Any Q	3.5	9	3.5	7.5	ns
t _{PHL}			3.5	12	3.5	11	
t _{PHL}	$\overline{\text{CLR}}$	Any Q	3.5	14	3.5	13	ns
t _{PZH}	$\overline{\text{OC}}$	Any Q	4	12	4	11	ns
t _{PZL}			4	13	4	12	
t _{PHZ}	$\overline{\text{OC}}$	Any Q	2	10	2	8	ns
t _{PLZ}			2	10	2	8	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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