

CD4029A Types

CMOS Presettable Up/Down Counter

Binary or BCD-Decade

The RCA-CD4029A consists of a four-stage binary or BCD-decade up/down counter with provisions for look-ahead carry in both counting modes. The inputs consist of a single CLOCK, CARRY-IN (CLOCK INHIBIT), BINARY/DECADE, UP/DOWN, PRESET ENABLE, and four individual JAM signals and a CARRY OUT signal are provided as outputs.

A high PRESET ENABLE signal allows information on the JAM INPUTS to preset the counter to any state asynchronously with the clock. A low on each JAM line, when the PRESET-ENABLE signal is high, resets the counter to its zero count. The counter is advanced one count at the positive transition of the clock when the CARRY-IN and PRESET ENABLE signals are low. Advancement is inhibited when the CARRY-IN or PRESET ENABLE signals are high. The CARRY-OUT signal is normally high and goes low when the counter reaches its maximum count in the UP mode or the minimum count in the DOWN mode provided the CARRY-IN signal is low. The CARRY-IN signal in the high state can thus be considered a CLOCK INHIBIT. The CARRY-IN terminal must be connected to VSS when not in use.

Binary counting is accomplished when the BINARY/DECADE input is high; the counter counts in the decade mode when the BINARY/DECADE input is low. The counter counts Up when the UP/DOWN INPUT is high, and Down when the UP/DOWN INPUT

Features:

- Medium speed operation . . . 5 MHz (typ.) @ CL=15 pF and VDD-VSS=10 V
- Multi-package parallel clocking for synchronous high speed output response or ripple clocking for slow clock input rise and fall times
- "Preset Enable" and individual "Jam" inputs provided
- Binary or decade up/down counting
- BCD outputs in decade mode
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Programmable binary and decade counting/frequency synthesizers-BCD output
- Analog to digital and digital to analog conversion
- Up/Down binary counting
- Magnitude and sign generation
- Up/Down decade counting
- Difference counting

is low. Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement.

Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

RECOMMENDED OPERATING CONDITIONS at TA=25°C, Except as Noted.

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V _{DD} (V)	LIMITS				UNITS
		D, F, K, H Packages		E Package		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T _A =Full Package-Temperature Range)		3	12	3	12	V
Setup Time, t _S *	5 10	650 230	—	1300 460	—	ns
Clock Pulse Width, t _W	5 10	340 170	—	500 250	—	ns
Clock Input Frequency, f _{CL}	5 10	dc dc	1.5 3	dc dc	1 2	MHz
Clock Rise or Fall Time, t _{rCL} ,t _{fCL} **	5 10	— —	15 15	— 15	15	μs
Preset Enable Pulse Width, t _W	5 10	330 160	—	660 320	—	ns

*From Up/Down, Binary/Decode, Carry In, or Preset Enable Control Inputs to Clock Edge.

**If more than one unit is cascaded in the parallel clocked application, tCL should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load.

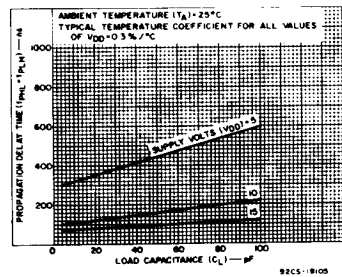
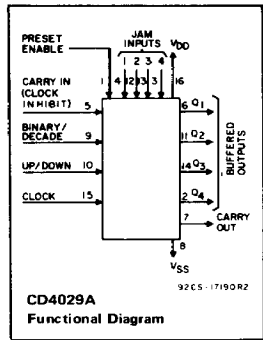


Fig. 1—Typical propagation delay time vs. CL for Q outputs.

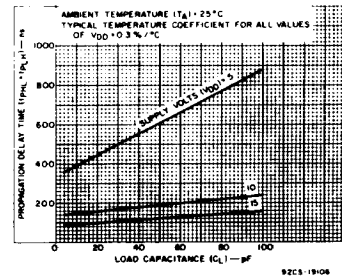


Fig. 2—Typical propagation delay time vs. CL for carry output.

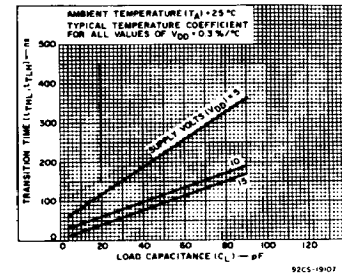


Fig. 3—Typical transition time vs. CL for Q outputs.

CD4029A Types

MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE (T_{stg})	-65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	-55 to +125°C
PACKAGE TYPE E	40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
(Voltages referenced to V_{SS} Terminal)	-0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):	
FOR $T_A = -40$ to +60°C (PACKAGE TYPE E)	500 mW
FOR $T_A = +60$ to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
FOR $T_A = -55$ to +100°C (PACKAGE TYPES D, F, K)	500 mW
FOR $T_A = +100$ to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:	
FOR T_A =FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A=25^\circ\text{C}$, Input $t_r, t_f=20$ ns,
 $C_L=15$ pF, $R_L=200$ k Ω

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		D, F, K, H Packages			E Package			
		V _{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	
Clocked Operation								
Propagation Delay Time:								
^t _{PHL} , ^t _{PLH}		5	—	325	650	—	325	1300
Q Outputs		10	—	115	230	—	115	460
Carry Output		5	—	425	850	—	425	1700
		10	—	150	300	—	150	600
Transition Time:								
^t _{THL} , ^t _{TLH}		5	—	100	200	—	100	400
Q Outputs		10	—	50	100	—	50	200
Carry Output		5	—	200	400	—	200	800
		10	—	100	200	—	100	400
Minimum Clock Pulse Width, ^t _w		5	—	200	340	—	200	500
		10	—	100	170	—	100	250
Clock Rise & Fall Time, ^t _{rCL} , ^t _{fCL} **		5	—	—	15	—	—	15
		10	—	—	15	—	—	15
Minimum Setup Times, ^t _s *		5	—	325	650	—	325	1300
		10	—	115	230	—	115	460
Maximum Clock Input Frequency, ^f _{CL}		5	1.5	2.5	—	1	2.5	—
		10	3	5	—	2	5	—
Input Capacitance, C _I	Any Input		—	5	—	—	5	—
Preset Enable								
Propagation Delay Time:								
^t _{PHL} , ^t _{PLH}		5	—	325	650	—	325	1300
Q Outputs		10	—	115	230	—	115	460
Carry Output		5	—	425	850	—	425	1700
		10	—	150	300	—	150	600
Minimum Preset Enable Pulse Width, ^t _w		5	—	115	330	—	115	660
		10	—	80	160	—	80	320
Minimum Preset Enable Removal Time		5	—	325	650	—	325	1300
		10	—	115	230	—	115	460
Carry Input								
Propagation Delay Time:								
^t _{PHL} , ^t _{PLH}		5	—	175	350	—	175	700
Carry Output		10	—	50	100	—	50	200

For footnotes, see Recommended Operating Conditions.

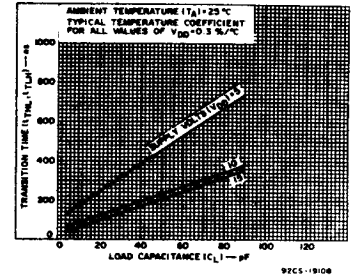


Fig. 4—Typical transition time vs. C_L for carry output.

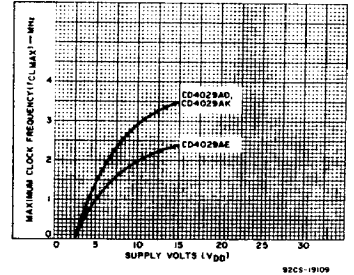


Fig. 5—Maximum clock input frequency vs. V_{DD} .

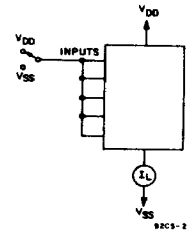


Fig. 6—Quiescent-device-current test circuit.

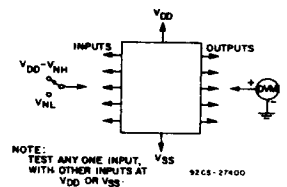


Fig. 7—Noise-immunity test circuit.

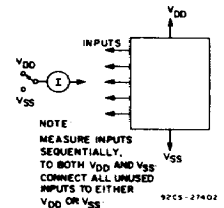


Fig. 8—Input-leakage-current test circuit.

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STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D, F, K, H Packages				E Package				
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	+25		+125	-40	+25		+85	
					Typ.	Limit			Typ.	Limit		
Quiescent Device Current, I _L Max.	—	—	5	5	0.3	5	300	50	0.5	50	700	μA
	—	—	10	10	0.5	10	600	100	1	100	1400	
	—	—	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V _{OL}	—	5	5	0 Typ.; 0.05 Max.								V
High-Level, V _{OH}	—	10	10	0 Typ.; 0.05 Max.								
	—	0	5	4.95 Min.; 5 Typ.								
	—	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V _{NL}	4.2	—	5	1.5 Min.; 2.25 Typ.								V
Inputs High, V _{NH}	9	—	10	3 Min.; 4.5 Typ.								
	0.8	—	5	1.5 Min.; 2.25 Typ.								
	1	—	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V _{NML}	4.5	—	5	1 Min.								V
Inputs High, V _{NMH}	9	—	10	1 Min.								
	0.5	—	5	1 Min.								
	1	—	10	1 Min.								
Output Drive Current: N-Channel (Sink), I _{DN} Min.	0.5	—	5	0.5	0.8	0.4	0.28	0.24	0.8	0.2	0.16	mA
Q Outputs	0.5	—	10	0.74	1.2	0.6	0.42	0.36	1.2	0.3	0.24	
Carry Out-put	0.5	—	5	0.1	0.16	0.08	0.06	0.05	0.16	0.04	0.03	
	0.5	—	10	0.4	0.64	0.32	0.22	0.19	0.64	0.16	0.13	mA
P-Channel (Source), I _{DP} Min.	4.5	—	5	-0.18	-0.24	-0.12	-0.08	-0.07	-0.24	-0.06	-0.05	
Q Outputs	9.5	—	10	-0.3	-0.4	-0.2	-0.14	-0.14	-0.4	-0.1	-0.08	
Carry Out-put	4.5	—	5	-0.09	-0.12	-0.06	-0.04	-0.04	-0.12	-0.03	-0.02	mA
	9.5	—	10	-0.15	-0.2	-0.1	-0.07	-0.07	-0.2	-0.05	-0.04	
Input Leakage Current, I _{IL} , I _{IH}	Any Input	—	15	±10 ⁻⁵ Typ., ±1 Max.								μA

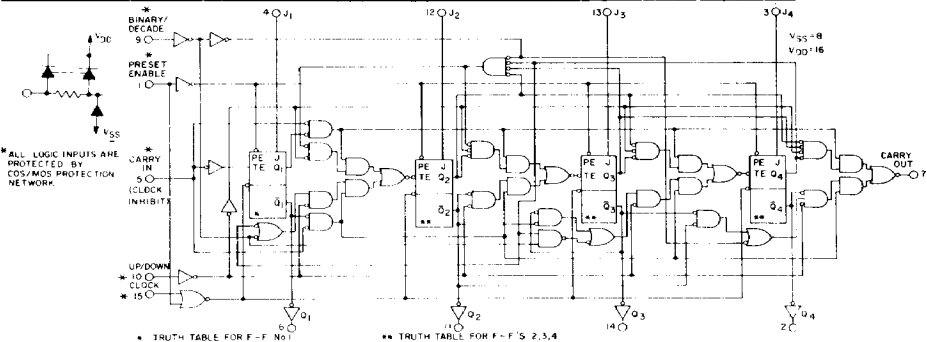


Fig. 11—Logic diagram.

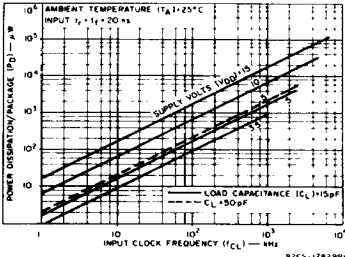


Fig. 9—Typical dissipation characteristics.

