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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

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HD74HC279

Quad. $\overline{S}$ – $\overline{R}$ Latches

RENESAS

ADE-205-483 (Z)

1st. Edition

Sep. 2000

Description

The latch is ideally suited for use as temporary stage for binary information processing and input/output units. When either $\overline{S}$ or $\overline{R}$ is low, output is dependent on $\overline{R}$ input. When both inputs are high, Output is stored before the indicated steady-state input conditions were established. And when both inputs are low, output is high, but this high level are uncontinuance, if either of input goes high.

Features

- High Speed Operation: $t_{pd}(\overline{S} \text{ to } Q) = 10 \text{ ns typ } (C_L = 50 \text{ pF})$
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2 \text{ to } 6 \text{ V}$
- Low Input Current: $1 \mu\text{A max}$
- Low Quiescent Supply Current: $I_{CC}(\text{static}) = 2 \mu\text{A max } (T_a = 25^\circ\text{C})$

Function Table

Input		Output
$\overline{S}^{*2}$	$\overline{R}$	Q
H	H	Q_0
L	H	H
H	L	L
L	L	H^{*1}

H : High level

L : Low level

Q_0 : The level of Q respectively, before the indicated steady-state input conditions were established.

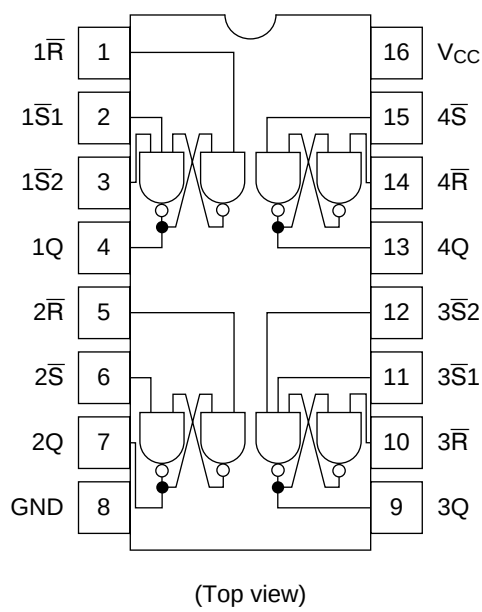
Notes: 1. It is unpredictable, if $\overline{S}$ or $\overline{R}$ goes High.

2. As to latches which has two $\overline{S}$ inputs.

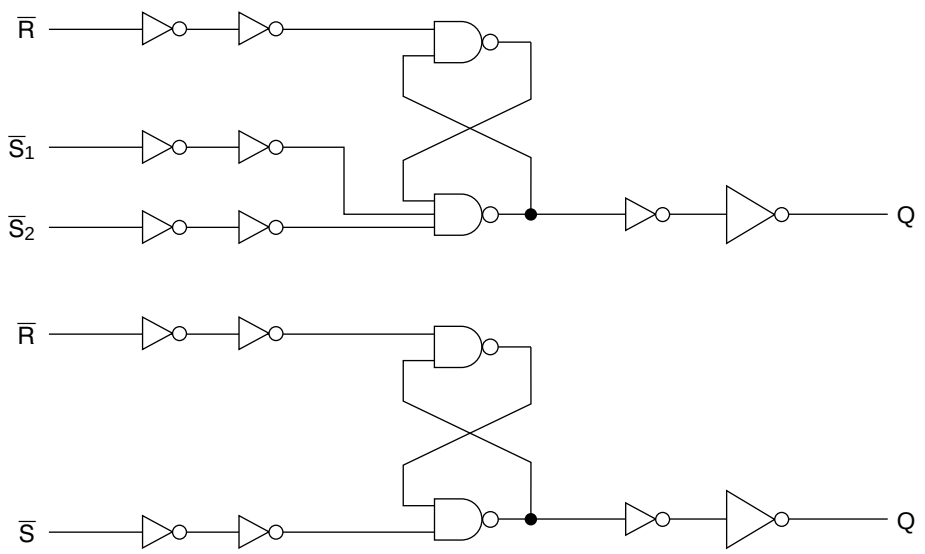
H: Both of $\overline{S}$ inputs are high.

L: Either or both of $\overline{S}$ inputs are low.

Pin Arrangement



Logic Diagram (1/2)



DC Characteristics

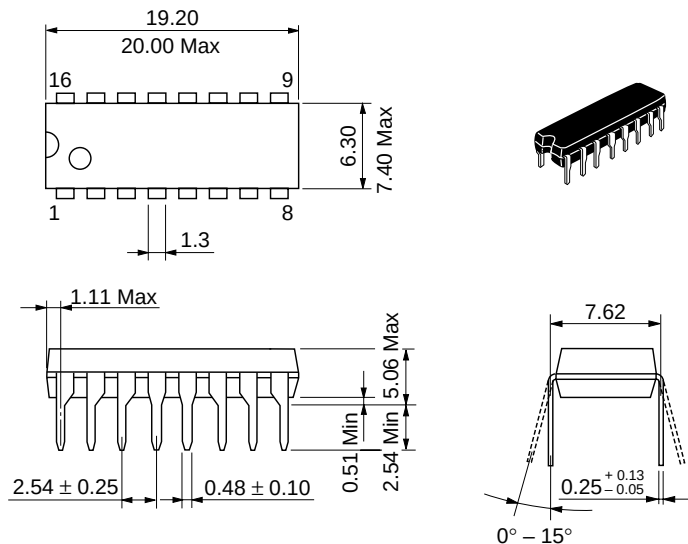
Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V _{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL} I _{OH} = -20 μA	
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I _{OH} = -4 mA
		6.0	5.68	—	—	5.63	—			I _{OH} = -5.2 mA
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V _{IH} or V _{IL} I _{OL} = 20 μA	
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I _{OL} = 4 mA
		6.0	—	—	0.26	—	0.33			I _{OL} = 5.2 mA
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND	
Quiescent supply current	I _{CC}	6.0	—	—	2.0	—	20	μA	Vin = V _{CC} or GND, Iout = 0 μA	

AC Characteristics (C_L = 50 pF, Input t_r = t_f = 6 ns)

Item	Symbol	V _{CC} (V)	Ta = −40 to +85°C						Unit	Test Conditions
			Ta = 25°C							
			Min	Typ	Max	Min	Max			
Propagation delay time	t _{PLH}	2.0	—	—	130	—	165	ns	$\overline{S}$ to Q	
	t _{PHL}	4.5	—	10	26	—	33			
		6.0	—	—	22	—	28			
	t _{PHL}	2.0	—	—	120	—	150	ns	$\overline{R}$ to Q	
		4.5	—	12	24	—	30			
		6.0	—	—	20	—	26			
Output rise/fall time	t _{TLH}	2.0	—	—	75	—	95	ns		
	t _{THL}	4.5	—	5	15	—	19			
		6.0	—	—	13	—	16			
Input capacitance	C _{in}	—	—	5	10	—	10	pF		

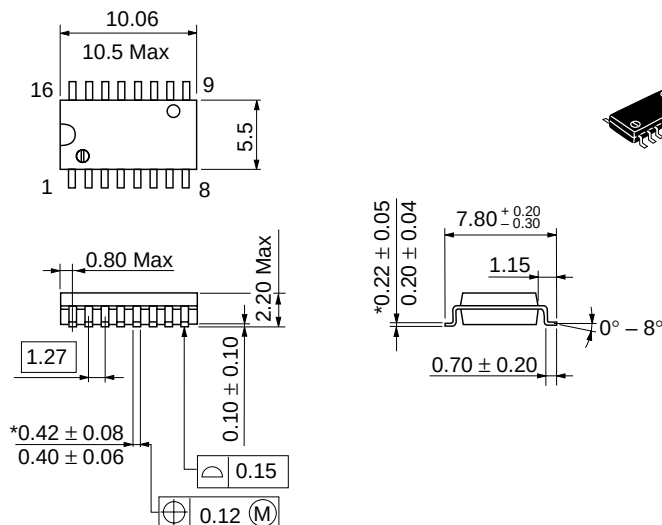
Package Dimensions

Unit: mm



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	1.07 g

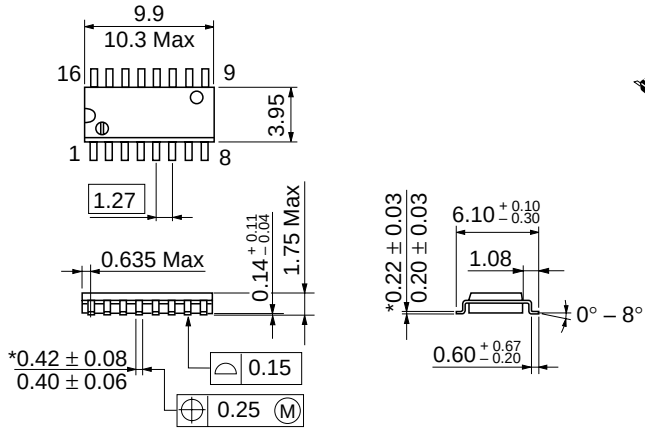
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.24 g

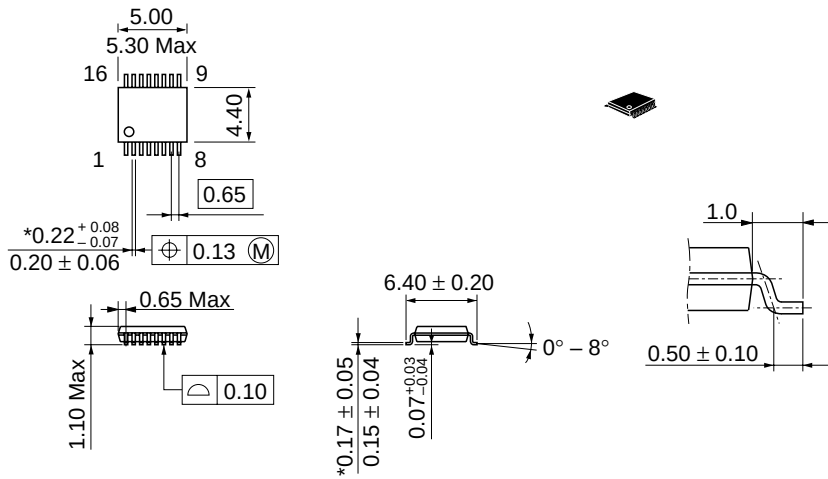
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.15 g

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-16DA
JEDEC	—
EIAJ	—
Mass (reference value)	0.05 g

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