Features

- Dual Outputs
  (See Ordering Information)
- Ideal Power Source for DSPs
- 12V Input
- Outputs Adjustable
- Remote Sensing (Vo_1 & Vo_2)
- Standby Function
- Soft-Start
- Internal Sequencing
- Short Circuit Protection
- 23-pin Space-Saving Package
- Solderable Copper Case

Description

The PT6980 Excalibur™ series of power modules are dual output integrated switching regulators (ISRs) specifically designed to power mixed signal ICs. Operating from a 12-V input bus, the dual output provides power for both the digital I/O logic and a DSP core from a single module. Both output voltages are internally sequenced during power-up and power-down to comply with the requirements of the latest DSP chips. Each output is independently adjustable or can be set to at least one alternative bus voltage with a simple pin-strap. The modules are made available in a space-saving solderable case. The features include output current limit and short-circuit protection.

Ordering Information

PT6981❑ = +2.5/1.8 Volts
PT6982❑ = +3.3/2.5 Volts
PT6983❑ = +3.3/1.8 Volts
PT6984❑ = +3.3/1.2 Volts
PT6985❑ = +2.5/1.2 Volts

PT Series Suffix (PT1234x)

Case/Pin Configuration	Order Suffix	Package Code
Vertical	N	(ELF)
Horizontal	A	(ELG)
SMD	C	(ELH)

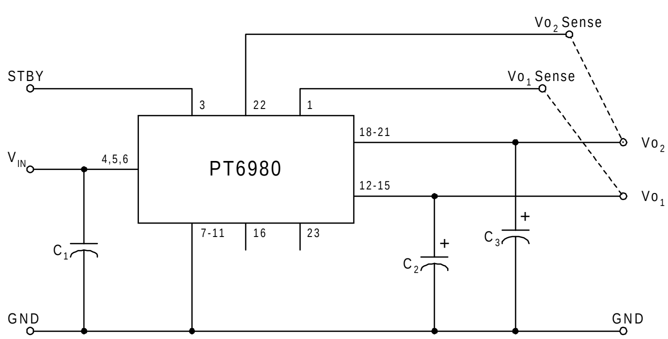
(Reference the applicable package code drawing for the dimensions and PC layout)

Pin-Out Information

Pin	Function	Pin	Function
1	Vo_1 Sense	13	Vo_1
2	No Connect	14	Vo_1
3	STBY	15	Vo_1
4	V_{in}	16	Vo_1 Adjust*
5	V_{in}	17	No Connect
6	V_{in}	18	Vo_2
7	GND	19	Vo_2
8	GND	20	Vo_2
9	GND	21	Vo_2
10	GND	22	Vo_2 Sense
11	GND	23	Vo_2 Adjust*
12	Vo_1		

* *Vo_1 and Vo_2 can be pin-strapped to another voltage. See application note on output voltage adjustment.*

Standard Application



C_1 = Req'd 560µF electrolytic
C_2 = Req'd 330µF electrolytic
C_3 = Optional 100µF electrolytic

General Specifications (Unless otherwise stated, T_a =25°C, V_{in} =12V)

Characteristic	Symbol	Conditions	PT6980 Series Min	Typ	Max	Units
Short Circuit Current	I_{sc}	$Io_1 + Io_2$ combined	—	19	—	A
Switching Frequency	f_o	Over V_{in} range	500	550	600	kHz
Standby (Pin 3)		Referenced to GND (pin 7)				
Input High Voltage	V_{IH}		—	—	Open (1)	V
Input Low Voltage	V_{IL}		–0.1	—	+0.4	
Input Low Current	I_{IL}		—	-0.5	–	mA
Standby Input Current	I_{in} standby	pin 3 to GND	—	4	6	mA
External Output Capacitance	C_2		330 (2)	—	15,000 (2)	µF
	C_3		0	—	330	
Maximum Operating Temperature Range	T_a	Over V_{in} Range	–40 (3)	—	+85 (4)	°C
Storage Temperature	T_s	—	–40	—	+125	°C
Mechanical Shock		Per Mil-STD-883D, Method 2002.3 1 msec, ½ Sine, mounted	—	500	—	G's
Mechanical Vibration		Per Mil-STD-883D, Method 2007.2 20-2000 Hz, Soldered in a PC board	—	15	—	G's
Weight	—	Vertical/Horizontal	—	26	—	grams
Flammability	—	Meets UL 94V-O				

Notes: (1) *The Standby (pin 3) has an internal pull-up to Vin, and if it is left open circuit the module will operate when input power is applied. Refer to the application notes for interface considerations.*
(2) *The total combined ESR of all output capacitance at 100kHz must be (less than) <50 mΩ.*
(3) *For operating temperatures below 0°C, Cin and Cout must have stable characteristics. Use either tantalum or Oscon® capacitors.*
(4) *See Safe Operating Area curves for the specific output voltage combination, or contact the factory for the appropriate derating.*

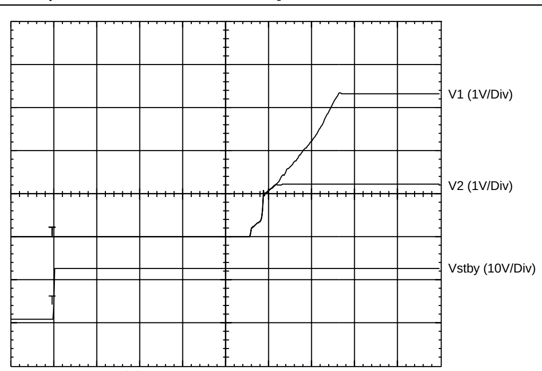
Input/Output Capacitors: *The PT6980 series requires a 330µF electrolytic capacitor at both the input and output for proper operation (300µF for Oscon® or low ESR tantalum). In addition, the input capacitance must be rated for a minimum of 1.0Arms ripple current. For transient or dynamic load applications, additional capacitance may be required. Refer to the application notes for more information.*

Power-up Sequencing and Vo_1/Vo_2 Loading

Power-up Sequencing

The PT6980 series of regulators provide two output voltages, Vo_1 and Vo_2. Each of the output voltage combinations offered by the PT6980 series provides power for both a low-voltage processor core, and the associated digital support circuitry. In addition, each output is internally sequenced during power-up and power-down to comply with the requirements of most DSP and µP IC's, and their accompanying chipsets. Figure 1 shows the typical waveforms of the output voltages, Vo_1 and Vo_2, from the instance that either input power is applied or the module is enabled via the Standby pin. Following a delay of about 25 milli-secs, the voltages at Vo_1 and Vo_2 rise together until Vo_2 reaches its set-point. Then Vo_1 continues to rise until both output voltages have reached full voltage.

Figure 1; PT6980 Series Power-up



Vo_1/Vo_2 Loading

The output voltages from the PT6980 series regulators are independently regulated. The voltage at Vo_1 is produced by a highly efficient switching regulator. The lower output voltage, Vo_2, is derived from Vo_1. The regulation method used for Vo_2 also provides control of this output voltage during power-down. Vo_2 will sink current if the voltage at Vo_1 attempts to fall below it.

The load specifications for each model of the PT6980 series gives both a 'Typical' (Typ) and 'Maximum' (Max) load current for each output. For operation within the product's rating, the load currents at Vo_1 and Vo_2 must comply with the following limits:-

- Io_2 must be less than Io_2(max).
- The sum-total current from both outputs (Io_1 + Io_2) must not exceed Io_1(max).

In the case that either Vo_1 or Vo_2 are adjusted to some other value than the default output voltage, the absolute maximum load current for Io_2 must be revised to comply with the following equation.

$$Io_2\,(max) = \frac{2.5}{Vo_1 - Vo_2} \quad Adc$$

Consult the specification table for each model of the series for the actual numeric values.

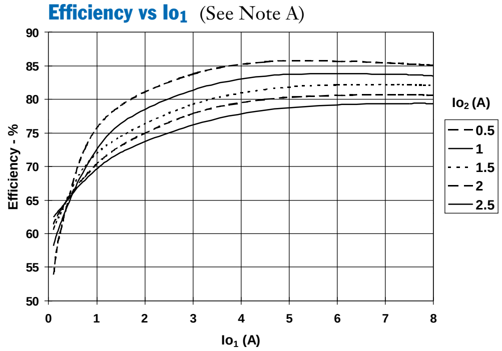
PT6981 Performance Specifications (Unless otherwise stated, T_a =25°C, V_{in} =12V, C_1 =560µF, C_2 =330µF, Io_1 =Io_1typ, and Io_2 =Io_2typ)

				PT6981 (2.5V/1.8V)			
Characteristic	**Symbol**	**Conditions**		**Min**	**Typ**	**Max**	**Units**
Output Current	Io_1 Io_2	T_a =25°C, natural convection	Vo_1 (2.5V) Vo_2 (1.8V)	0.1 (i) 0	8 (ii) 2.5 (ii)	10.5 (iii) 2.5 (iii)	A
	Io_1 Io_2	T_a =60°C, 200LFM airflow	Vo_1 (2.5V) Vo_2 (1.8V)	0.1 (i) 0	8 (ii) 2.5 (ii)	10.5 (iii) 2.5 (iii)	A
Input Voltage Range	V_{in}	Over I_o Range		10.8	—	13.2	VDC
Set Point Voltage Tolerance	V_o tol		Vo_1 Vo_2	— —	±12 ±9	±38 ±27	mV
Temperature Variation	Reg_{temp}	–40° >T_a > +85°C	Vo_1 Vo_2	— —	±0.5 ±0.5	— —	%V_o
Line Regulation	Reg_{line}	Over V_{in} range	Vo_1 Vo_2	— —	±10 ±5	±15 ±7	mV
Load Regulation	Reg_{load}	Over I_o range	Vo_1 Vo_2	— —	±10 ±5	±15 ±7	mV
Total Output Voltage Variation	ΔV_otot	Includes set-point, line, load –40° >T_a > +85°C	Vo_1 Vo_2	— —	±44 ±28	— —	mV
Efficiency	η			—	80	—	%
V_o Ripple (pk-pk)	V_r	20MHz bandwidth	Vo_1 Vo_2	— —	35 35	— —	mV_{pp}
Transient Response	t_{tr}	1A/µs load step, 50% to 100% $I_o$typ		—	60	—	µs
	ΔV_{tr}	V_o over/undershoot	Vo_1 Vo_2	— —	±50 ±20	— —	mV

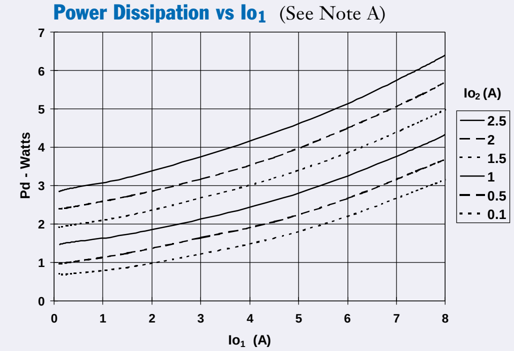
Notes: *(i)* *Io_1(min) current of 0.1A can be divided between both outputs, Vo_1 or Vo_2. The module will operate at no load with reduced specifications.*
(ii) *The typical current is that which can be drawn simultaneously from both outputs under the stated operating conditions.*
(iii) *The sum of Io_1 and Io_2 must be less than Io_1max, and Io_2 must be less than Io_2max.*

PT6981 Typical Characteristics

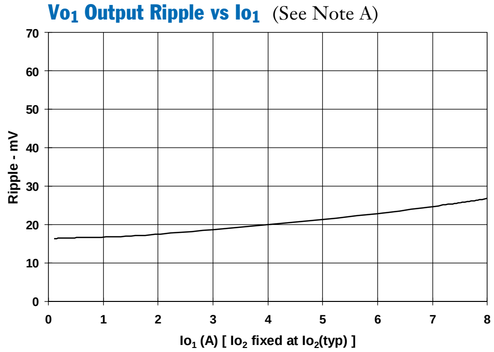
Efficiency vs Io_1 (See Note A)



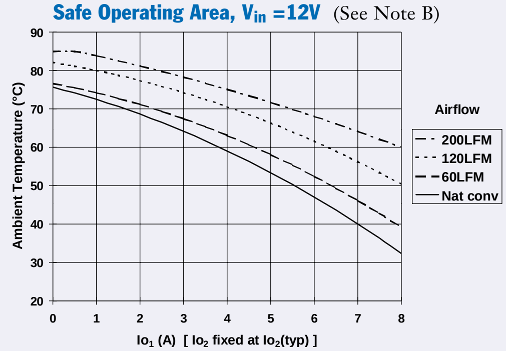
Power Dissipation vs Io_1 (See Note A)



Vo_1 Output Ripple vs Io_1 (See Note A)



Safe Operating Area, V_{in} =12V (See Note B)



Note A: *Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the Converter.*
Note B: *SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures*

PT6982 Performance Specifications

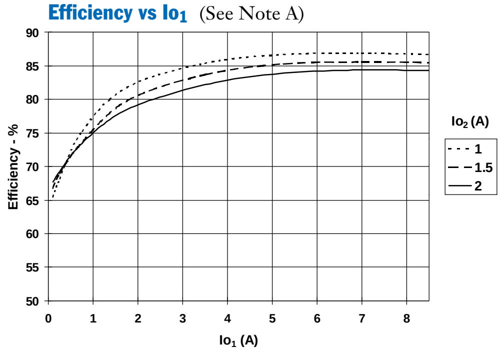
(Unless otherwise stated, T_a =25°C, V_{in} =12V, C_1 =560µF, C_2 =330µF, Io_1 =Io_1typ, and Io_2 =Io_2typ)

Characteristic	Symbol	Conditions		PT6982 (3.3V/2.5V) Min	Typ	Max	Units
Output Current	Io_1 Io_2	T_a=25°C, natural convection	Vo_1 (3.3V) Vo_2 (2.5V)	0.1 (i) 0	8.5 (ii) 2 (ii)	10.5 (iii) 2.25 (iii)	A
	Io_1 Io_2	T_a =60°C, 200LFM airflow	Vo_1 (3.3V) Vo_2 (2.5V)	0.1 (i) 0	8.5 (ii) 2 (ii)	10.5 (iii) 2.25 (iii)	A
Input Voltage Range	V_{in}	Over I_o Range		10.8	—	13.2	VDC
Set Point Voltage Tolerance	V_o tol		Vo_1 Vo_2	— —	±16 ±12	±50 ±38	mV
Temperature Variation	Reg_{temp}	–40° >T_a > +85°C	Vo_1 Vo_2	— —	±1.0 ±0.5	— —	%V_o
Line Regulation	Reg_{line}	Over V_{in} range	Vo_1 Vo_2	— —	±10 ±5	±15 ±7	mV
Load Regulation	Reg_{load}	Over I_o range	Vo_1 Vo_2	— —	±10 ±10	±15 ±13	mV
Total Output Voltage Variation	ΔV_otot	Includes set-point, line, load –40° >T_a > +85°C	Vo_1 Vo_2	— —	±69 ±39	— —	mV
Efficiency	η			—	84	—	%
V_o Ripple (pk-pk)	V_r	20MHz bandwidth	Vo_1 Vo_2	— —	35 35	— —	mV_{pp}
Transient Response	t_{tr}	1A/µs load step, 50% to 100% $I_o$typ		—	60	—	µs
	ΔV_{tr}	V_o over/undershoot	Vo_1 Vo_2	— —	±50 ±30	— —	mV

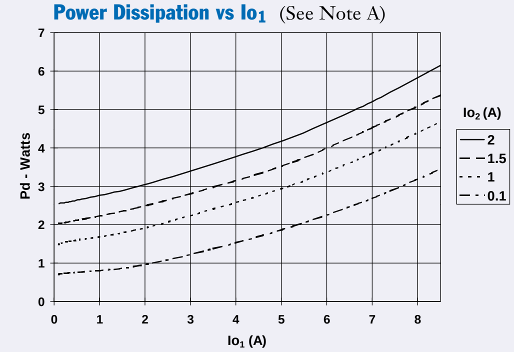
Notes: *(i)* *Io_1(min) current of 0.1A can be divided between both outputs, Vo_1 or Vo_2. The module will operate at no load with reduced specifications.*
(ii) *The typical current is that which can be drawn simultaneously from both outputs under the stated operating conditions.*
(iii) *The sum of Io_1 and Io_2 must be less than Io_1max, and Io_2 must be less than Io_2max.*

PT6982 Typical Characteristics

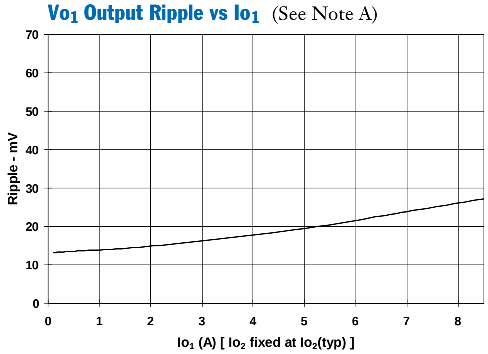
Efficiency vs Io_1 (See Note A)



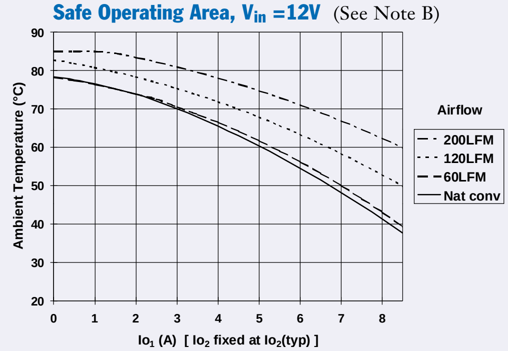
Power Dissipation vs Io_1 (See Note A)



Vo_1 Output Ripple vs Io_1 (See Note A)



Safe Operating Area, V_{in} =12V (See Note B)



Note A: *Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the Converter.*
Note B: *SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures*

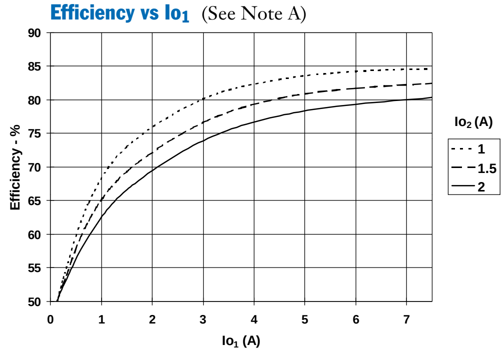
PT6983 Performance Specifications (Unless otherwise stated, T_a =25°C, V_{in} =12V, C_1 =560µF, C_2 =330µF, Io_1 =Io_1typ, and Io_2 =Io_2typ)

Characteristic	Symbol	Conditions		PT6983 (3.3V/1.8V) Min	Typ	Max	Units
Output Current	Io_1 Io_2	T_a =25°C, natural convection	Vo_1 (3.3V) Vo_2 (1.8V)	0.1 (i) 0	7.5 (ii) 2 (ii)	9.5 (iii) 2 (iii)	A
	Io_1 Io_2	T_a =60°C, 200LFM airflow	Vo_1 (3.3V) Vo_2 (1.8V)	0.1 (i) 0	7.5 (ii) 2 (ii)	9.5 (iii) 2 (iii)	A
Input Voltage Range	V_{in}	Over I_o Range		10.8	—	13.2	VDC
Set Point Voltage Tolerance	V_o tol		Vo_1 Vo_2	— —	±16 ±9	±50 ±27	mV
Temperature Variation	Reg_{temp}	–40° >T_a > +85°C	Vo_1 Vo_2	— —	±1.0 ±0.5	— —	%V_o
Line Regulation	Reg_{line}	Over V_{in} range	Vo_1 Vo_2	— —	±10 ±5	±15 ±7	mV
Load Regulation	Reg_{load}	Over I_o range	Vo_1 Vo_2	— —	±10 ±5	±15 ±7	mV
Total Output Voltage Variation	ΔV_otot	Includes set-point, line, load –40° >T_a > +85°C	Vo_1 Vo_2	— —	±69 ±28	— —	mV
Efficiency	η			—	81	—	%
V_o Ripple (pk-pk)	V_r	20MHz bandwidth	Vo_1 Vo_2	— —	35 35	— —	mV_{pp}
Transient Response	t_{tr}	1A/µs load step, 50% to 100% $I_o$typ		—	60	—	µs
	ΔV_{tr}	V_o over/undershoot	Vo_1 Vo_2	— —	±50 ±20	— —	mV

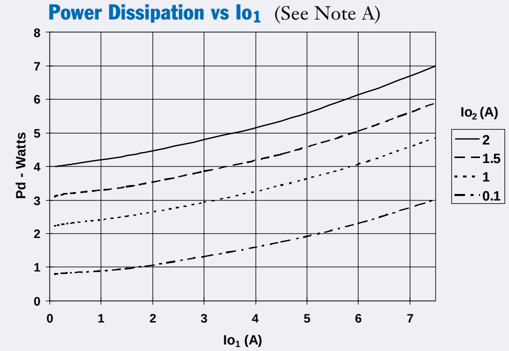
Notes: *(i)* *Io_1(min) current of 0.1A can be divided between both outputs, Vo_1 or Vo_2. The module will operate at no load with reduced specifications.*
(ii) *The typical current is that which can be drawn simultaneously from both outputs under the stated operating conditions.*
(iii) *The sum of Io_1 and Io_2 must be less than Io_1max, and Io_2 must be less than Io_2max.*

PT6983 Typical Characteristics

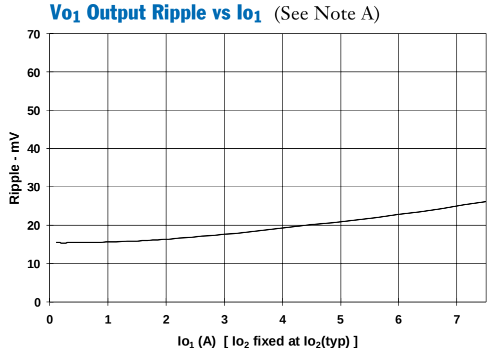
Efficiency vs Io_1 (See Note A)



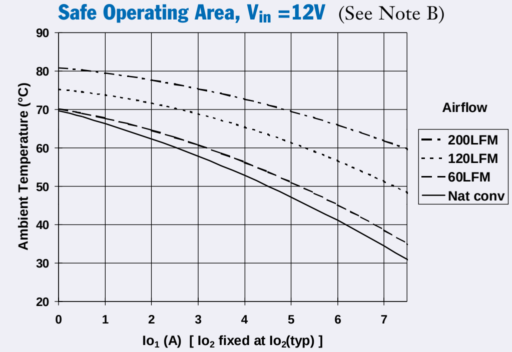
Power Dissipation vs Io_1 (See Note A)



Vo_1 Output Ripple vs Io_1 (See Note A)



Safe Operating Area, V_{in} =12V (See Note B)



Note A: *Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the Converter.*
Note B: *SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures*

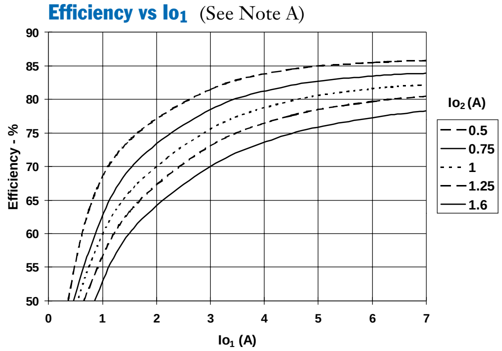
PT6984 Performance Specifications (Unless otherwise stated, T_a =25°C, V_{in} =12V, C_1 =560µF, C_2 =330µF, Io_1 =Io_1typ, and Io_2 =Io_2typ)

Characteristic	Symbol	Conditions		PT6984 (3.3V/1.2V) Min	Typ	Max	Units
Output Current	Io_1 Io_2	T_a =25°C, natural convection	Vo_1 (3.3V) Vo_2 (1.2V)	0.1 (i) 0	7 (ii) 1.6 (ii)	8.6 (iii) 1.6 (iii)	A
	Io_1 Io_2	T_a =60°C, 200LFM airflow	Vo_1 (3.3V) Vo_2 (1.2V)	0.1 (i) 0	7 (ii) 1.6 (ii)	8.6 (iii) 1.6 (iii)	A
Input Voltage Range	V_{in}	Over I_o Range		10.8	—	13.2	VDC
Set Point Voltage Tolerance	V_o tol		Vo_1 Vo_2	— —	±16 ±6	±50 ±18	mV
Temperature Variation	Reg_{temp}	–40° >T_a > +85°C	Vo_1 Vo_2	— —	±1.0 ±0.5	— —	$\%V_o$
Line Regulation	Reg_{line}	Over V_{in} range	Vo_1 Vo_2	— —	±10 ±5	±15 ±7	mV
Load Regulation	Reg_{load}	Over I_o range	Vo_1 Vo_2	— —	±10 ±5	±15 ±7	mV
Total Output Voltage Variation	ΔV_otot	Includes set-point, line, load –40° >T_a > +85°C	Vo_1 Vo_2	— —	±69 ±22	— —	mV
Efficiency	η			—	78	—	%
V_o Ripple (pk-pk)	V_r	20MHz bandwidth	Vo_1 Vo_2	— —	35 35	— —	mV_{pp}
Transient Response	t_{tr}	1A/µs load step, 50% to 100% $I_o$typ		—	60	—	µs
	ΔV_{tr}	V_o over/undershoot	Vo_1 Vo_2	— —	±50 ±20	— —	mV

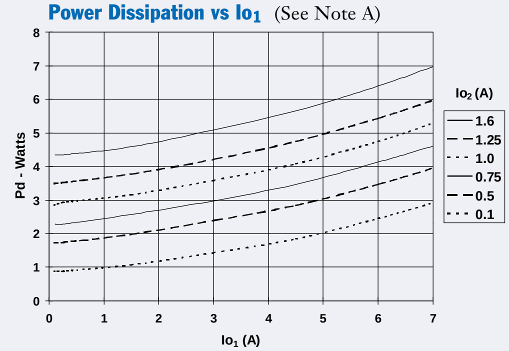
Notes: *(i)* *Io_1(min) current of 0.1A can be divided between both outputs, Vo_1 or Vo_2. The module will operate at no load with reduced specifications.*
(ii) *The typical current is that which can be drawn simultaneously from both outputs under the stated operating conditions.*
(iii) *The sum of Io_1 and Io_2 must be less than Io_1max, and Io_2 must be less than Io_2max.*

PT6984 Typical Characteristics

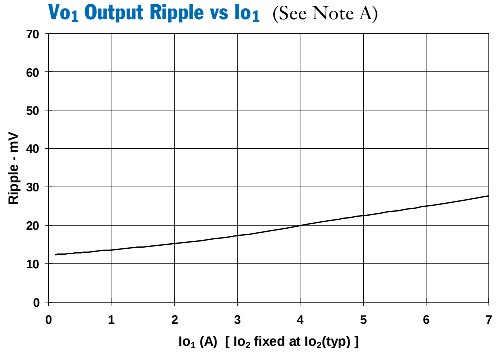
Efficiency vs Io_1 (See Note A)



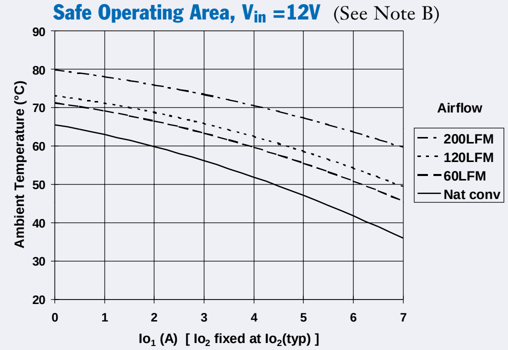
Power Dissipation vs Io_1 (See Note A)



Vo_1 Output Ripple vs Io_1 (See Note A)



Safe Operating Area, V_{in} =12V (See Note B)



Note A: *Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the Converter.*
Note B: *SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures*

PT6985 Performance Specifications

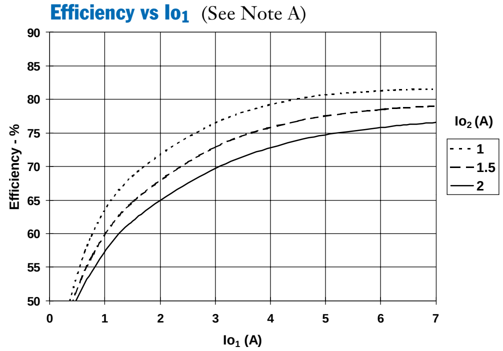
(Unless otherwise stated, T_a =25°C, V_{in} =12V, C_1 =560µF, C_2 =330µF, Io_1 =Io_1typ, and Io_2 =Io_2typ)

Characteristic	Symbol	Conditions		PT6985 (2.5V/1.2V) Min	Typ	Max	Units
Output Current	Io_1 Io_2	T_a =25°C, natural convection	Vo_1 (2.5V) Vo_2 (1.2V)	0.1 (i) 0	7 (ii) 2 (ii)	9 (iii) 2.2 (iii)	A
	Io_1 Io_2	T_a =60°C, 200LFM airflow	Vo_1 (2.5V) Vo_2 (1.2V)	0.1 (i) 0	7 (ii) 2 (ii)	9 (iii) 2.2 (iii)	A
Input Voltage Range	V_{in}	Over I_o Range		10.8	—	13.2	VDC
Set Point Voltage Tolerance	V_o tol		Vo_1 Vo_2	— —	±12 ±6	±38 ±18	mV
Temperature Variation	Reg_{temp}	–40° >T_a > +85°C	Vo_1 Vo_2	— —	±0.5 ±0.5	— —	$\%V_o$
Line Regulation	Reg_{line}	Over V_{in} range	Vo_1 Vo_2	— —	±10 ±5	±15 ±7	mV
Load Regulation	Reg_{load}	Over I_o range	Vo_1 Vo_2	— —	±10 ±5	±15 ±7	mV
Total Output Voltage Variation	ΔV_otot	Includes set-point, line, load –40° >T_a > +85°C	Vo_1 Vo_2	— —	±44 ±22	— —	mV
Efficiency	η			—	77	—	%
V_o Ripple (pk-pk)	V_r	20MHz bandwidth	Vo_1 Vo_2	— —	35 35	— —	mV_{pp}
Transient Response	t_{tr}	1A/µs load step, 50% to 100% $I_o$typ		—	60	—	µs
	ΔV_{tr}	V_o over/undershoot	Vo_1 Vo_2	— —	±50 ±20	— —	mV

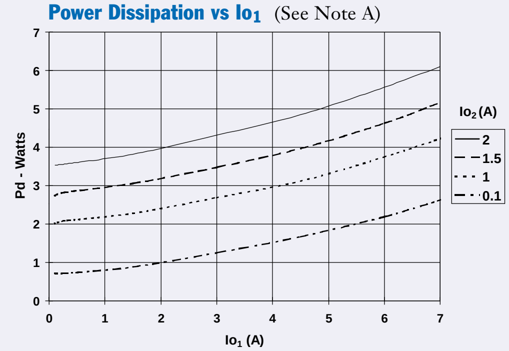
Notes: *(i)* *Io_1(min) current of 0.1A can be divided between both outputs, Vo_1 or Vo_2. The module will operate at no load with reduced specifications.*
(ii) *The typical current is that which can be drawn simultaneously from both outputs under the stated operating conditions.*
(iii) *The sum of Io_1 and Io_2 must be less than Io_1max, and Io_2 must be less than Io_2max.*

PT6985 Typical Characteristics

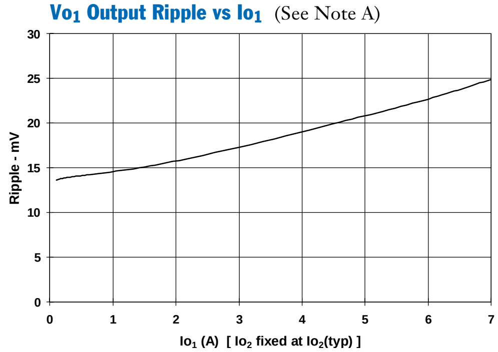
Efficiency vs Io_1 (See Note A)



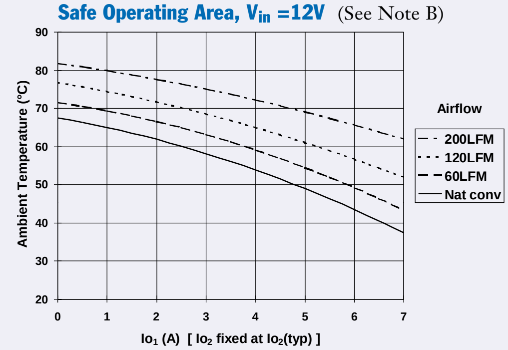
Power Dissipation vs Io_1 (See Note A)



Vo_1 Output Ripple vs Io_1 (See Note A)



Safe Operating Area, V_{in} =12V (See Note B)



Note A: *Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the Converter.*
Note B: *SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures*

Capacitor Recommendations for the Dual-Output PT6980 Regulator Series

Input Capacitors:

The recommended input capacitance is determined by 1.0 ampere minimum ripple current rating and 330µF minimum capacitance . Ripple current and <100mΩ equivalent series resistance (ESR) values are the major considerations, along with temperature, when designing with different types of capacitors. Tantalum capacitors have a recommended minimum voltage rating of 2 × the maximum DC voltage + AC ripple. This is necessary to insure reliability for input voltage bus applications

Output Capacitors: C_2(Required), C_3(Optional)

The ESR of the required capacitor (C_2) must not be greater than 50mΩ. Electrolytic capacitors have poor ripple performance at frequencies greater than 400kHz but excellent low frequency transient response. Above the ripple frequency, ceramic capacitors are necessary to improve the transient response and reduce any high frequency noise components apparent during higher current excursions. Preferred low ESR type capacitor part numbers are identified in Table 1. The optional 100µF capacitor (C_3) for V_2out can have an ESR of up to 200mΩ for optimum performance and ripple reduction. *(Note: Vendor part numbers for the optional capacitor, C_3, are not identified in the table. Use the same series selected for C_2)*

Tantalum Capacitors

Tantalum type capacitors may be used at the output, but only the AVX TPS series, Sprague 593D/594/595 series, or Kemet T495/T510 series. The AVX TPS series, Kemet or Sprague series tantalums are recommended over many other types due to their higher rated surge, power dissipation, and ripple current capability. As a caution, the TAJ series by AVX is not recommended. This series has considerably higher ESR, reduced power dissipation and lower ripple current capability. The TAJ Series is also less reliable than the AVX TPS series when determining power dissipation capability. Tantalum or Oscon® types are recommended for applications where ambient temperatures fall below 0°C.

Capacitor Table

Table 1 identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The number of capacitors required at both the input and output buses is identified for each capacitor type.

This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The RMS ripple current rating and ESR (Equivalent Series Resistance at 100kHz) are critical parameters necessary to insure both optimum regulator performance and long capacitor life.

Table 1: Input/Output Capacitors

Capacitor Vendor/ Component Series	Capacitor Characteristics					Quantity		
	Working Voltage	Value(µF)	(ESR) Equivalent Series Resistance	85°C Maximum Ripple Current(Irms)	Physical Size(mm)	Input Bus	Output Bus	Vendor Number
Panasonic FC	35V 35V 50V	680µF 560µF 680µF	0.043Ω 0.038Ω 0.048Ω	1690mA 1655mA 1835mA	16x15 12.5x20 16x20	1 1 1	1 1 1	EEUFC1V681S EEUFC1V561S EEUFC1H681
Un ited Chemi-con LXV/LXZ/ FX/FS	35V 50V 10V 20V	680µF 680µF 390µF 150µF	0.038Ω 0.048Ω 0.030Ω 0.024Ω	1660mA 1840mA 3080mA 3200mA	12.5x20 16x20 8x10.5 8x10.5	1 1 N/R 4	1 1 1 2	LXZ35VB681M112X20LL LXZ50VB681M16X20LL 10FX390M 20FX150M
Nichicon PL/ PM	35V 25V 35V	560µF 820µF 560µF	0.048Ω 0.049Ω 0.0048Ω	1360mA 1340mA 1360mA	16x15 16x15 16x15	1 1 1	1 1 1	UPL1V561MHH6 UPL1E821MHH6 UPM1V561MHH6
Panasonic FC Surface Mtg	35V 35V 35V	330µF 1000µF 470µF	0.065÷2Ω 0.038Ω 0.043Ω	>1205mA 2000mA 1690mA	12.5x16.5 18x16.5 16x16.5	2 1	2 1 1	EEVFC1V331LQ EEVFC1V1021N EEVFC1V471N
Oscon SS/SV	10V 10V	330µF 330µF	0.025Ω 0.025Ω	>3500mA >3800mA	10.0x10.5 10.3x10.3	N/R N/R	1 1	10SS330M 10SV330M Surface Mount(SV)
AVX Tantalum TPS	10V 10V	330µF 220µF	0.060÷2Ω 0.060÷2Ω	>2500mA >3000mA	7.3Lx 4.3Wx	N/R N/R	2 2	TPSV337M010R0060 TPSV227M010R0060
Kemet T510 T495	10V 10V	330µF 220µF	0.033Ω 0.07Ω÷2 =0.035Ω	1400mA >2000mA	7.3Lx5.7W x 4.0H	N/R N/R	1 2	T510X337M010AS T495X227M010AS
Sprague 594D	10V	330µF	0.045Ω	2350mA	7.3Lx 6.0Wx 4.1H	N/R	1	594D337X0010R2T

N/R –Not recommended. The voltage rating does not meet the minimin operating limits.

Adjusting the Output Voltage of the PT6980 Dual-Output Voltage Regulators

Each output voltage from the PT6980 series of integrated switching regulators (ISRs) can be independently adjusted higher or lower than the factory trimmed pre-set voltage. The voltages, Vo_1 and Vo_2 may be adjusted either up or down using a single external resistor [1]. Table 1 gives the adjustment range for both Vo_1 and Vo_2 for each model in the series as V_a(min) and V_a(max). Note that Vo_2 must always be lower than Vo_1 [2].

Vo_1 Adjust Up: To increase the output, add a resistor R_4 between pin 16 (V_1 Adjust) and pins 7-11 (GND) [1].

Vo_1 Adjust Down: Add a resistor (R_3), between pin 16 (Vo_1 Adjust) and pin 1 (Vo_1 Sense) [1].

Vo_2 Adjust Up: Add a resistor R_2 between pin 23 (Vo_2 Adjust) and pins 7-11 (GND) [1].

Vo_2 Adjust Down: Add a resistor (R_1) between pin 23 (Vo_2 Adjust) and pin 22 (Vo_2 Sense) [1].

Refer to Figure 1 and Table 2 for both the placement and value of the required resistor.

Notes:

1. Use only a single 1% resistor in either the (R_3) or R_4 location to adjust Vo_1, and in the (R_1) or R_2 location to adjust Vo_2. Place the resistor as close to the ISR as possible.
2. Vo_2 must always be at least 0.2V lower than Vo_1.
3. Both the Vo_1 and Vo_2 may be adjusted down to an alternative bus voltage by making, (R_3) or (R_1) respectively, a zero ohm link. Refer to the Table 1 footnotes for guidance.
4. Never connect capacitors to either the Vo_1 Adjust or Vo_2 Adjust pins. Any capacitance added to these control pins will affect the stability of the respective regulated output.
5. Adjusting either voltage (Vo_1 or Vo_2) may increase the power dissipation in the regulator, and change the maximum current available at either output. Consult the note on p.2 of the data sheet regarding Vo_1/Vo_2 loading.

The adjust up and adjust down resistor values can also be calculated using the following formulas. Be sure to select the correct formula parameter from Table 1 for the output and model being adjusted.

$$(R_1) \text{ or } (R_3) = \frac{10\,(V_a - V_r)}{V_o - V_a} - R_s \quad k\Omega$$

$$(R_2) \text{ or } (R_4) = \frac{10 \cdot V_r}{V_a - V_o} - R_s \quad k\Omega$$

Where: V_o = Original output voltage, (Vo_1 or Vo_2)
V_a = Adjusted output voltage
V_r = The reference voltage from Table 1
R_s = The series resistance from Table 1

Figure 1

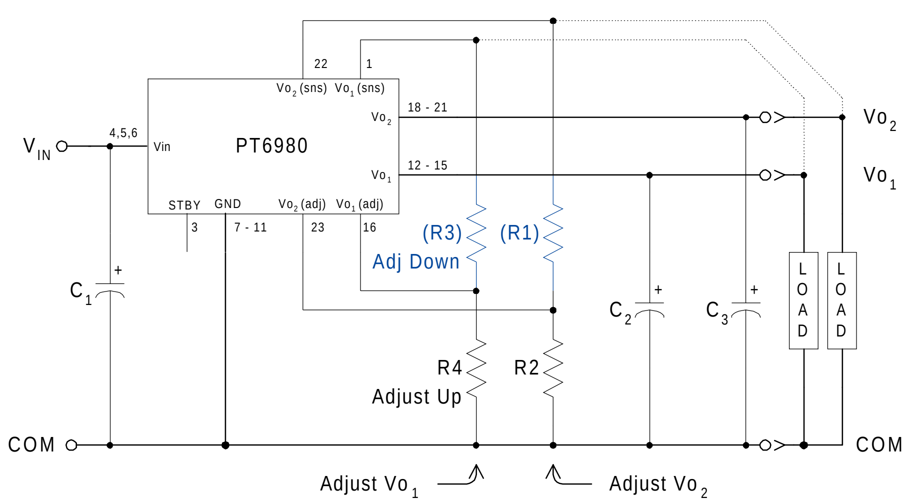


Table 1

ADJUSTMENT RANGE AND FORMULA PARAMETERS

V_{O1} Bus			**V_{O2} Bus (2)**		
Series Pt #	**PT6981/85**	**PT6982/83/84**	**PT6984/85**	**PT6981/83**	**PT6936**
Adj. Resistor	**(R3)/R4**	**(R3)/R4**	**(R1)/R2**	**(R1)/R2**	**(R1)/R2**
V_o(nom)	2.5V	3.3V	1.2V	1.8V	2.5V
Va(min)	1.8V *	2.5V *	1.0V †	1.5V †	1.8V †
Va(max)	3.6V	3.6V	1.5V #	2.4V	3.0
Vr	1.27V	1.27V	0.6125V	1.0V	1.0V
R_s (kΩ)	7.5	15.4	20.0	16.9	11.5

Ref. Note 3: * (R3) = Zero-ohm link
†(R1) = Zero-ohm link
(R2) = Zero-ohm link

Table 2

ADJUSTMENT RESISTOR VALUES

V_{O1} Bus		
Series Pt #	**PT6981/85**	**PT6982/83/84**
Adj. Resistor	**(R3)/R4**	**(R3)/R4**
V_o(nom)	2.5V	3.3V
V_a(req'd)		
1.8	(0.0)	
1.85	(1.4)kΩ	
1.9	(3.0)kΩ	
1.95	(4.9)kΩ	
2.0	(7.1)kΩ	
2.05	(9.8)kΩ	
2.1	(13.3)kΩ	
2.2	(23.5)kΩ	
2.3	(44.0)kΩ	
2.4	(106.0)kΩ	
2.5		(0.0)kΩ
2.6	120.0kΩ	(3.6)kΩ
2.7	56.0kΩ	(8.4)kΩ
2.8	34.8kΩ	(15.2)kΩ
2.9	24.3kΩ	(25.4)kΩ
3.0	17.9kΩ	(42.3)kΩ
3.1	13.7kΩ	(76.1)kΩ
3.2	10.6kΩ	(178.0)kΩ
3.3	8.4kΩ	
3.4	6.6kΩ	112.0k
3.5	5.2kΩ	48.1k
3.6	4.1kΩ	26.9k

V_{O2} Bus			
Series Pt #	**PT6984/85**	**PT6981/83**	**PT6982**
Adj. Resistor	**(R1)/R2**	**(R1)/R2**	**(R1)/R2**
V_o(nom)	1.2V	1.8V	2.5V
V_a(req'd)			
1.0	(0.0)kΩ		
1.05	(9.2)kΩ		
1.1	(28.8)kΩ		
1.15	(87.5)kΩ		
1.2			
1.25	101.5kΩ		
1.3	41.2kΩ		
1.35	20.8kΩ		
1.4	10.6kΩ		
1.45	4.5kΩ		
1.5	0.0kΩ	(0.0)kΩ	
1.55		(5.1)kΩ	
1.6		(13.1)kΩ	
1.65		(26.4)kΩ	
1.7		(53.1)kΩ	
1.75		(133.0)kΩ	
1.8			(0.0)kΩ
1.85		183.0kΩ	(1.6)kΩ
1.9		83.1kΩ	(3.5)kΩ
1.95		49.8kΩ	(5.8)kΩ
2.0		33.1kΩ	(8.5)kΩ
2.05		23.1kΩ	(11.8)kΩ
2.1		16.4kΩ	(16.0)kΩ
2.2		8.1kΩ	(28.5)kΩ
2.3		3.1kΩ	(53.5)kΩ
2.4		0.0kΩ	(129.0)kΩ
2.5			
2.6			88.5kΩ
2.7			38.5kΩ
2.8			21.8kΩ
2.9			13.5kΩ
3.0			8.5kΩ

R_1/R_3 = (Blue), R_2/R_4 = Black

Using the Standby Function on the PT6980 Series of Dual-Output Voltage Regulators

Both output voltages of the 23-pin PT6980 dual-output converter may be disabled using the regulator's 'Standby' function. This function may be used in applications that require power-up/shutdown sequencing, or wherever there is a requirement to control the output voltage On/Off status with external circuitry.

The standby function is provided by the *STBY** control (pin 3). If pin 3 is left open-circuit the regulator operates normally, and provides a regulated output at both Vo_1 (pins 12–15) and Vo_2 (pins 18–21) whenever a valid supply voltage is applied to V_{in} (pins 4, 5, & 6) with respect to GND (pins 7-11). If a low voltage[1] is then applied to pin-3 both regulator outputs will be simultaneously disabled and the input current drawn by the ISR will drop to a typical value of 4mA. The standby control may also be used to hold-off both regulator outputs during the period that input power is applied.

The standby pin is ideally controlled using an open-collector (or open-drain) discrete transistor (See Figure 1). The open-circuit voltage is the input voltage $+V_{in}$. Table 1 gives the circuit parameters for this control input.

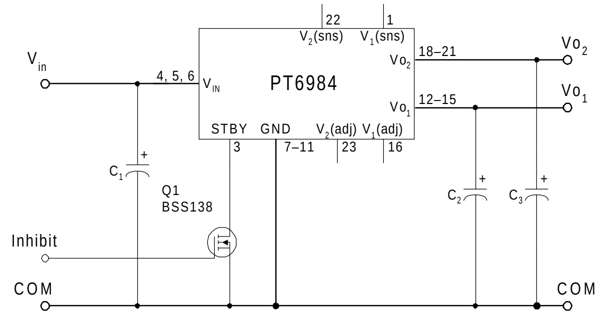
Table 1 Standby Control Parameters [1, 2]

Parameter	Min	TYP	Max
Enable (V_{IH})	—	—	Open circuit
Disable (V_{IL})	–0.1V	—	0.4V [1]
V_{STBY} (open circuit)	—	$+V_{in}$ [2]	—
I_{STBY} (I_{IL})	—	—	–0.5mA

Notes:

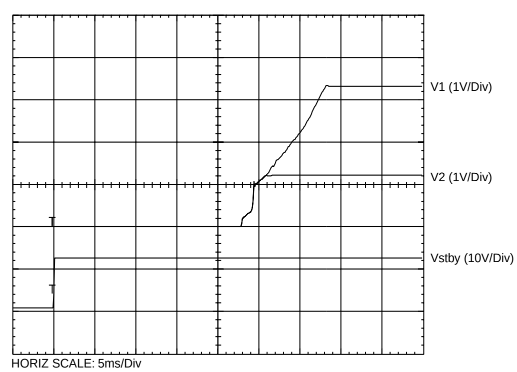
1. The standby control input is *Not* compatible with TTL or other devices that incorporate a totem-pole output drive. Use only a true open-collector device, preferably a discrete bipolar transistor (or MOSFET). To ensure the regulator output is disabled, the control pin must be pulled to less than 0.4Vdc with a low-level 0.5mA sink to ground.
2. The standby control input requires no external pull-up resistor. The open-circuit voltage of the STBY* pin is the input voltage $+V_{in}$.
3. When the regulator output is disabled the current drawn from the input source is typically reduced to 4mA.

Figure 1



Turn-On Time: Turning Q_1 in Figure 1 off removes the low-voltage signal at pin 3 and enables the PT6980 series regulator. Following a delay of about 25ms, Vo_1 and Vo_2 rise together until the lower voltage, Vo_2, reaches its set output. Vo_1 continues to rise until both outputs reach full regulation voltage. The total power-up time is less than 40ms, and is relatively independent of load, temperature, and output capacitance. Figure 2 shows waveforms of the output voltages, Vo_1 and Vo_2, for a PT6984 (3.3V/1.2V). The turn-off of Q_1 corresponds to the rise in V_{STBY}. The waveforms were measured with a 12V input voltage, and with resistive loads of 5A and 1.25A at the Vo_1 and Vo_2 outputs respectively.

Figure 2



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